AP1355AEM
Amplifier for Hall Element

1. General Descriptions

AP1355AEM is an amplifier specially designed for Hall Element. The AP1355AEM integrates built-in current source for driving a Hall Element and amplifier for Hall output. The current source and offset voltage of Hall Element are controllable by external voltage supply, so as to calibrate characteristics of Hall Element and to calibrate errors after installation of Hall element to the system.

2. Features

- Input Voltage ±13.5V ～ ±15V ～ ±16.5V
- Operating Temperature range –40°C ～ 105°C
- Built-in current source for Hall Element 5mA±5.4% @ Ta= 25°C (+0.045%/°C)
- Amplifier Gain Gain A ×180
  Gain B ×95
- Offset Voltage Offset Calibration Range ±1.85V(typ)、
- Offset Calibration Accuracy ±2.0mV
- Built-in Voltage Reference 5.0V±2% @ Ta= 25°C
- Output Drive Ability ±10mA
- Package 16-pin TSSOP
- ESD Level HBM = ±2.0kV

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram

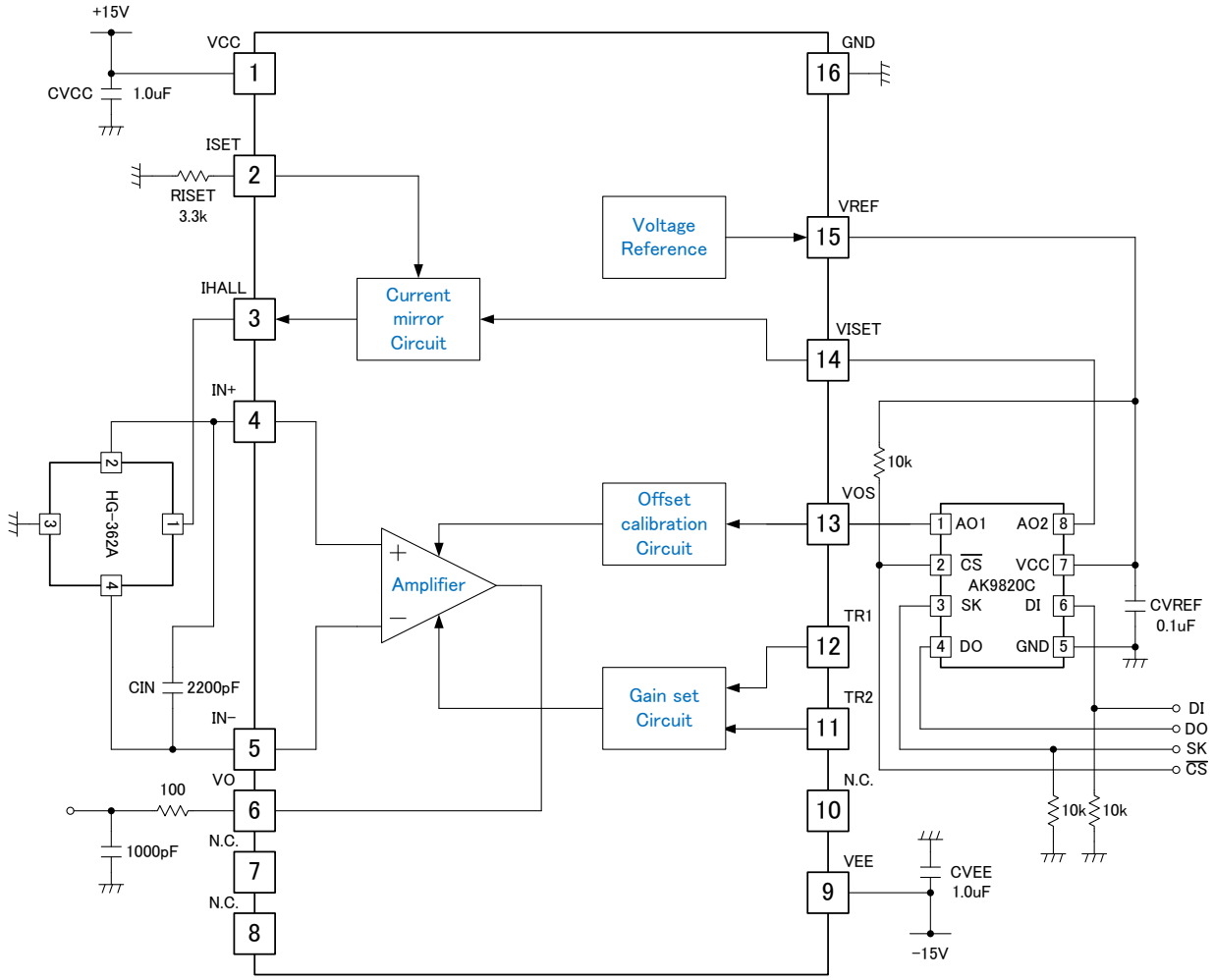


Figure 1. Block Diagram

■ Functions

Block	Functions
Amplifier	It amplifies the generated voltage of Hall Element. It can change the gain by making the short circuit between TR1 pin and TR2 pin.
Offset Calibration Circuit	It adjusts the offset of the amplifier output. The offset is adjustable by inputting the voltage to VOS pin.
Voltage Reference	It outputs the reference voltage (5V). Its voltage is supplied for the power supply of DAC.
Current Mirror Circuit	It supplies the current to the hall element. The current is adjustable by inputting the voltage to VISET pin.

■ D/A Converter (AK9820CTH)

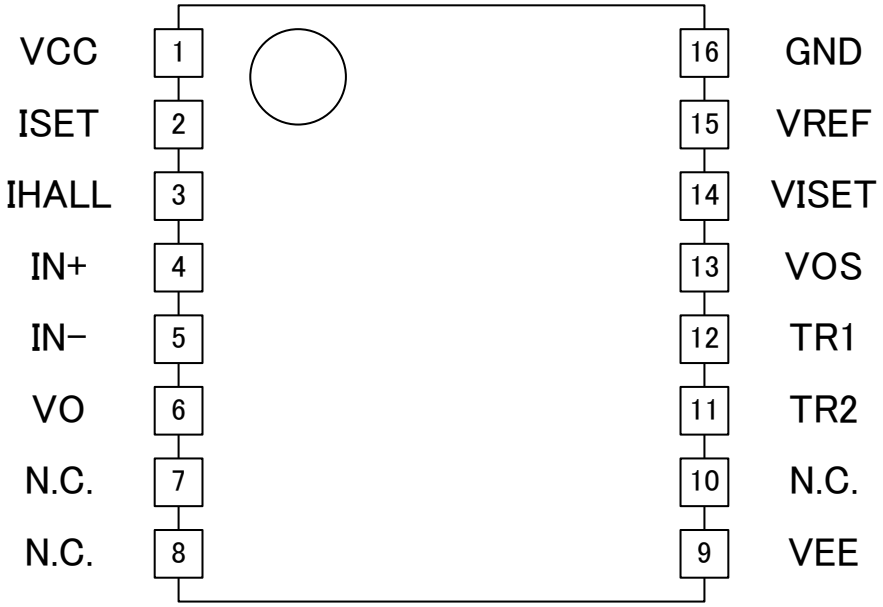
AK9820CTH inputs the voltage to the offset calibration circuit, and sets up the current for Hall Element.

5. Ordering Information

AP1355AEM –40°C ～ 105°C 16-pin TSSOP

6. Pin Configurations and Functions

■ Pin Configurations



■ Pin Functions

No.	Pin Name	I/O	Descriptions
1	VCC	I	Positive power supply
2	ISET	I	Pin for setting driving current of Hall Element. Connect external resistor RISET.
3	IHALL	O	Current source pin for driving Hall Element. Driving current IHALL can be calculated by following formula; $I_{IHALL}=V_{VISET}\div R_{ISET}\times 3$
4	IN+	I	Input pin of Hall signal. Connect OUT+ of HG-362A.
5	IN-	I	Input pin of Hall signal. Connect OUT- of HG-362A.
6	VO	O	Output pin
7	N.C.	-	No connection
8	N.C.	-	No connection
9	VEE	I	Negative Power supply
10	N.C.	-	No connection
11	TR2	I	Pin for gain setting
12	TR1	I	Pin for gain setting
13	VOS	I	Pin for offset voltage control. Connect AO1 of AK9820CTH.
14	VISET	I	Pin for control of driving current of Hall Element. Connect AO2 of AK9820CTH.
15	VREF	O	Voltage reference pin. Connect VCC of AK9820CTH. Temperature characteristics differ by changing load. Do not connect any external parts except for parts with specified load.
16	GND	-	GND

Note 1. It should be shorted by below 1ohm, when the pins between TR1 and TR2 are shorted.

7. Absolute Maximum Ratings

Parameter	Symbol	min	max	Units	Condition
Supply Voltage	V_{CC}	GND	+18	V	
	V_{EE}	-18	GND	V	
Input Pin	IN-, IN+, TR1,TR2, VOS	V_{EE}	V_{CC}	V	
	VISET	GND	V_{CC}	V	
Output Pin	VO	V_{EE}	V_{CC}	V	
	ISET, IHALL, VREF	GND	V_{CC}	V	
Storage Temperature Range	T_{STG}	-55	+150	°C	
Junction Temperature Range	T_J	125		°C	
Power Dissipation (Note 3)	P_D	200		mW	Ta=105°C

Note 2. All Voltages with respect to GND pin.
Note 3. Thermal Resistance of PKG(θ_{JA}): 112.6°C/W (JEDEC51, four-layers PCB)

WARNING: The maximum ratings are the absolute limitation values with the possibility of the IC breakage. When the operation exceeds this standard quality cannot be guaranteed.

8. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Units
Positive Power Supply Voltage	V_{CC}	13.5	15	16.5	V
Negative Power Supply Voltage	V_{EE}	-16.5	-15	-13.5	V
Operating Temperature Range	T_{OPR}	-40	25	105	°C
VO Capacitor	C_{VO}	-	-	470	pF
VREF Capacitor	C_{VREF}	-	0.1	0.47	µF
VCC Capacitor	C_{VCC}	0.47	1.0	-	µF
VEE Capacitor	C_{VEE}	0.47	1.0	-	µF
Input Capacitor	C_{IN}	1650	2200	2750	pF

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

9. Electrical Characteristics

Ta=-40°C ~105°C、VCC=13.5V~16.5V、V_{EE}= -V_{CC}, unless otherwise specified.

Parameter	Symbol	min	typ	max	Units	Conditions
Supply Current	I_{CC}	-	9.0	11.0	mA	R_{ISET}=3.00kΩ, V_{VISET}=5.0V
	I_{EE}	-	-2.0	-3.0	mA	V_{VOS}=2.5V, HE:HG-362A
At Startup, Supply Current	I_{CC}	-	-	11.0	mA	V_{CC},V_{EE}=0~±16.5V, I_{SET}=3.00kΩ
	I_{EE}	-	-	-3.0	mA	V_{VISET}= V_{VREF}=V_{VOS}, HE:HG-362A
Reference Voltage Source						
Reference Voltage (25°C)	V_{REF}	4.9	5.0	5.1	V	I_{VREF}=0mA, V_{VISET}=5.0V V_{VOS}=2.5V, R_{ISET}=3.00kΩ, Ta=25°C
At Startup, Reference Voltage	V_{REF}	-0.6	-	6.5	V	
Temperature Characteristics of Reference Voltage	ΔV_{REF}	-100	0	+100	ppm/°C	I_{VREF}=0mA, V_{VISET}=5.0V V_{VOS}=2.5V, R_{ISET}=3.00kΩ
Load Regulation	$LoReg_{VREF}$	-	-	100	mV	I_{VREF}=0 to 5.5mA, V_{VISET}=5.0V V_{VOS}=2.5V, R_{ISET}=3.00kΩ
ISET Pin						
At ISET Pin Offset Voltage	V_{ISETO}	-50	-10	5	mV	V_{ISETO} = V_{ISET}-V_{VISET}, R_{ISET}=2.7kΩ～7.5kΩ, V_{VISET}=0.9V～5.2V, V_{VOS}=2.5V
ISET Pin Voltage, Load Regulation	$LoReg_{ISET}$	-	-	50	mV	R_{ISET}=2.7kΩ～7.5kΩ, V_{VISET}=0.9V～5.2V, V_{VOS}=2.5V
Hall Element Driving Current						
HALL Current (25°C)	I_{HALL}	4.73	5.0	5.27	mA	I_{IHALL}= V_{VISET} /R_{ISET} ×3, R_{ISET}= 3.00kΩ, V_{VISET}= V_{VREF}, V_{VOS}=2.5V, Ta=25°C
HALL Current (105°C)	I_{HALL}105	4.76	5.18	5.59	mA	I_{IHALL}= V_{VISET} /R_{ISET} ×3 R_{ISET}=3.00kΩ, R_{ISET} Temperature Characteristic =0ppm/°C, V_{VISET}=V_{VREF}, V_{VOS}=2.5V
HALL Current (-40°C)	I_{HALL}-40	4.46	4.85	5.24	mA	I_{IHALL}= V_{VISET} /R_{ISET} ×3 R_{ISET}=3.00kΩ, R_{ISET} Temperature Characteristic =0ppm/°C, V_{VISET}=V_{VREF}, V_{VOS}=2.5V
Temperature Drift of HALL Current	ΔI_{HALL}	200	450	700	ppm/°C	V_{VISET}=0.9V～5.2V, V_{VOS}=2.5V R_{ISET}=2.7kΩ～7.5kΩ,
Ratio of ISET Pin Current to Hall Current (25°C)	I_{HALL} / I_{ISET}	2.90	3.0	3.10	-	V_{VISET}=0.9V～5.2V, V_{VOS}=2.5V, R_{ISET}=2.7kΩ～7.5kΩ, Ta=25°C
Maximum HALL Current	$I_{HALL\ MAX}$	5.8	-	-	mA	R_{ISET}=1.0kΩ, R_{IHALL}=1.92kΩ V_{VOS}=2.5V, V_{VISET}=5.2V

Ta=-40°C ~105°C、VCC=13.5V~16.5V、V_{EE}= -V_{CC}, unless otherwise specified.

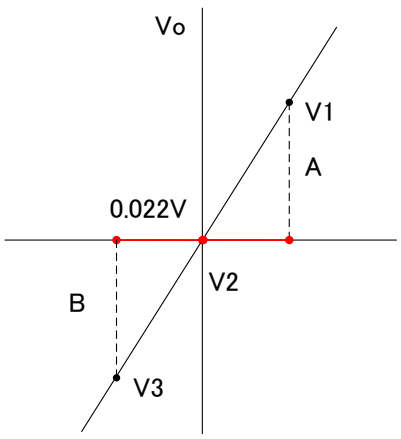
Parameter	Symbol	min	typ	max	Units	Conditions
Amplifier（Offset Calibration）						
Output Voltage A	V_{OS_A}	-0.20	0	0.20	V	V_{VOS}=1/2V_{REF}, TR1-TR2=0Ω VIN+=VIN-= 0~4V, I_{VO} =0mA V_{VISET}=5.0V
Output Voltage B	V_{OS_B}	1.65	1.85	2.05	V	V_{VOS}=0V, TR1-TR2=0Ω VIN+=VIN-= 0~4V, I_{VO} =0mA V_{VISET}=5.0V
Output Voltage C	V_{OS_C}	-2.05	-1.85	-1.65	V	V_{VOS}=V_{REF}, TR1-TR2=0Ω VIN+=VIN-= 0~4V, I_{VO} =0mA V_{VISET}=5.0V
Amplifier（DC）						
Input Bias Current	I_{IB}	-	-15	-70	nA	VIN+=VIN-= 0~7.5V
Input Offset Current	I_{IO}	-	±1.5	±30	nA	VIN+=VIN-= 0~7.5V
Common Mode Input Voltage Range	V_{ICR}	V_{CC} -3.0	V_{CC} -2.0	-	V	CMR > 80dB, (Ta=25°C～105°C) CMR > 75dB, (Ta=-40°C～below 25°C) Gain=180, I_{VO} =0mA
		-	V_{EE} +2.0	V_{EE} +3.0	V	
Maximum Output Voltage Range	V_{OM}	V_{CC} -3.0	-	-	V	R_L =2kΩ
		-	-	V_{EE} +3.0	V	
Output Current	$I_{O\ SINK}$	10	-	-	mA	VIN+=2V, VIN-=3V, V_{VO}=0V
	$I_{O\ SOURCE}$	-	-	-10	mA	VIN+=3V, VIN-=2V, V_{VO}=0V
Amplifier（DC2）						
Amplifier Gain A	Gain A	TYP -5%	180	TYP +5%	times	TR1-TR2=0Ω, V_{VO}=±4.0V I_{VO} =0mA
Amplifier Gain A	Gain A	TYP -5%	180	TYP +5%	times	TR1-TR2=0Ω, V_{CC},V_{EE}=±15V V_{VO}=±12.0V, I_{VO} =0mA
Amplifier Gain B	Gain B	TYP -5%	95	TYP +5%	times	TR1-TR2=Open, V_{VO}=±4.0V I_{VO} =0mA
Amplifier Gain B	Gain B	TYP -5%	95	TYP +5%	times	TR1-TR2=Open, V_{CC},V_{EE}=±15V V_{VO}=±12.0V, I_{VO} =0mA
Linearity of Amplifier Gain A	-	-	-	±0.5	%	V_{VO}=±4.0V

■ The equation of the Linearity of Gain A

V_{VO}= ±4.0V, ±4.0V / 180= ±0.022V

A: V1-V2 amount of change
B: V2-V3 amount of change

Equation：(A-B)/{(A+B)/2}×100

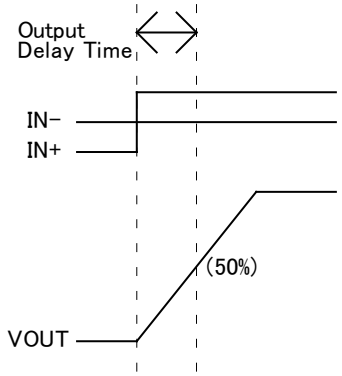


Ta=-40°C ~105°C、VCC=13.5V~16.5V、V_{EE}= -V_{CC}, unless otherwise specified.

Parameter	Symbol	min	typ	max	Units	Conditions
Amplifier（AC）						
Slew Rate	SR	5	8	-	V/μs	C_L =100pF, R_L≧2kΩ, Gain=180, 95
Output Delay Time	t_{dely}	-	1.0	3.0	μs	Gain=180, C_L =100pF , R_L≧2kΩ
Input Referred Voltage Noise	V_{NI}	-	4	8	μVrms	HPF=400Hz, LPF=30kHz VIN+=VIN-= 0V
Common Mode Rejection Ratio	CMR	80	100	-	dB	Ta=25°C～105°C
		75	-	-	dB	Ta=-40°C～below 25°C
Protection						
VREF limit Current	-	6	12	20	mA	
Thermal Protection	-	135	155	180	°C	

■Output Delay Time

Output Delay Time is specified the time of up to 50% of VOUT from IN+/IN- start-up.



10. Functional Descriptions

AP1355AEM is, as the amplifier for the Hall Element, "Drive Current Circuit" which supplies the current to the Hall Element, "Amplification Circuit" which amplifies the output voltage of the Hall Element, and "Offset Calibration Circuit" which adjusts the offset of the Amplification Circuit output. Furthermore, it supplies the voltage of 5V to the external DAC which controls "Drive Current Circuit" and "Offset Calibration Circuit" as the power supply.

10.1 Drive Current Circuit

The current (I_{IHALL}) which is supplied from IHALL pin to the Hall Element is calculated by the resistor (R_{ISET}) of ISET pin and the voltage (V_{VISET}) of VISET pin.

$$I_{IHALL}=V_{VISET} / R_{ISET} \times 3 \qquad (Ta=25°C)$$

And, as for the set up current (I_{IHALL}), it is set up to have the temperature characteristic of about 450ppm/°C(typ.) to correct the temperature characteristic of the Hall Element. But, the temperature characteristic of the external resistor (R_{ISET}) is 0ppm/°C at that time.
And, the setup range for the resistor (R_{ISET}) is 2.7kΩ to 7.5kΩ, and the voltage (V_{VISET}) is 1.0V to 5.0V.

10.2 Amplifier Circuit

Amplification Circuit is the measurement amplifier structure using three Operational Amplifiers.
The Amplifier Gain is selectable 95 times and 180 times by shorting the pins between TR1 pin and TR2 pin.

$$\Delta Vout = \Delta Vin\ (100k\Omega/10k\Omega)(1+2\times 42.5k\Omega/(5k\Omega \text{ or } 10k\Omega))$$

And, the DC offset of the output voltage is adjustable by "Offset Calibration Circuit".

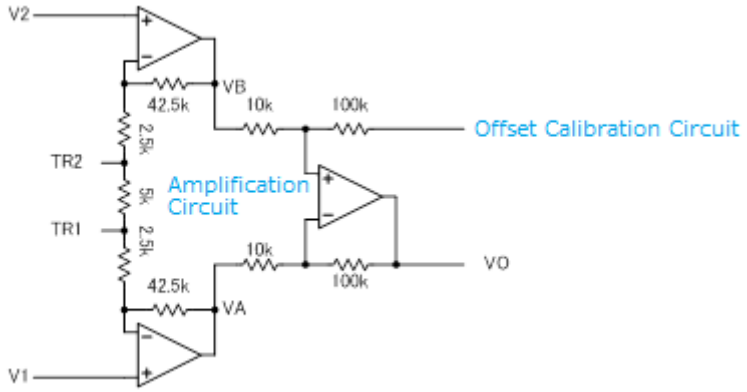


Figure 2. Amplification Circuit

When the voltage which is at the output of the offset calibration circuit is 0V, the output voltage is VO= (100k/10k) × (VB-VA). When it is based on the virtual short, the input pins both amplifiers (V1, V2) can be considered the same voltage.
It supplies the same current through each resistor in the line from VA to VB (to 42.5k to 10k to 42.5k to VB), because the current does not flow into the input pin.

For that, the equation becomes;

(VA-V1) / 42.5k = (V1-V2) / 10k = (V2-VB) / 42.5k
VA-VB = 42.5k / 10k×(V1-V2), V2-VB = 42.5k / 10k×(V1-V2)

By the above two equations;

VA-VB-(V1-V2) = (42.5k+42.5k)/10k×(V1-V2)
VA-V1 = (1+(42.5k+42.5k)/10k)×(V1-V2)

And, VO becomes;

VO = 100k/10k×(1+(42.5k+42.5k)/10k)×(V1-V2)

10.3 Offset Calibration Circuit

The DC offset of the amplifier output is adjustable by inputting the voltage to VOS pin.
The offset voltage is adjustable in the typical range from +1.85V to -1.85V by inputting the voltage (from 0V to 5V) to VOS pin.

・The equation for the component values
Specification Values

① VOS pin：0V VO pin：1.85V
② VOS pin：2.5V VO pin：0V
③ VOS pin：5V VO pin：-1.85V

When it set up VOS pin as the horizontal axis (from ① to ③), VO pin as the vertical axis, It is y=1.85-2.5x, (ex. y=0V, x=0.74)

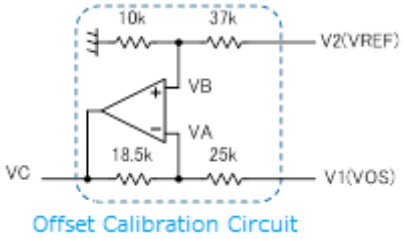


Figure 3. Offset Calibration Circuit

VB=V2/(37k+10k)×10k

The current value through the register of 25kΩ is the below, because it becomes VA=VB by the virtual short.

I=(V1-VA)/25k=(V1-VB)/18.5k=(V1-(V2×10k)/(10k+37k))/18.5k

VC=VA-I×18.5k=VB- I×25k
VC=-18.5k/25k×V1+(10k/(10k+37k)×V2×(1+18.5k/25k)
VC=-0.74×V1+0.370×V2

The voltage of the precision which is divided by VREF/1023 is inputted to VOS.

10.4 Reference Voltage Circuit

5.0V which is the reference voltage is outputted from VREF pin. It is available for an external DAC.

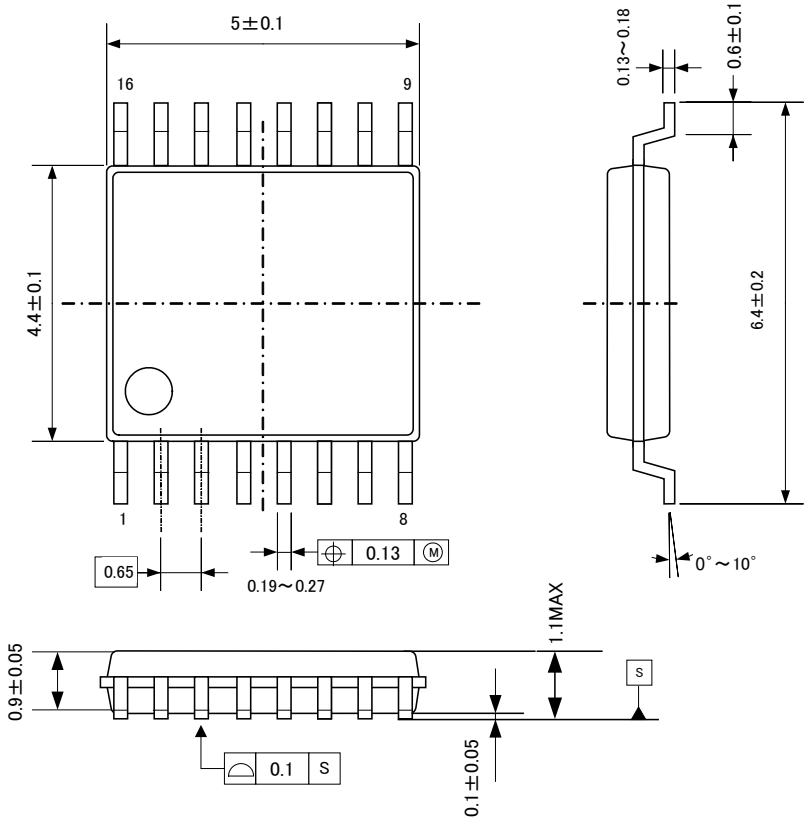
10.5 Protection Circuit

VREF Current Limit ：The VREF Current is limited below 12mA (typ.).
VO Current Limit ：The VO Current is limited below ±30mA(typ.).
Thermal Protection：When the internal temperature in IC exceeds 155°C (typ.), the current for each circuit in IC is turned off and all circuit is in shutdown.

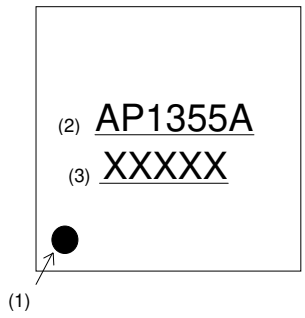
11. Package

■ Outline Dimensions

・16-pin TSSOP (Unit : mm)



■ Marking



(1) 1pin Indication

(2) Market No.

(3) Date Code (5digits)

Year Code(the rightmost digit) (ex. “2015” → “5”)、

Week Code throughout the year(two digit)、

Manegement Code(two digit)

12. Revision History

Date (YY/MM/DD)	Revision	Page	Contents
15/07/28	00	-	First Edition

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