DFBR030U3LP

3.0A SBR® FULL BRIDGE RECTIFIER

Features

- Dual 30V N-Channel MOSFETs (Q1, Q2) with Dual 3.0A Super Barrier Rectifier Diodes (D1, D2) packaged in a 4.0 x 4.0 x 0.6mm DFN package
- Full-Bridge Rectifier Block
- Super Barrier Rectifiers (D1, D2)
  - Ultra low forward voltage drop
  - Patented Super Barrier Rectifier technology
  - +150°C operating temperature
  - ±8kV ESD protection (HBM, 3B)
  - ±25kV ESD protection (IEC61000-4-2 Level 4, Air Discharge)
- N-Channel MOSFET (Q1, Q2)
  - Low On-Resistance to minimize conduction loss
  - Low Gate Threshold Voltage
  - Low Input Capacitance
  - Fast Switching Speed
  - Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

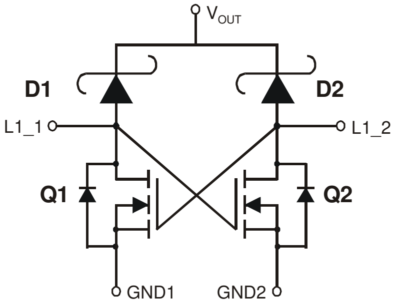
Mechanical Data

- Case: U-DFN4040-8
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiPdAu over Copper Leadframe (Lead-Free Plating); Solderable per MIL-STD-202, Method 208 ⓔ4
- Terminal Connections: See Diagram
- Weight: 0.031 grams

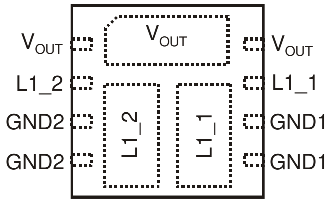
Applications

- Wireless Charging
- AC-DC Rectification
- Optimized for Power Management Applications for Portable Products

U-DFN4040-8



Device Schematic (Dual Channel)



Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Compliance	Case	Packaging
DFBR030U3LP-13	Standard	U-DFN4040-8	4,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

U-DFN4040-8

FB302 = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Digit of Year (ex: 15 for 2015)
WW = Week Code (01 to 53)

Maximum Ratings – D1, D2 (@T_A = +25°C, unless otherwise specified.)

Single phase, half wave, 60Hz, resistive or inductive load.
For capacitance load, derate current by 20%.

Characteristic	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_{RM}	30	V
RMS Reverse Voltage	$V_{R(RMS)}$	21	V
Average Rectified Output Current (See Figure 1)	I_O	3.0	A
Non-Repetitive Peak Forward Surge Current 8.3ms Single Half Sine-Wave Superimposed on Rated Load	I_{FSM}	20	A

Maximum Ratings – Q1, Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Input Voltage Between Two MOSFET Drain	V_{LL}	30	V
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current (Note 5)	I_D	3.2	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	500	mW
Thermal Resistance, Junction to Ambient Air (Note 5)	$R_{\theta JA}$	250	°C/W
Power Dissipation (Note 6)	P_D	1000	mW
Thermal Resistance, Junction to Ambient Air (Note 6)	$R_{\theta JA}$	125	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics – D1, D2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Breakdown Voltage (Note 7)	$V_{(BR)R}$	30	—	—	V	I_R = 400μA
Forward Voltage Drop	V_F	—	0.25	0.278	V	I_F = 0.1A, T_J = +25°C
		—	0.33	0.37		I_F = 1.0A, T_J = +25°C
		—	0.36	0.42		I_F = 2.0A, T_J = +25°C
		—	0.24	0.27		I_F = 0.1A, T_J = +125°C
		—	0.33	0.36		I_F = 1.0A, T_J = +125°C
		—	0.35	0.40		I_F = 2.0A, T_J = +125°C
Leakage Current (Note 7)	I_R	—	50	150	μA	V_R = 5V, T_J = +25°C
		—	100	400	μA	V_R = 30V, T_J = +25°C
		—	6	15	mA	V_R = 5V, T_J = +125°C
		—	10	20	mA	V_R = 30V, T_J = +125°C

Notes: 5. Part mounted on FR-4 board with recommended pad layout, which can be found on our website at http://www.diodes.com.
6. Part mounted on FR-4 board with 1-in sq pad layout, 2oz Cu.
7. Short duration pulse test used to minimize self-heating effect. Pulse width ≤ 300μs, duty cycle ≤ 2%.

Electrical Characteristics – Q1, Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	220	μA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±200	μA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1	—	2.2	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	13	--	mΩ	V_{GS} = 10V, I_D = 2.0A
			17	26		V_{GS} = 10V, I_D = 3.2A
			22	--		V_{GS} = 4.5V, I_D = 2.0A
			23	32		V_{GS} = 4.5V, I_D = 3.2A
Forward Transconductance	g_{fs}	—	7	—	S	V_{DS} =15V, I_D = 2.0A
Diode Forward Voltage (Note 7)	V_{SD}	0.5	—	1.2	V	V_{GS} = 0V, I_S = 2.25A

Electrical Characteristics – DFBR030U3LP (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Rectifying Forward Voltage (Note 7)	Vfd2	—	0.45	0.56	V	Input voltage V_{LL} = ±5V; The output current of Rectifier I_{OUT} = 2A
Rectifier leakage current	Ileak	—	30	1000	μA	Input voltage V_{LL} = 16V; No Load on the Rectifier output
Rectifier Reverse leakage current	Irleak	—	20	1000	μA	Input voltage V_{LL} = 0V; The output voltage of the Rectifier V_{OUT} = 5V

Note: 7. Short duration pulse test used to minimize self-heating effect. Pulse width ≤ 300μs, duty cycle ≤ 2%.

Typical Performance Curves – D1, D2

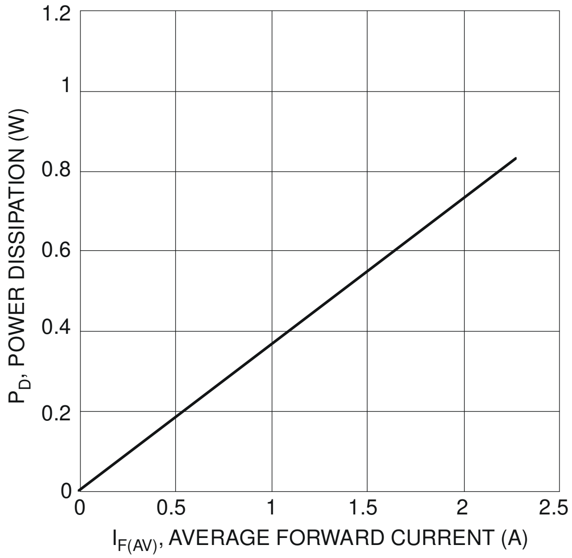


Figure 1 Forward Power Dissipation

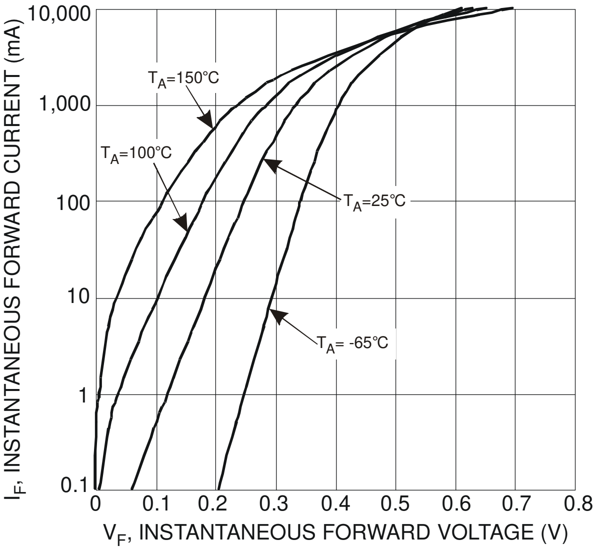


Figure 2 Typical Forward Characteristics

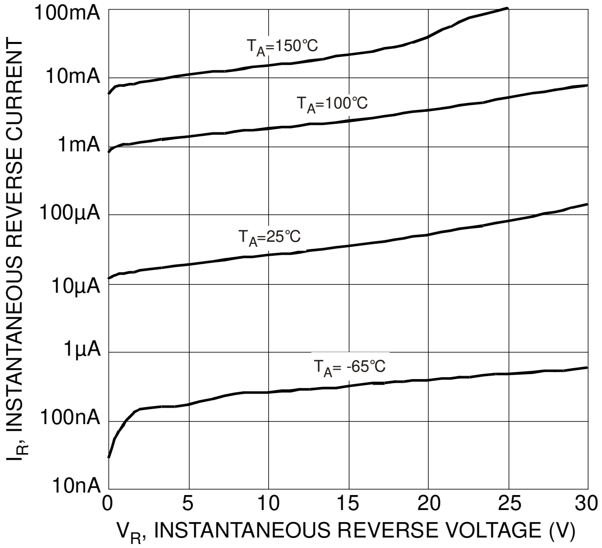


Figure 3 Typical Reverse Characteristics

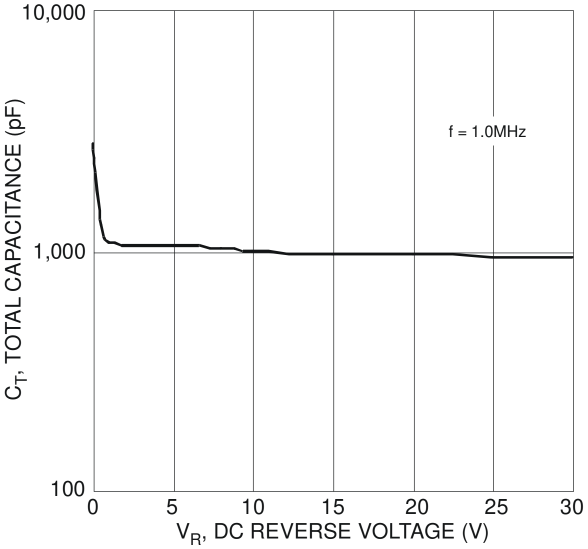


Figure 4 Total Capacitance vs. Reverse Voltage

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Typical Performance Curves – Q1, Q2

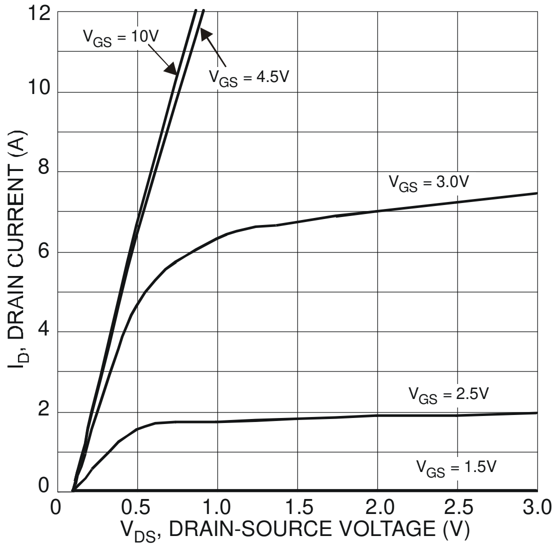

Figure 5 Typical Output Characteristics

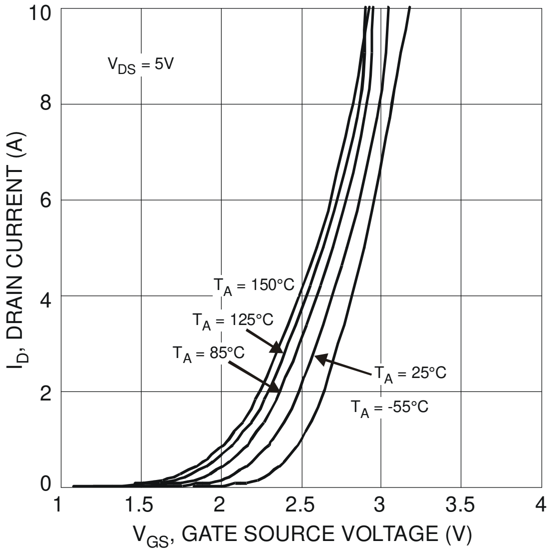

Figure 6 Typical Transfer Characteristics

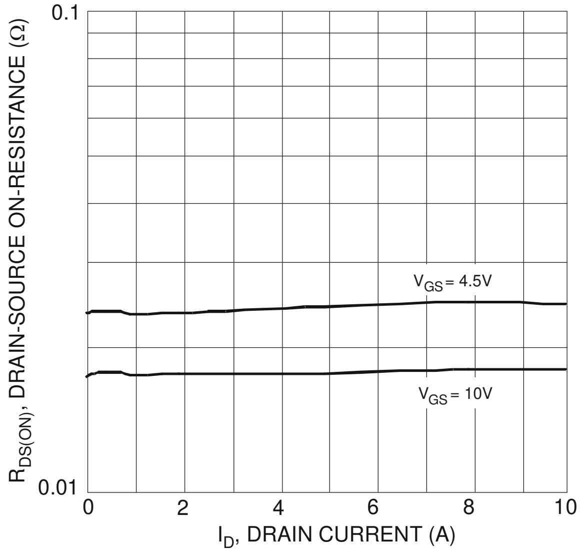

Figure 7 Typical On-Resistance
vs. Drain Current and Gate Voltage

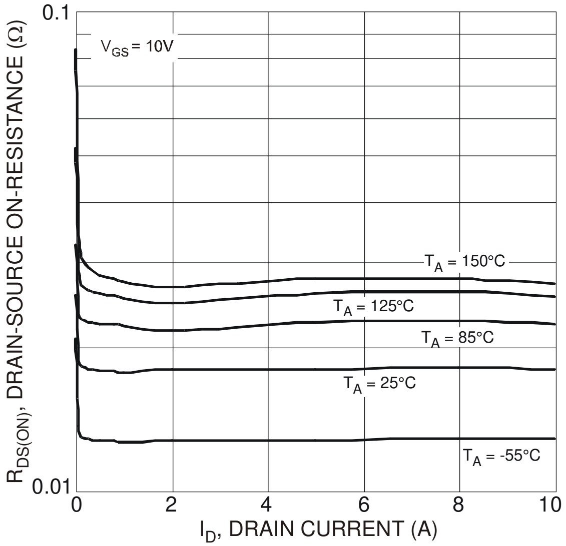

Figure 8 Typical Drain-Source On-Resistance
vs. Drain Current and Temperature

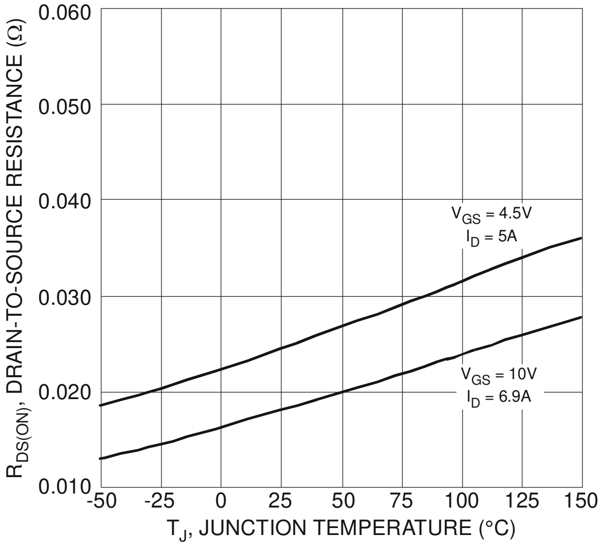

Figure 9 On-Resistance Variation with Temperature

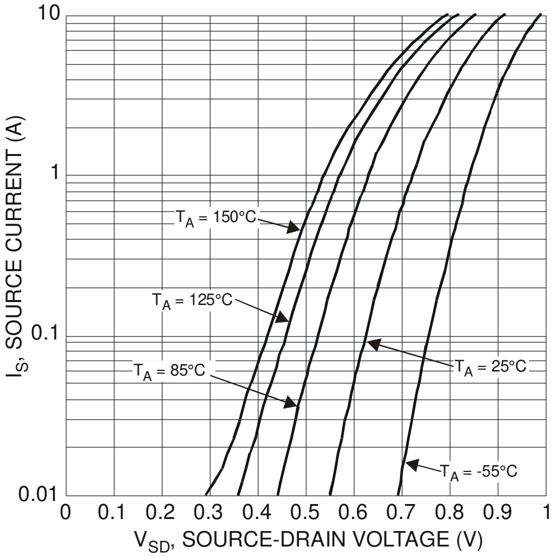

Figure 10 Diode Forward Voltage vs. Current

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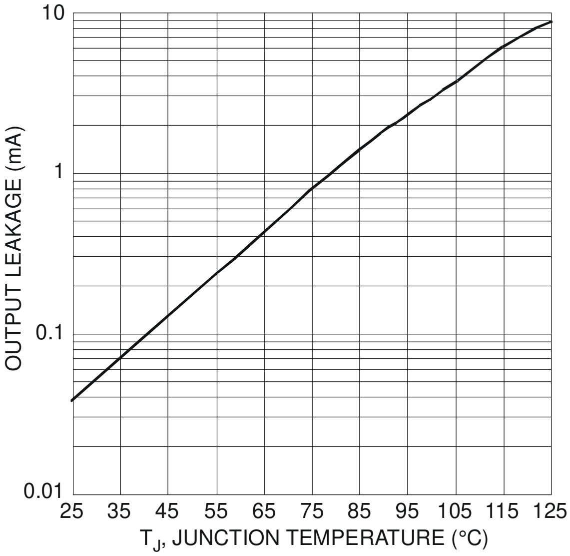

Figure 11 Output Leakage at 5V Bias vs. Junction Temperature

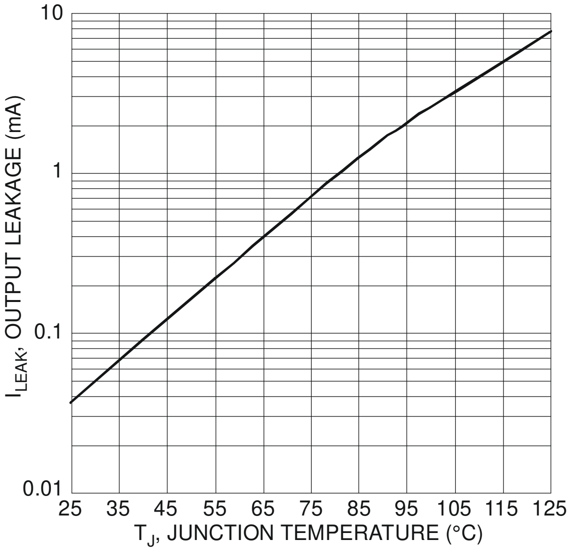

Figure 12 Input Leakage at 16V Bias vs. Junction Temperature

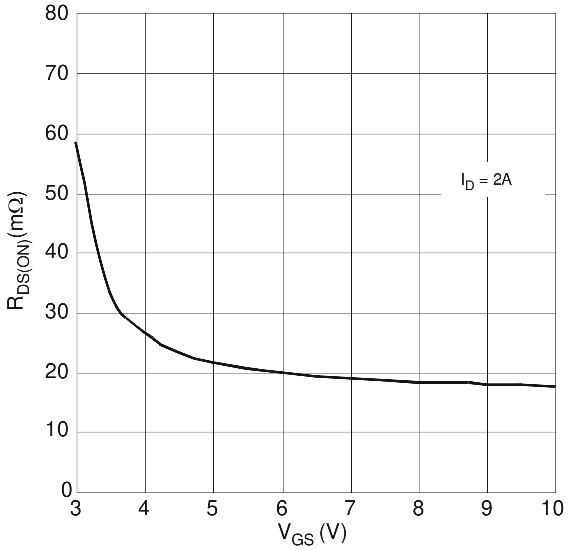

Figure 13 FET Typical On-Resistance vs. Gate-to-Source Voltage (from 3V to 10V)

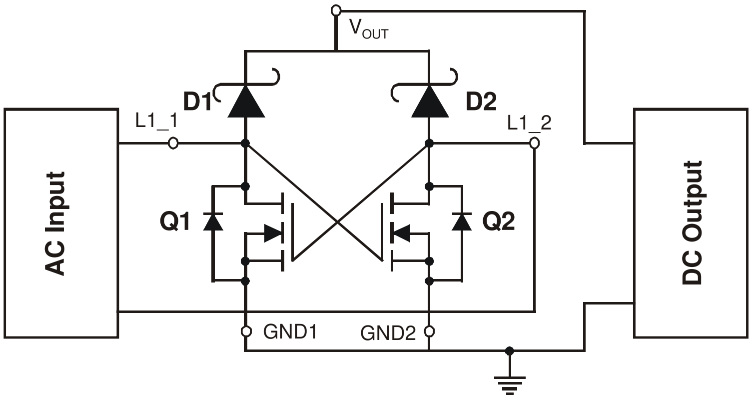

Figure 14 Typical Application Circuit
GND1 and GND2 are not internally connected.
The user should make the connection in the PCB design.

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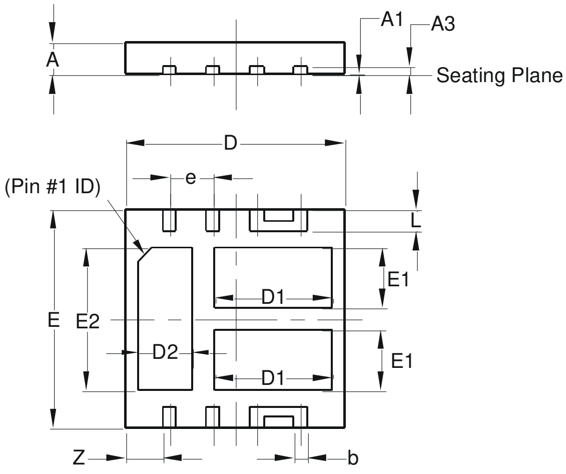
Package Outline Dimensions

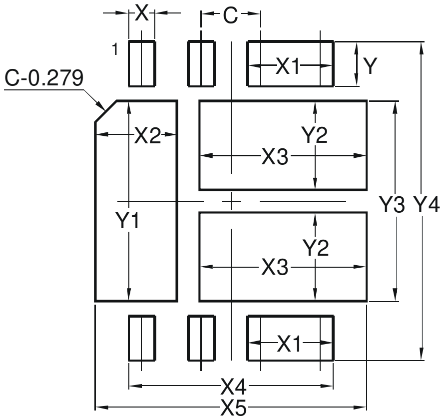
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



U-DFN4040-8			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D1	2.05	2.25	2.15
D2	0.90	1.10	1.00
E	3.95	4.05	4.00
E1	1.00	1.20	1.10
E2	2.50	2.70	2.60
e	-	-	0.80
L	0.35	0.45	0.40
Z	-	-	0.675
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
C	0.800
X	0.350
X1	1.150
X2	1.100
X3	2.250
X4	2.750
X5	3.650
Y	0.600
Y1	2.700
Y2	1.200
Y3	2.700
Y4	4.300

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