# SY88345BL

## 3.3V, 3.2Gbps CML Low-Power Limiting Post Amplifier w/ High-Gain TTL Signal Detect

## General Description

The SY88345BL high-sensitivity limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88345BL quantizes these signals and outputs CML-level waveforms.

The SY88345BL operates from a single +3.3V $\pm$10% power supply, and over temperatures ranging from –40$^{o}$C to +85$^{o}$C. With its wide bandwidth, high gain, and signals with data rates up to 3.2Gbps and as small as 5mV$_{PP}$ can be amplified to drive devices with CML inputs or AC-coupled CML/PECL inputs.

The SY88345BL generates a signal-detect (SD) open-collector TTL output. A programmable signal-detect level-set pin (SD$_{LVL}$) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold sets by SD$_{LVL}$ and de-asserts low otherwise. The enable input (EN) de-asserts the true output signal without removing the input signal. The SD output can be fed back to the EN input to maintain output stability under loss-of-signal condition. Typically, 3.5dB SD hysteresis is provided to prevent chattering.

Datasheet and support documentation can be found on Micrel's web site at: www.micrel.com.

## Features

- Single 3.3V power supply
- 155Mbps to 3.2Gbps operation
- Low-noise CML data outputs
- Chatter-free Open-Collector TTL signal detect (SD) output with internal 4.75kΩ pull-up resistor
- TTL EN input
- Internal 50Ω input termination
- Programmable SD level set (SD$_{LVL}$)
- Ideal for multi-rate applications
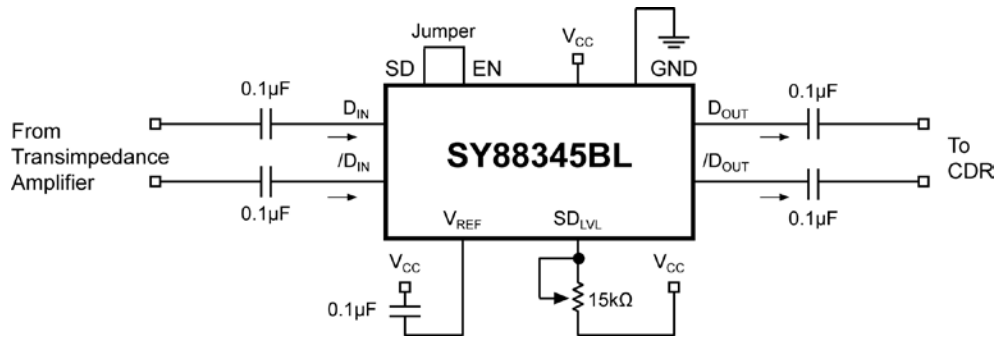- Available in a tiny 10-pin EPAD MSOP and 16-pin QFN package

## Applications

- APON/BPON, EPON, GPON and GEPON
- Gigabit Ethernet
- 1X and 2X Fibre Channel
- SONET/SDH: OC-3/12/24/48–STMD/4/8/16
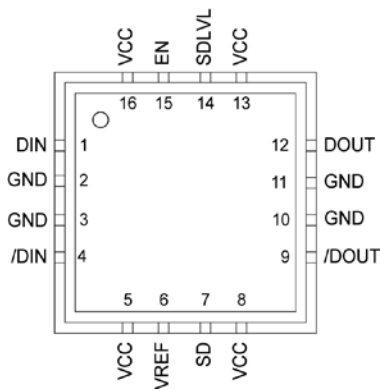- High-gain line driver and line receiver

## Markets

- FTTP/FTTH
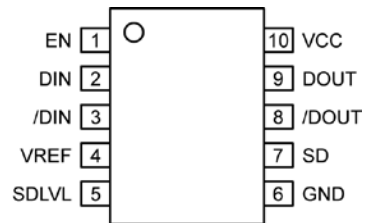- Optical transceivers
- Datacom/Telecom
- Low-gain TIA interface

## Typical Application



## Pin Configuration



**16-Pin QFN**



**10-Pin EPAD-MSOP (K10-2)**

## Ordering Information

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY88345BLEY | K10-2 | Industrial | 345B with Pb-Free bar line indicator | Matte-Sn |
| SY88345BLEYTR[1] | K10-2 | Industrial | 345B with Pb-Free bar line indicator | Matte-Sn |
| SY88345BLMG[2] | QFN-16 | Industrial | 345B with Pb-Free bar line indicator | NiPdAu Pb-Free |
| SY88345BLMGTR[1, 2] | QFN-16 | Industrial | 345B with Pb-Free bar line indicator | NiPdAu Pb-Free |

**Notes:**

1. Tape and Reel.

2. Pb-Free package is recommended for new designs.

## Pin Description

| Pin Number (MSOP) | Pin Number (QFN) | Pin Name | Type | Pin Function |
|---|---|---|---|---|
| 1 | 15 | EN | TTL Input: Default is high. | Enable: De-asserts true data output when LOW. |
| 2 | 1 | DIN | Data Input | True data input w/50Ω termination to $V_{REF}$. |
| 3 | 4 | /DIN | Data Input | Complementary data input w/50Ω termination to $V_{REF}$. |
| 4 | 6 | VREF | | Reference Voltage: Placing a capacitor here to $V_{CC}$ helps stabilize $SD_{LVL}$. |
| 5 | 14 | SDLVL | Input: Default is maximum sensitivity | Signal-detect Level Set: A resistor from this pin to $V_{CC}$ sets the threshold for the data input amplitude at which the SD output will be asserted. |
| 6 Exposed Pad | 2, 3, 10, 11 Exposed Pad | GND | Ground | Device ground. Exposed pad must be connected to PCB ground plane. |
| 7 | 7 | SD | Open Collector TTL Output with Internal 4.75kΩ pull-up Resistor | Signal-detect: Asserts high when the data input amplitude rises above the threshold sets by $SD_{LVL}$. |
| 8 | 9 | /DOUT | CML Output | Complementary data output. |
| 9 | 12 | DOUT | CML Output | True data output. |
| 10 | 5, 8, 13, 16 | VCC | Power supply | Positive power supply. |

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{CC}$) ..................................... 0V to +4.0V
Input Voltage (DIN, /DIN) ................................... 0 to $V_{CC}$
Output Current ($I_{OUT}$) ............................................$\pm$25mA
EN Voltage ......................................................... 0 to $V_{CC}$
$V_{REF}$ Current…………………………….-800uA to +500uA
$SD_{LVL}$ Voltage ............................................... $V_{REF}$ to $V_{CC}$
Lead Temperature (soldering, 20sec.) ..................260°C
Storage Temperature ($T_s$) .....................-65°C to +150°C

## Operating Ratings[2]

Supply Voltage ($V_{CC}$)..................................+3.0V to +3.6V
Ambient Temperature ($T_A$) .......................–40°C to +85°C
Junction Temperature ($T_J$) .....................–40°C to +125°C
Junction Thermal Resistance
  QFN
    ($\theta_{JA}$) Still-air ............................................... 61°C/W
    ($\Psi_{JB}$)............................................................ 38°C/W

  EPAD-MSOP
    ($\theta_{JA}$) Still-air ............................................... 38°C/W
    ($\Psi_{JB}$)............................................................ 22°C/W

## DC Electrical Characteristics

$V_{CC}$ = 3.0V to 3.6V; $R_{LOAD}$ = 50Ω to $V_{CC}$; $T_A$ = –40°C to +85°C.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------|-----------|-----------|-----|-----|-----|-------|
| $I_{CC}$ | Power Supply Current | No output load | | 42 | 65 | mA |
| $SD_{LVL}$ | $SD_{LVL}$ Voltage | | $V_{REF}$ | | $V_{CC}$ | V |
| $V_{OH}$ | CML Output HIGH Voltage | | $V_{CC}$-0.020 | $V_{CC}$-0.005 | $V_{CC}$ | V |
| $V_{OL}$ | CML Output LOW Voltage | $V_{CC}$ = 3.3V | $V_{CC}$-0.475 | $V_{CC}$-0.400 | $V_{CC}$-0.350 | V |
| $V_{OFFSET}$ | Differential Output Offset | | | | $\pm$80 | mV |
| $Z_O$ | Single-Ended Output Impedance | | 40 | 50 | 60 | Ω |
| $Z_I$ | Single-Ended Input Impedance | | 40 | 50 | 60 | Ω |
| $V_{REF}$ | Reference Voltage | | | $V_{CC}$-1.28 | | V |

## TTL DC Electrical Characteristics

$V_{CC}$ = 3.0V to 3.6V; $R_{LOAD}$ = 50Ω to $V_{CC}$; $T_A$ = –40°C to +85°C.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------|-----------|-----------|-----|-----|-----|-------|
| $V_{IH}$ | EN Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | EN Input LOW Voltage | | | | 0.8 | V |
| $I_{IH}$ | EN Input HIGH Current | $V_{IN}$ = 2.7V | | | 20 | µA |
| | | $V_{IN}$ = $V_{CC}$ | | | 100 | µA |
| $I_{IL}$ | EN Input LOW Current | $V_{IN}$ = 0.5V | -300 | | | µA |
| $V_{OH}$ | SD Output HIGH Level | $V_{CC}$ ≥ 3.3V, $I_{OH}$ (max) < 160µA | 2.4 | | | V |
| | | $V_{CC}$ < 3.3V, $I_{OH}$ (max) < 160µA | 2.0 | | | V |
| $V_{OL}$ | SD Output LOW Level | Sinking 2mA | | | 0.5 | V |

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. $\Psi_{JB}$ uses 4-layer ($\theta_{JA}$) in still-air-number, unless otherwise stated.

## AC Electrical Characteristics

$V_{CC}$ = 3.0V to 3.6V; $R_{LOAD}$ = 50Ω to $V_{CC}$; $T_A$ = −40°C to +85°C.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time (20% to 80%) | Note 4 | | 60 | 120 | ps |
| $t_{JITTER}$ | Deterministic | Note 5 | | 15 | | $ps_{PP}$ |
| | Random | Note 6 | | 5 | | $ps_{RMS}$ |
| $V_{ID}$ | Differential Input Voltage Swing | Figure 1 | 5 | | 1800 | $mV_{PP}$ |
| $V_{OD}$ | Differential Output Voltage Swing | $V_{ID} \geq 10mV_{PP}$  Figure 1 | 700 | 800 | 950 | $mV_{PP}$ |
| $T_{OFF}$ | SD De-assert Time | | | 2 | 10 | µs |
| $T_{ON}$ | SD Assert Time | | | 2 | 10 | µs |
| $SD_{AL}$ | Low SD Assert Level | $R_{SDLVL}$ = 15kΩ, Note 8 | | 4.5 | | $mV_{PP}$ |
| $SD_{DL}$ | Low SD De-assert Level | $R_{SDLVL}$ = 15kΩ, Note 8 | | 3.0 | | $mV_{PP}$ |
| $HYS_L$ | Low SD Hysteresis | $R_{SDLVL}$ = 15kΩ, Note 7 | | 3.5 | | dB |
| $SD_{AM}$ | Medium SD Assert Level | $R_{SDLVL}$ = 5kΩ, Note 8 | | 7.5 | 11 | $mV_{PP}$ |
| $SD_{DM}$ | Medium SD De-assert Level | $R_{SDLVL}$ = 5kΩ, Note 8 | 2 | 5.0 | | $mV_{PP}$ |
| $HYS_M$ | Medium SD Hysteresis | $R_{SDLVL}$ = 5kΩ, Note 7 | 2 | 3.5 | 4.5 | dB |
| $SD_{AH}$ | High SD Assert Level | $R_{SDLVL}$ = 100Ω, Note 8 | | 18 | 23 | $mV_{PP}$ |
| $SD_{DH}$ | High SD De-assert Level | $R_{SDLVL}$ = 100Ω, Note 8 | 8 | 12 | | $mV_{PP}$ |
| $HYS_H$ | High SD Hysteresis | $R_{SDLVL}$ = 100Ω, Note 7 | 2 | 3.5 | 4.5 | dB |
| $B_{-3dB}$ | 3dB Bandwidth | | | 2 | | GHz |
| $A_{V(Diff)}$ | Differential Voltage Gain | | 32 | 38 | | dB |
| $S_{21}$ | Single-ended Small-Signal Gain | | 26 | 32 | | dB |

**Notes:**

4. Amplifier in limiting mode. Input is a 200MHz square wave.

5. Deterministic jitter measured using 3.2Gbps K28.5 pattern, $V_{ID}$ = 10m$V_{PP}$.

6. Random jitter measured using 3.2Gbps K28.7 pattern, $V_{ID}$ = 10m$V_{PP}$.

7. This specification defines electrical hysteresis as 20log (SD Assert/SD De-assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2, depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-4.5dB, as shown in the AC characteristics table, will be 1dB-3dB.

8. See "Typical Operating Characteristics" for a graph showing how to choose a particular $R_{SDLVL}$ for a particular SD assert and its associated de-assert amplitude.

# Typical Characteristics



$V_{ID}$ to Assert/De-Assert SD vs. $R_{SDLVL}$



Hysteresis vs. $R_{SDLVL}$
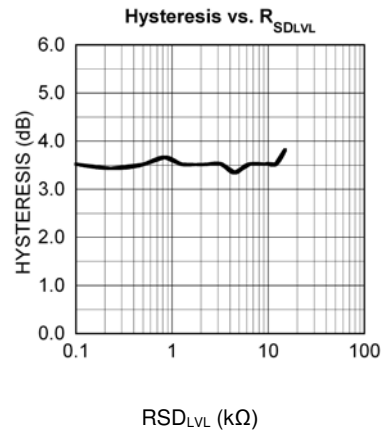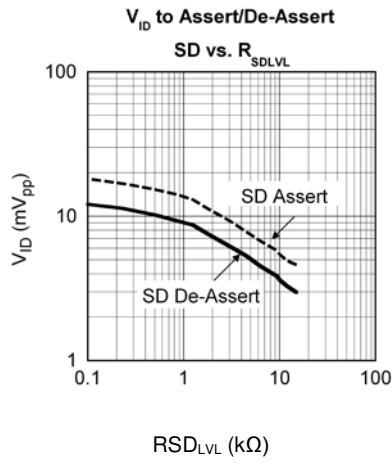
## Functional Diagram
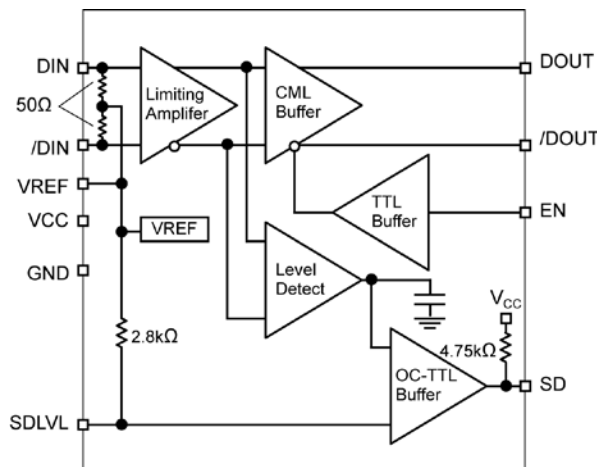


## Detailed Description

The SY88345BL low-power, high-sensitivity limiting post amplifier operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 3.2Gbps and as small as 5mV$_{PP}$ can be amplified. Figure 1 shows the allowed input voltage swing. The SY88345BL generates an SD output. SD$_{LVL}$ sets the sensitivity of the input amplitude detection.

### Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the SY88345BL's input stage. The high-sensitivity of the input amplifier allows signals as small as 5mV$_{PP}$ to be detected and amplified. The input amplifier also allows input signals as large as 1800mV$_{PP}$. Input signals are linearly amplified with a typical 38dB differential voltage gain. Since it is a limiting amplifier, the SY88345BL typically outputs 800mV$_{PP}$ voltage-limited waveforms for input signals that are greater than 12mV$_{PP}$. Applications requiring the SY88345BL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88345BL's input pins to ensure the best performance of the device.

### Output Buffer

The SY88345BL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V$_{CC}$ for each output pin provides this. Figure 3 shows a simplified schematic of the output stage.

### Signal-Detect

The SY88345BL generates a chatter-free SD open-collector TTL output with an internal 4.75k pull-up resistor, as shown in Figure 4. SD is used to determine that the input amplitude is large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold sets by SD$_{LVL}$ and de-asserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss-of-signal condition. EN de-asserts the true output signal without removing the input signals. Typically, 3.5dB SD hysteresis is provided to prevent chattering.

### Signal-Detect Level Set

A programmable SD level-set pin (SD$_{LVL}$) sets the threshold of the input amplitude detection. Connecting an external resistor between V$_{CC}$ and SD$_{LVL}$ sets the voltage at SD$_{LVL}$. This voltage ranges from V$_{CC}$ to V$_{REF}$. The external resistor creates a voltage divider between V$_{CC}$ and V$_{REF,}$ as shown in Figure 5.

### Hysteresis

The SY88345BL typically provides 3.5dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as $V^2_{IN}/R$ for an electrical signal. Hence, the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power. Therefore, the ratios change linearly. Thus, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. Since the SY88345BL is an electrical device, this data sheet refers to hysteresis in electrical terms. With 3.5dB SD hysteresis, a voltage factor of 1.5 is required to assert or de-assert SD.
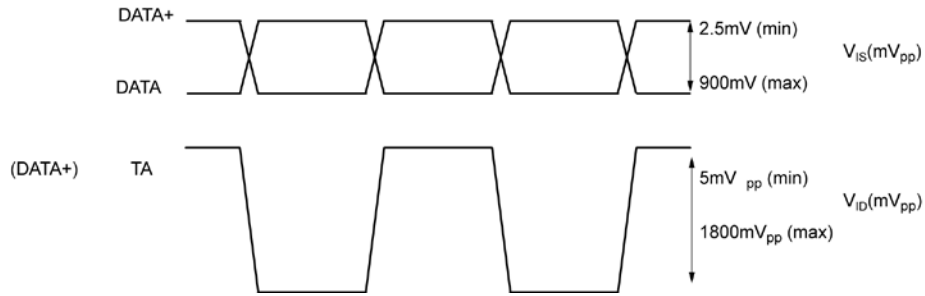
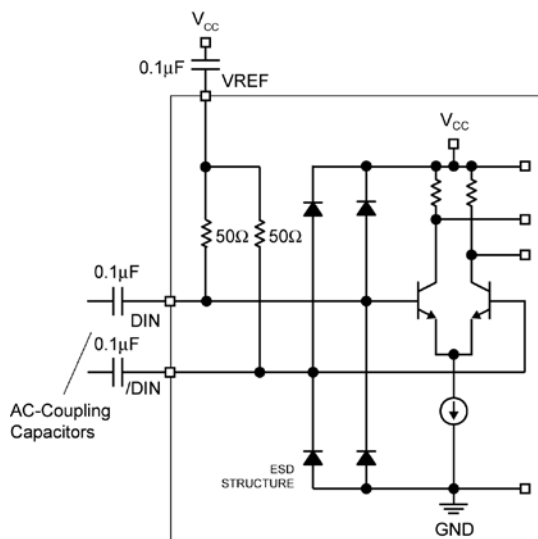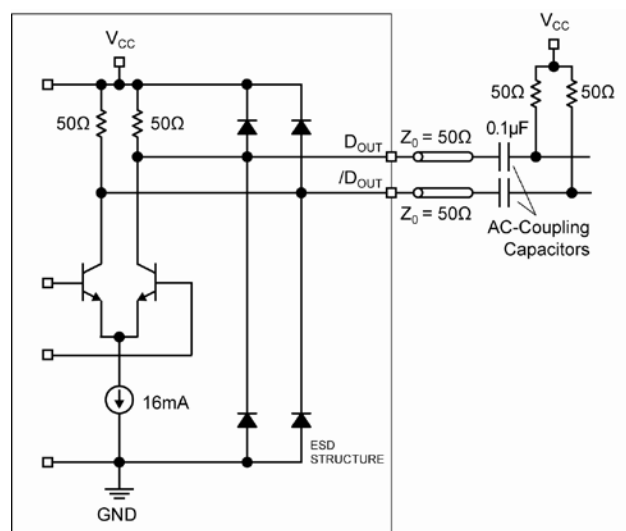Figure 1. $V_{IS}$ and $V_{ID}$ Definition



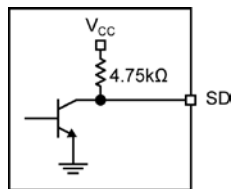Figure 2. Input Structure



Figure 3. Output Structure



Figure 4. SD Output Structure

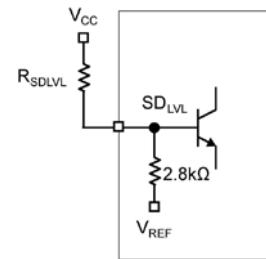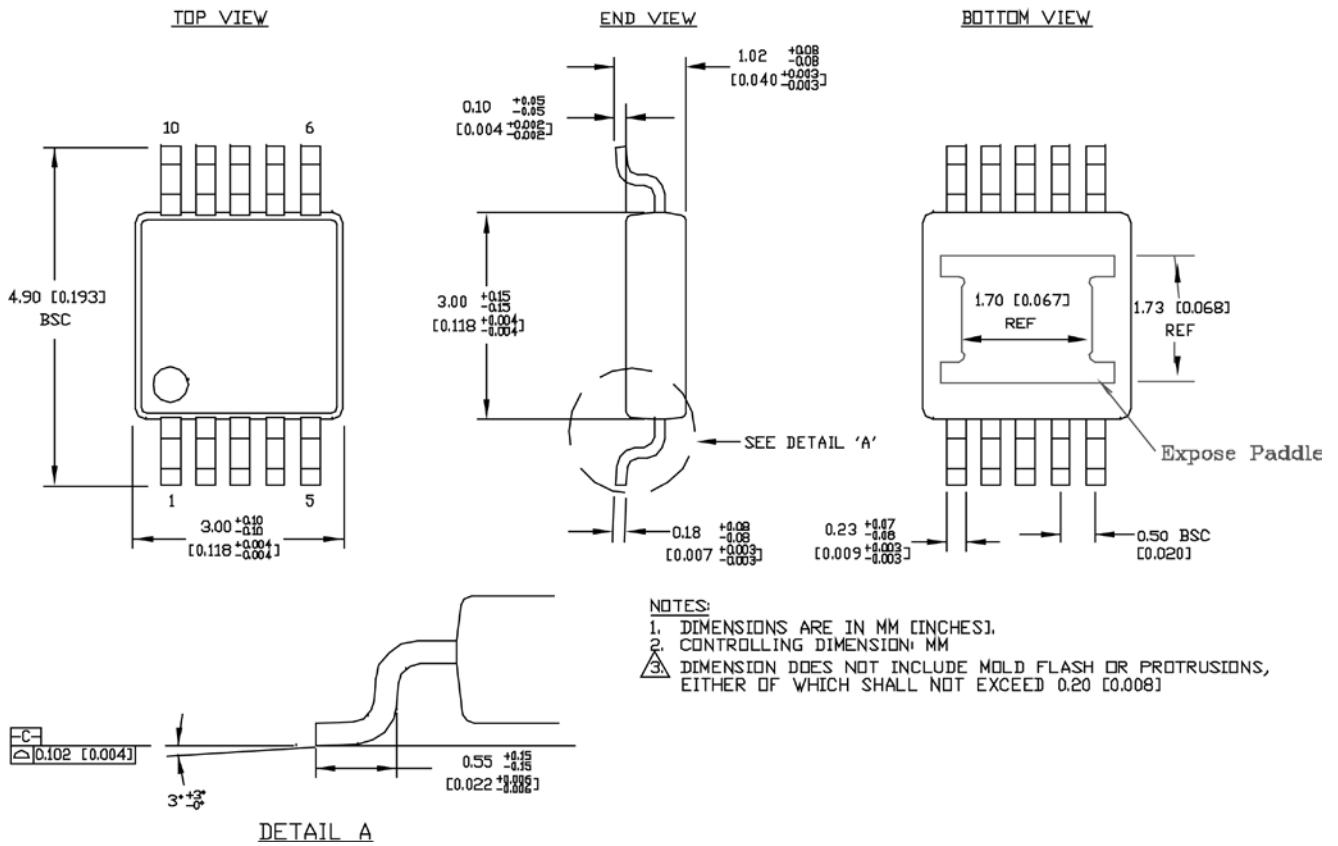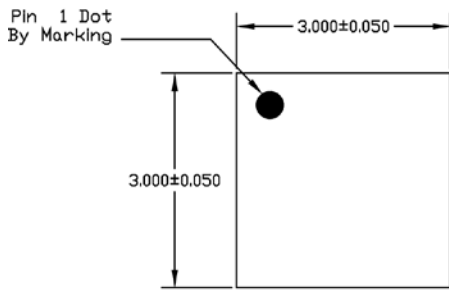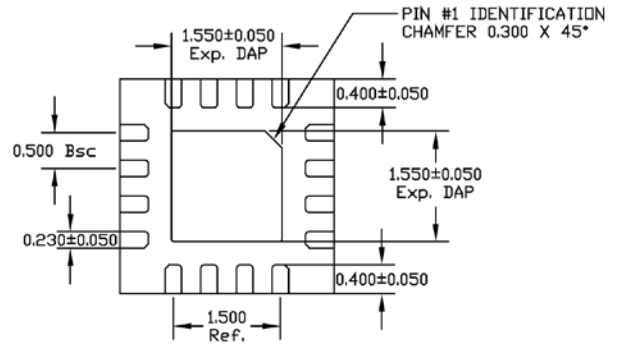
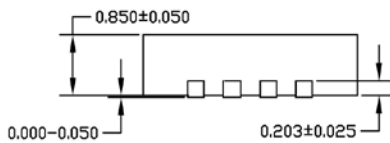
Figure 5. $SD_{LVL}$ Setting Circuit

## Package Information



**10-Pin EPAD-MSOP (K10-2)**

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

**16-Pin QFN**