



Seven Band Graphic Equalizer Data Sheet

MSGEQ7

Description

The seven band graphic equalizer IC is a CMOS chip that divides the audio spectrum into seven bands, 63Hz, 160Hz, 400Hz, 1kHz, 2.5kHz, 6.25kHz and 16kHz. The seven frequencies are peak detected and multiplexed to the output to provide a DC representation of the amplitude of each band. No external components are needed to select the filter responses. Only an off chip resistor and capacitor are needed to select the on chip clock oscillator frequency. The filter center frequencies track this frequency.

Other than coupling and decoupling capacitors, no other external components are needed. The chip supply can be between 2.7 and 5.5 volts with 5 volts providing the best performance. The device has very low quiescent current (less than 1mA typical) for portable audio devices. The multiplexor is controlled by a reset and a strobe, permitting multiplexor readout with only two pins. The multiplexor readout rate also controls the decay time (10% decay per read), so no external pins are needed for this function.

Features

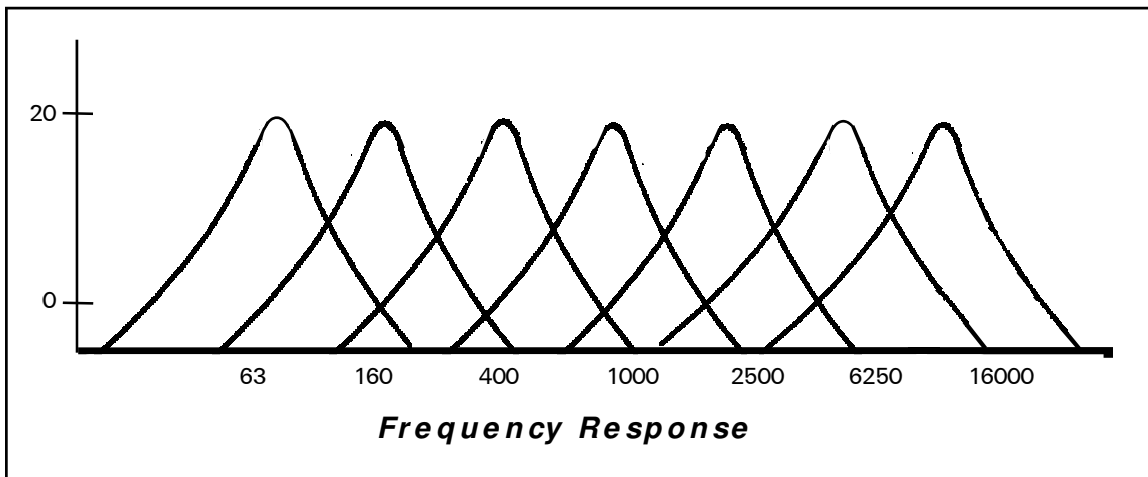
- Low Power Consumption
- Only Two External Components
- On Chip Ground Reference
- Switched - Capacitor Filters
- 3.3 or 5 volt Operation
- 20 dB of Gain Typical
- On Chip Oscillator
- Output Multiplexor
- Variable Decay Time
- 8 Pin Package

Applications

- Portable Stereos
- Car Stereos
- Hi-Fi Stereos
- Spectrum Analyzers

Absolute Maximum Ratings

Power Supply Voltage	+6V
Storage Temperature	-60 to + 150 C
Operating Temperature	0 to 70 C



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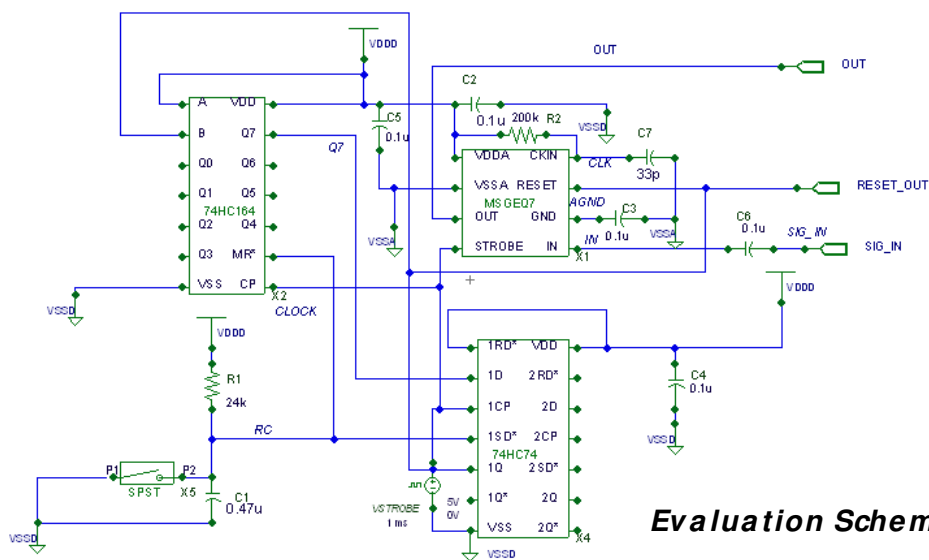
Electrical Characteristics

(VDD = +5.0V, T = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		2.7	5.0	5.5	V
Supply Current	IDD	1 Mohm Load on Output	0.5	0.8	1.0	mA
Output Drive	IO		1			mA
Output Impedance	ZO		700			ohms
Output Offset	VOS		600			mV
Band Offset Difference		Same device	200			mV
AC Specifications						
Gain	AV	Peak input to DC output, Vin = 100 mVpp, fin = 1 kHz	20	22	24	dB
Filter Q	Q		5.5	6.0	6.5	
Output Swing		Vin = 0.3Vpp, fin = 1 kHz	3.5	4		V
Clock Frequency	FCLK	C = 33 pF*, R = 200 kohms	145	165	180	kHz
Input Impedance	ZIN		1			Mohm

* includes stray capacitance

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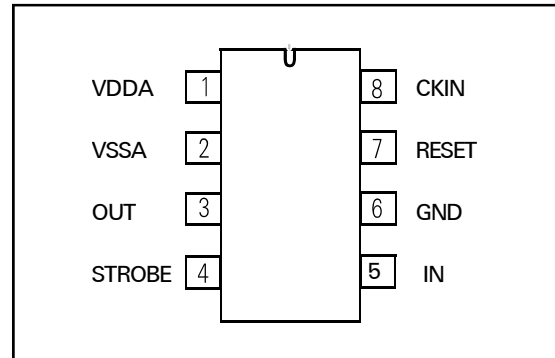
Evaluation Schematic

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Pin Description

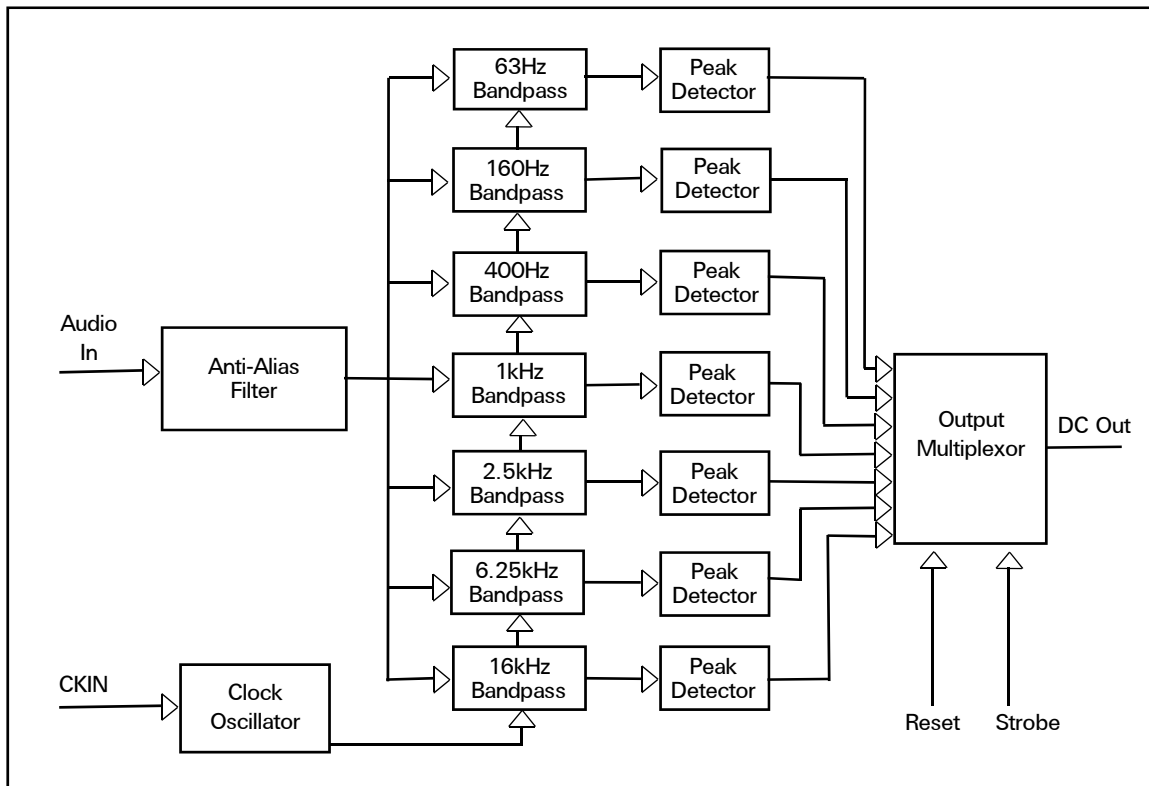
- | | |
|-----------|--|
| 1. VDD | Positive Power Supply
Typically 5 Volts |
| 2. VSS | Negative Power Supply
Typically 0 Volts |
| 3. OUT | Multiplexed DC Output |
| 4. STROBE | Channel Selection Pin |
| 5. IN | Audio Input |
| 6. GND | Internally Generated Ground
Reference. Typically 2.5V |
| 7. RESET | Resets Multiplexor |
| 8. CKIN | Clock Oscillator Pin |

Pin Configuration



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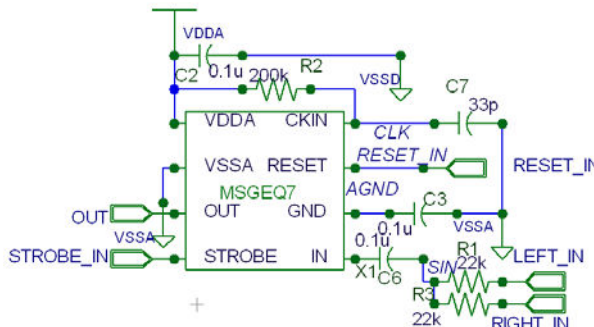
Block Diagram



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Multiplexor Operation ————— Typical Application

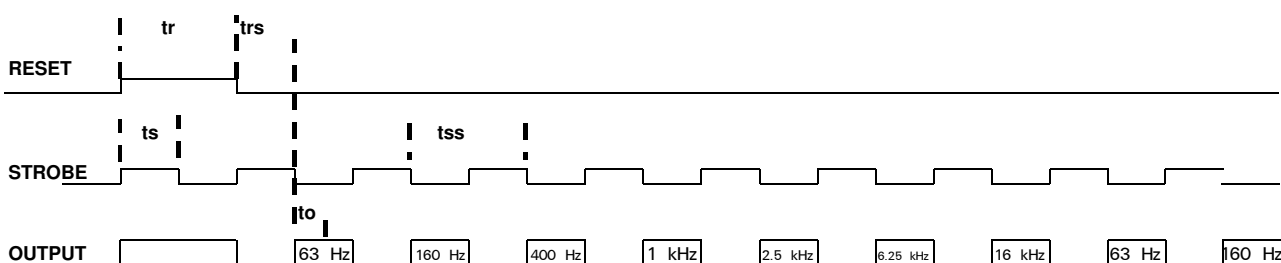
The DC peak output for measurement is selected using the reset and strobe pins. Reset high resets the multiplexor. Reset low enables the strobe pin. After the first strobe leading edge, 63Hz output is on OUT. Each additional strobe leading edge advances the multiplexor one channel (63Hz, 160Hz, 400Hz, 1kHz, 2.5kHz, 6.25kHz, 16kHz etc.) and this will repeat indefinitely. The multiplexor read rate is also the output decay time control. Each read decays that channel approximately 10%. The strobe timing is shown below:



Ordering Information

Part Number	Package	Operating Temperature
MSGEQ7N	8 Pin 150 mils SOIC	0-70 °C
MSGEQ7P	8 Pin 300 mils PDIP	0-70 °C

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tr - Reset Pulse Width		100 nS min
trs - Reset to Strobe	Delay	72 uS min
ts - Strobe Pulse Width		18 uS min
tss - Strobe to Strobe	Delay	72 uS min
to - Output Settling Time		36 uS min (with Cload = 22 pF and Rload = 1 Mohm)

Strobe Timing Diagram



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