

## FEATURES

- 1-of-4 Bidirectional Translating Switches
- I<sup>2</sup>C Bus and SMBus Compatible
- Active-Low Reset Input
- Three Address Pins, Allowing up to Eight Devices on the I<sup>2</sup>C Bus
- Channel Selection Via I<sup>2</sup>C Bus
- Power Up With All Switch Channels Deselected
- Low R<sub>ON</sub> Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5.5-V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA Per JESD 78
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

The PCA9546A is a quad bidirectional translating switch controlled via the I<sup>2</sup>C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active-low reset ( $\overline{\text{RESET}}$ ) input allows the PCA9546A to recover from a situation in which one of the downstream I<sup>2</sup>C buses is stuck in a low state. Pulling  $\overline{\text{RESET}}$  low resets the I<sup>2</sup>C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	QFN – RGV	Reel of 2500	PCA9546ARGVR	PD546A	
	QFN – RGY	Reel of 1000	PCA9546ARGYR	PD546A	
	SOIC – D	Tube of 40		PCA9546AD	PCA9546A
				PCA9546ADG4	
		Reel of 2500		PCA9546ADR	
				PCA9546ADRG4	
	SOIC – DW	Tube of 40		PCA9546ADW	PCA9546A
				PCA9546ADWR	
		Reel of 250		PCA9546ADWT	PREVIEW
	TSSOP – PW	Tube of 90		PCA9546APW	PD546A
				PCA9546APWE4	
		Reel of 2000		PCA9546APWR	
				PCA9546APWRE4	
	Reel of 250		PCA9546APWT		
			PCA9546APWTE4		
TVSOP – DGV	Reel of 2000		PCA9546ADGVR	PD546A	
	Reel of 250		PCA9546ADGVT	PREVIEW	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



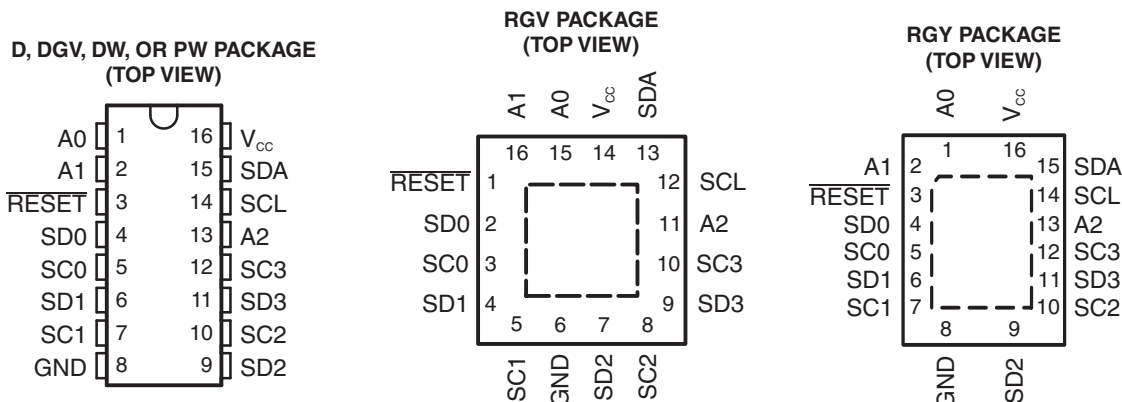
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# PCA9546A 4-CHANNEL I<sup>2</sup>C AND SMBus SWITCH WITH RESET FUNCTION

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## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

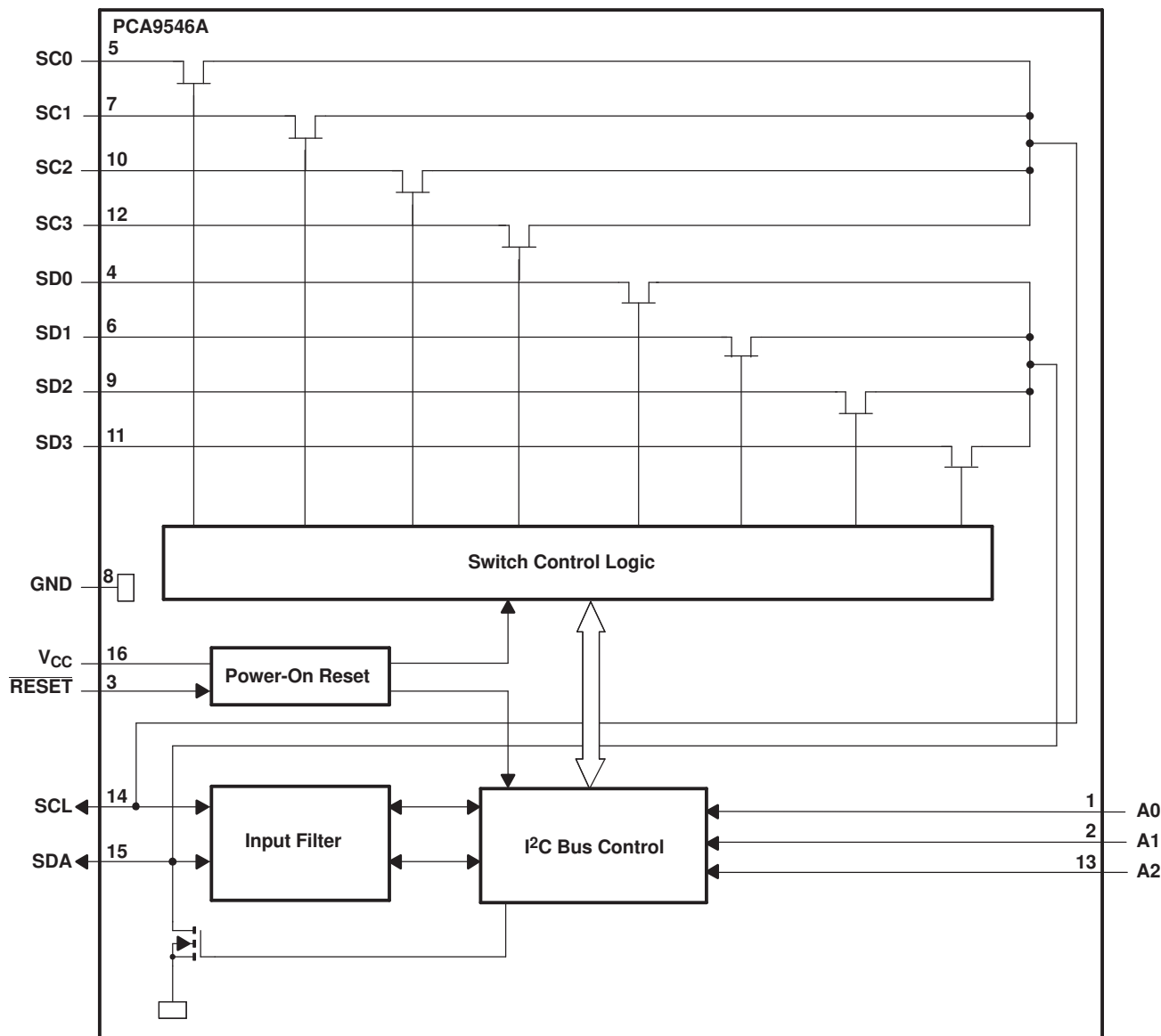
The pass gates of the switches are constructed such that the V<sub>CC</sub> pin can be used to limit the maximum high voltage, which will be passed by the PCA9546A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts without any additional protection. External pullup resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5-V tolerant.



## TERMINAL FUNCTIONS

NO.		NAME	DESCRIPTION
D, DGV, DW, PW, AND RGY	RGV		
1	15	A0	Address input 0. Connect directly to V <sub>CC</sub> or ground.
2	16	A1	Address input 1. Connect directly to V <sub>CC</sub> or ground.
3	1	RESET	Active low reset input. Connect to V <sub>CC</sub> through a pullup resistor, if not used.
4	2	SD0	Serial data 0. Connect to V <sub>CC</sub> through a pullup resistor.
5	3	SC0	Serial clock 0. Connect to V <sub>CC</sub> through a pullup resistor.
6	4	SD1	Serial data 1. Connect to V <sub>CC</sub> through a pullup resistor.
7	5	SC1	Serial clock 1. Connect to V <sub>CC</sub> through a pullup resistor.
8	6	GND	Ground
9	7	SD2	Serial data 2. Connect to V <sub>CC</sub> through a pullup resistor.
10	8	SC2	Serial clock 2. Connect to V <sub>CC</sub> through a pullup resistor.
11	9	SD3	Serial data 3. Connect to V <sub>CC</sub> through a pullup resistor.
12	10	SC3	Serial clock 3. Connect to V <sub>CC</sub> through a pullup resistor.
13	11	A2	Address input 2. Connect directly to V <sub>CC</sub> or ground.
14	12	SCL	Serial clock line. Connect to V <sub>CC</sub> through a pullup resistor.
15	13	SDA	Serial data line. Connect to V <sub>CC</sub> through a pullup resistor.
16	14	V <sub>CC</sub>	Supply power

**BLOCK DIAGRAM**



A. Pin numbers shown are for the D, DGV, DW, PW and RGY packages.

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## Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9546A is shown in Figure 1. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low.

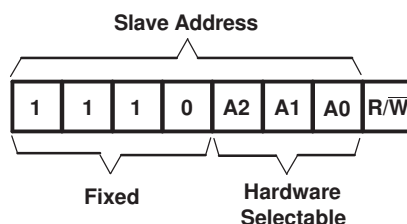


Figure 1. PCA9546A Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

## Control Register

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9546A, which is stored in the control register (see Figure 2). If multiple bytes are received by the PCA9546A, it will save the last byte received. This register can be written and read via the I<sup>2</sup>C bus.

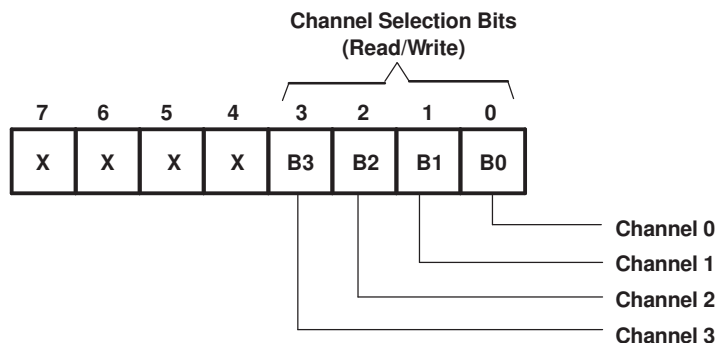


Figure 2. Control Register

## Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). This register is written after the PCA9546A has been addressed. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I<sup>2</sup>C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)<sup>(1)</sup>

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
								1
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

(1) Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 and 2 are enabled. Care should be taken not to exceed the maximum bus capacity.

## RESET Input

The  $\overline{\text{RESET}}$  input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of  $t_{\text{WL}}$ , the PCA9446A resets its registers and I<sup>2</sup>C state machine and deselects all channels. The  $\overline{\text{RESET}}$  input must be connected to  $V_{\text{CC}}$  through a pullup resistor.

## Power-On Reset

When power is applied to  $V_{\text{CC}}$ , an internal power-on reset holds the PCA9546A in a reset condition until  $V_{\text{CC}}$  has reached  $V_{\text{POR}}$ . At this point, the reset condition is released, and the PCA9546A registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter,  $V_{\text{CC}}$  must be lowered below 0.2 V to reset the device.

## Voltage Translation

The pass-gate transistors of the PCA9546A are constructed such that the  $V_{\text{CC}}$  voltage can be used to limit the maximum voltage that will be passed from one I<sup>2</sup>C bus to another.

Figure 3 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using the data specified in the electrical characteristics section of this data sheet). In order for the PCA9546A to act as a voltage translator, the  $V_{\text{pass}}$  voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V, and the downstream buses are 3.3 V and 2.7 V, then  $V_{\text{pass}}$  must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 3,  $V_{\text{pass}}(\text{max})$  is at 2.7 V when the PCA9546A supply voltage is 3.5 V or lower, so the PCA9546A supply voltage could be set to 3.3 V. Pullup resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 12).

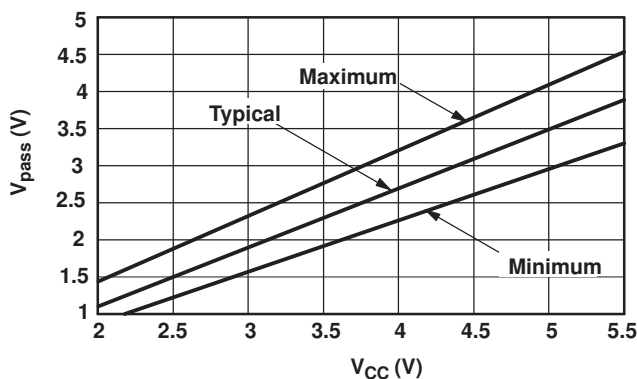


Figure 3.  $V_{\text{pass}}$  Voltage vs  $V_{\text{CC}}$

# PCA9546A 4-CHANNEL I<sup>2</sup>C AND SMBus SWITCH WITH RESET FUNCTION

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## I<sup>2</sup>C Interface

The I<sup>2</sup>C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 4).

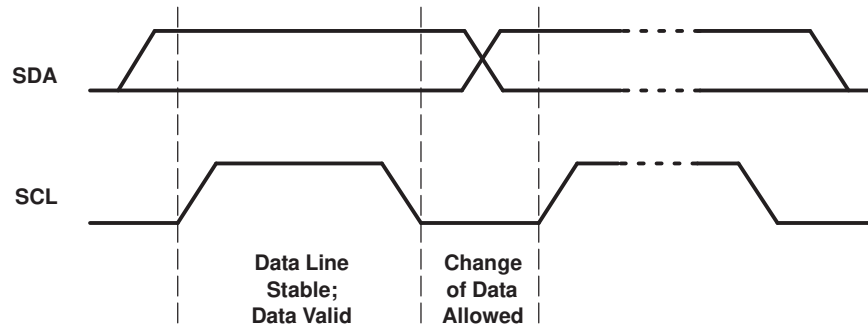


Figure 4. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 5).

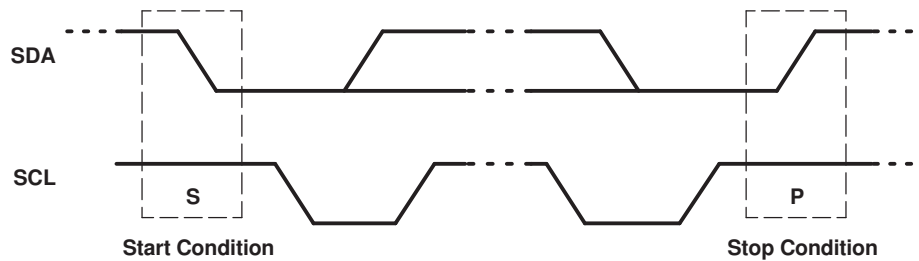


Figure 5. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 6).

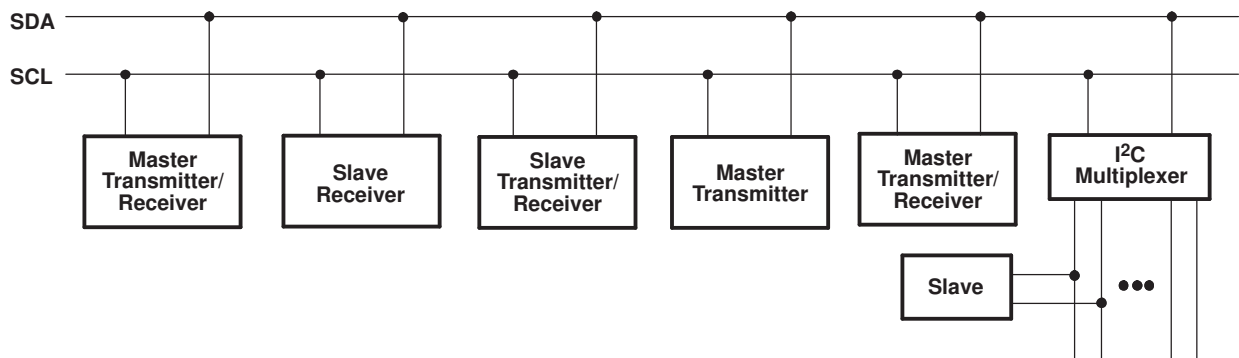


Figure 6. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). Setup and hold times must be taken into account.

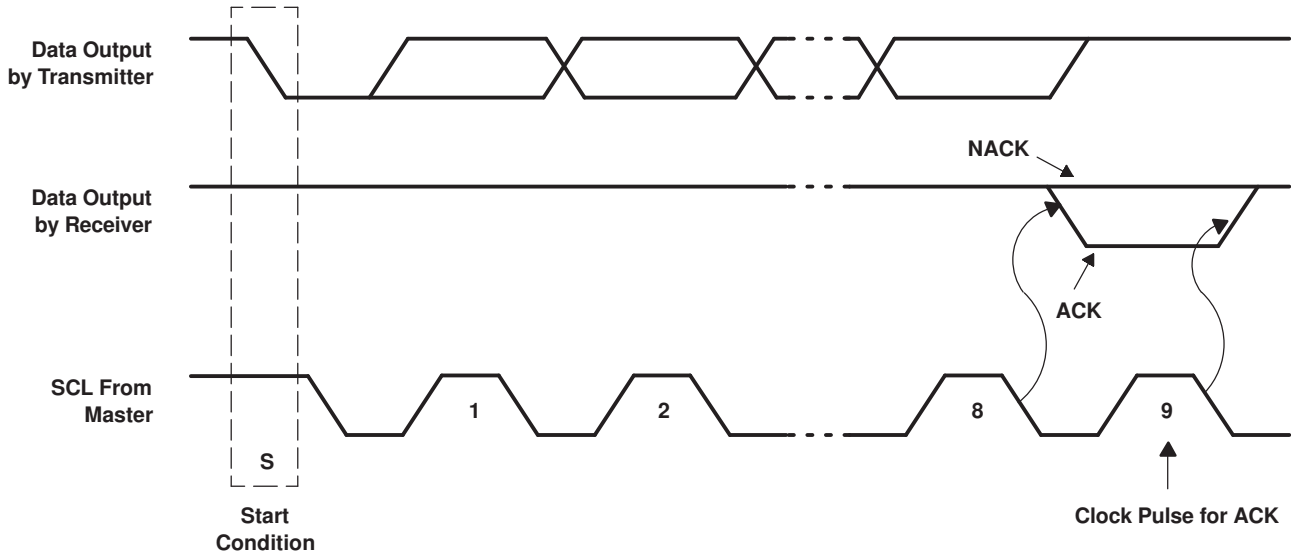


Figure 7. Acknowledgment on the I<sup>2</sup>C Bus

Data is transmitted to the PCA9546A control register using the write mode shown in Figure 8.

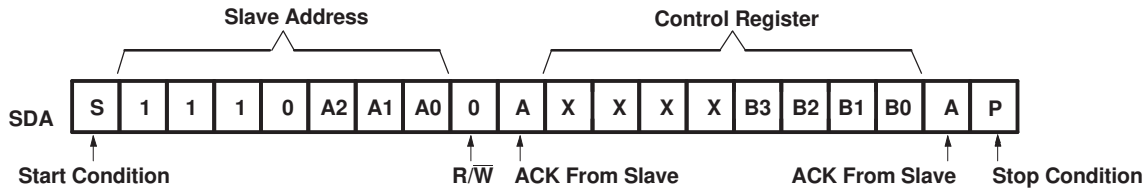


Figure 8. Write Control Register

Data is read from the PCA9546A control register using the read mode shown in Figure 9.

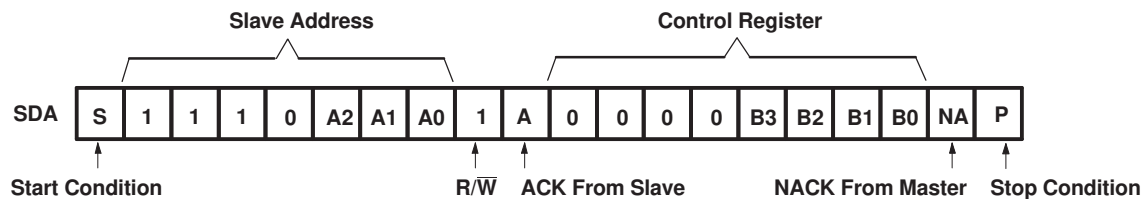


Figure 9. Read Control Register

# PCA9546A

## 4-CHANNEL I<sup>2</sup>C AND SMBus SWITCH WITH RESET FUNCTION

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### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5	7	V
I <sub>I</sub>	Input current		±20	mA
I <sub>O</sub>	Output current		±25	mA
	Continuous current through V <sub>CC</sub>		±100	mA
	Continuous current through GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	D package	73	°C/W
		DGV package	120	
		DW package	57	
		PW package	108	
		RGV package	51.38	
		RGY package	50	
P <sub>tot</sub>	Total power dissipation		400	mW
T <sub>stg</sub>	Storage temperature range	–65	150	°C
T <sub>A</sub>	Operating free-air temperature range	–40	85	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	6
		A2–A0, $\overline{\text{RESET}}$	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	–0.5	0.3 × V <sub>CC</sub>
		A2–A0, $\overline{\text{RESET}}$	–0.5	0.3 × V <sub>CC</sub>
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>POR</sub>	Power-on reset voltage <sup>(2)</sup>	No load,	V <sub>I</sub> = V <sub>CC</sub> or GND	V <sub>POR</sub>	1.6	2.1		V
V <sub>pass</sub>	Switch output voltage	V <sub>SWin</sub> = V <sub>CC</sub> ,	I <sub>SWout</sub> = -100 μA	5 V	3.6			V
				4.5 V to 5.5 V	2.6	4.5		
				3.3 V	1.9			
				3 V to 3.6 V	1.6	2.8		
				2.5 V	1.5			
				2.3 V to 2.7 V	1.1	2		
I <sub>OL</sub>	SCL, SDA	V <sub>OL</sub> = 0.4 V	V <sub>OL</sub> = 0.6 V	2.3 V to 5.5 V	3	7		mA
					6	10		
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V				±1	μA
	SC3–SC0, SD3–SD0						±1	
	A2–A0						±1	
	RESET						±1	
I <sub>CC</sub>	Operating mode	f <sub>SCL</sub> = 100 kHz	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	3	12	μA	
				3.6 V	3	11		
				2.7 V	3	10		
	Standby mode	Low inputs	V <sub>I</sub> = GND, I <sub>O</sub> = 0	5.5 V	0.3	1		
				3.6 V	0.1	1		
		High inputs	V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0	2.7 V	0.1	1		
				5.5 V	0.3	1		
				3.6 V	0.1	1		
2.7 V	0.1	1						
ΔI <sub>CC</sub>	Supply-current change	SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V <sub>CC</sub> or GND		8	15	μA	
			SCL or SDA input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.3 V to 5.5 V	8	15		
C <sub>I</sub>	A2–A0	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V		4.5	6	pF	
	RESET				4.5	5.5		
C <sub>IO(OFF)</sub> <sup>(3)</sup>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND, Switch OFF	2.3 V to 5.5 V		15	19	pF	
	SC3–SC0, SD3–SD0				6	8		
R <sub>ON</sub>	Switch on-state resistance	V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 15 mA	4.5 V to 5.5 V	4	9	16	Ω	
			3 V to 3.6 V	5	11	20		
		V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 10 mA	2.3 V to 2.7 V	7	16	45		

 (1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V<sub>CC</sub>), T<sub>A</sub> = 25°C.

 (2) The power-on reset circuit resets the I<sup>2</sup>C bus logic with V<sub>CC</sub> < V<sub>POR</sub>. V<sub>CC</sub> must be lowered to 0.2 V to reset the device.

 (3) C<sub>IO(ON)</sub> depends on internal capacitance and external capacitance added to the SC<sub>n</sub> lines when channels(s) are ON.

# PCA9546A

## 4-CHANNEL I<sup>2</sup>C AND SMBus SWITCH WITH RESET FUNCTION

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### I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 10)

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
t <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	250		100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0 <sup>(1)</sup>		0 <sup>(1)</sup>		μs
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1000	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time		300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time		300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start	4.7		1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	4.7		0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	4		0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup	4		0.6		μs
t <sub>vdL(Data)</sub>	Valid-data time (high to low) <sup>(3)</sup>	SCL low to SDA output low valid		1	1	μs
t <sub>vdH(Data)</sub>	Valid-data time (low to high) <sup>(3)</sup>	SCL low to SDA output high valid		0.6	0.6	μs
t <sub>vd(ack)</sub>	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1	1	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400		400	pF

- (1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH</sub> min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.  
(2) C<sub>b</sub> = total bus capacitance of one bus line in pF  
(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see Figure 10)

### Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see Figure 10)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pd</sub> <sup>(1)</sup>	Propagation delay time	R <sub>ON</sub> = 20 Ω, C <sub>L</sub> = 15 pF	SDA or SCL	SDn or SCn	0.3	ns
		R <sub>ON</sub> = 20 Ω, C <sub>L</sub> = 50 pF			1	

- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

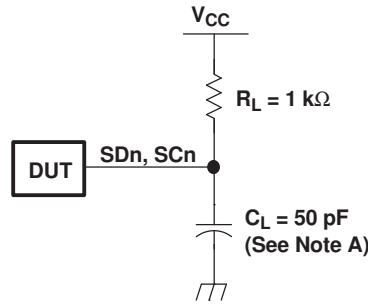
### Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

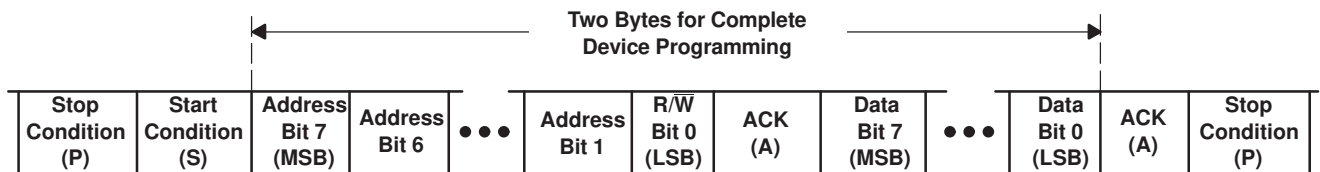
PARAMETER		MIN	MAX	UNIT
t <sub>wL</sub>	Pulse duration, $\overline{\text{RESET}}$ low	6		ns
t <sub>rst</sub> <sup>(1)</sup>	$\overline{\text{RESET}}$ time (SDA clear)		500	ns
t <sub>REC(STA)</sub>	Recovery time from $\overline{\text{RESET}}$ to start	0		ns

- (1) t<sub>rst</sub> is the propagation delay measured from the time the  $\overline{\text{RESET}}$  pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t<sub>wL</sub>.

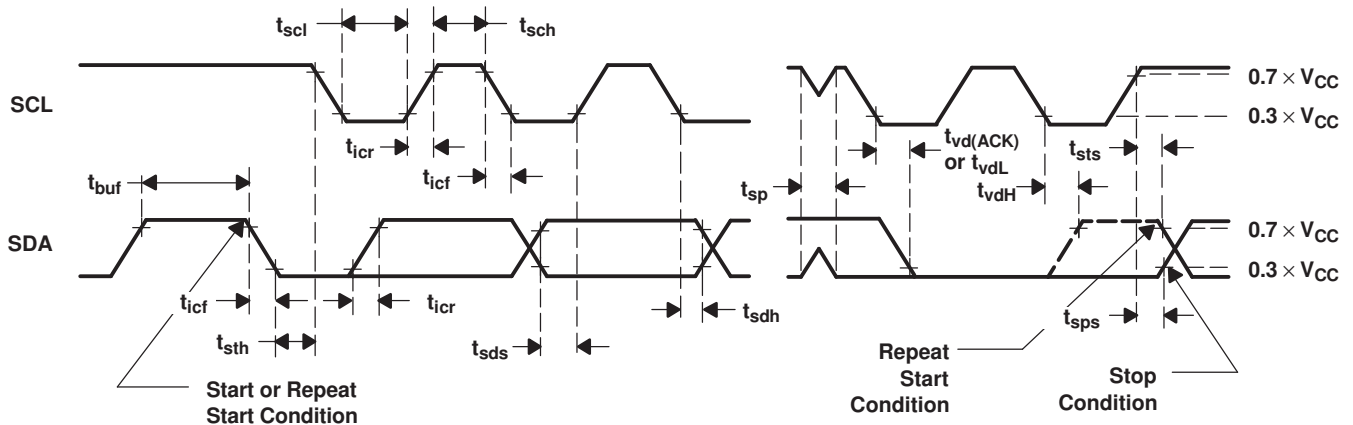
PARAMETER MEASUREMENT INFORMATION



I<sup>2</sup>C PORT LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I <sup>2</sup> C address + R/W
2	Control register data



VOLTAGE WAVEFORMS

- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>/t<sub>f</sub> ≤ 30 ns.
- C. The outputs are measured one at a time, with one transition per measurement.

Figure 10. I<sup>2</sup>C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

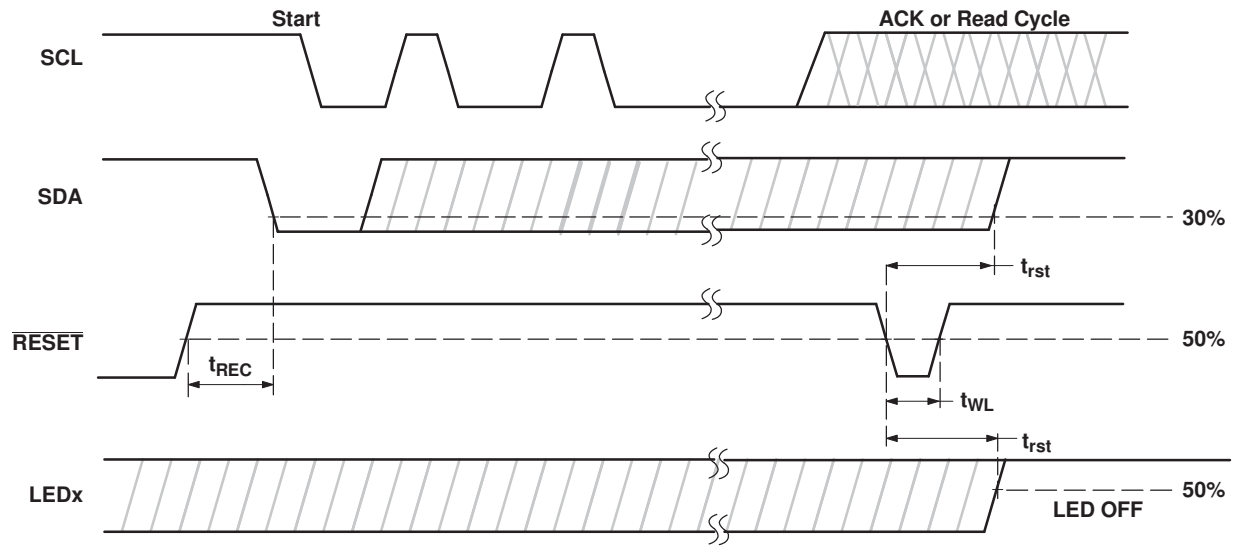
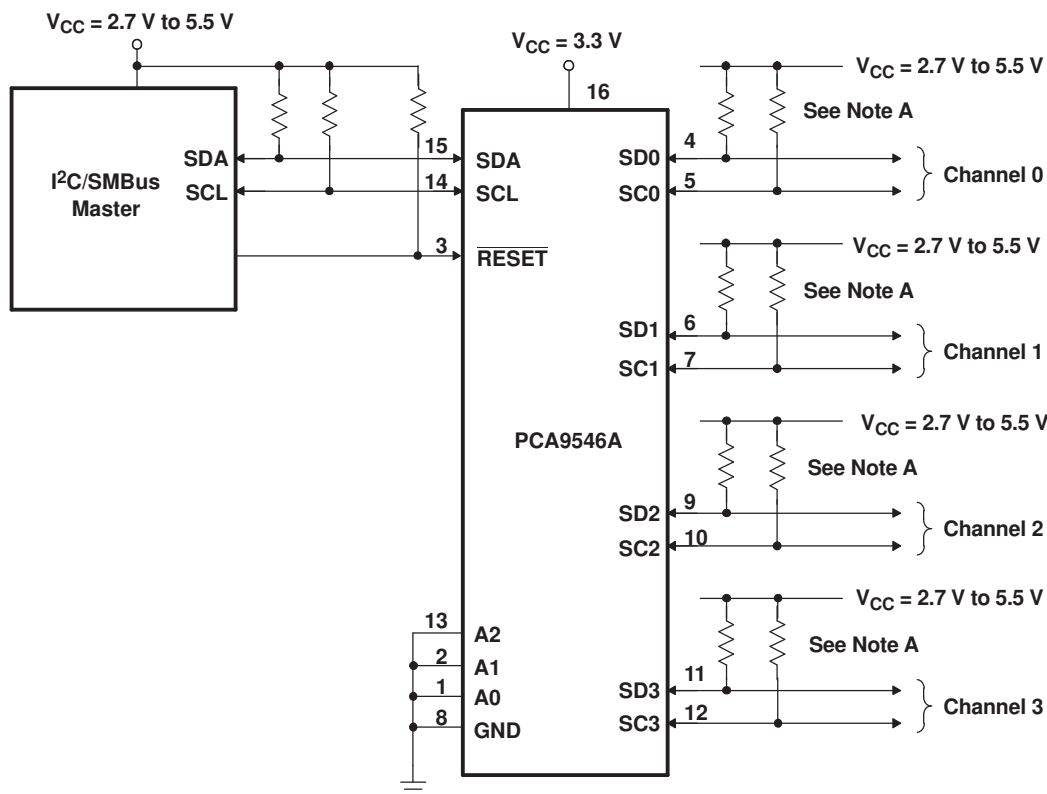


Figure 11. Reset Timing

**APPLICATION INFORMATION**

Figure 12 shows an application in which the PCA9546A can be used.



A. Pin numbers shown are for the D, DGV, DW, PW, and RGY packages.

**Figure 12. Typical Application**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PCA9546AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADGVT	PREVIEW	TVSOP	DGV	20	250	TBD	Call TI	Call TI
PCA9546ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ADWT	PREVIEW	SOIC	DW	16	250	TBD	Call TI	Call TI
PCA9546AGQNR	PREVIEW	BGA MICROSTAR JUNIOR	GQN	20	1000	TBD	Call TI	Call TI
PCA9546APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9546ARGVR	ACTIVE	QFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PCA9546ARGVRG4	ACTIVE	QFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9546ARGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9546ARGYRG4	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9546AZQNR	PREVIEW	BGA MI CROSTA R JUNI OR	ZQN	20	1000	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

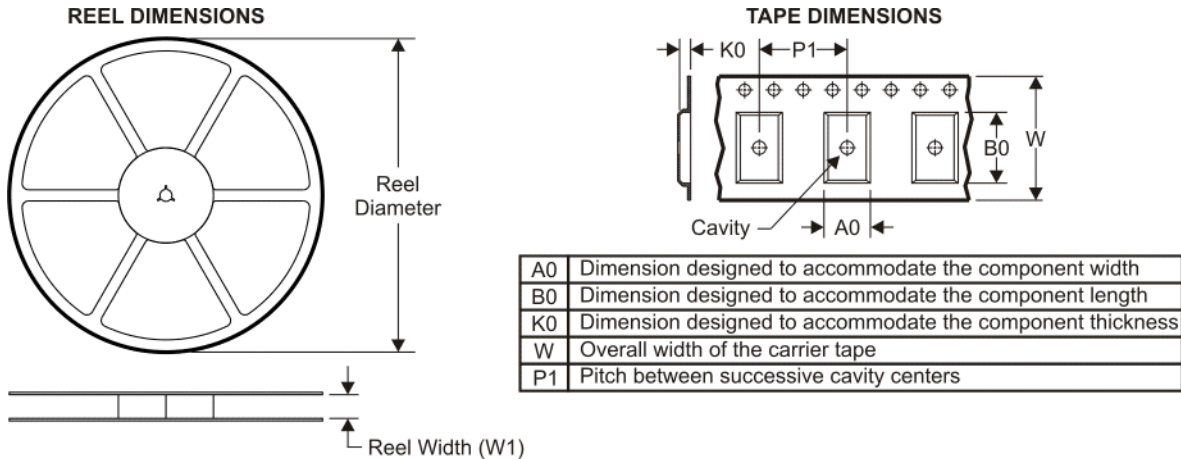
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

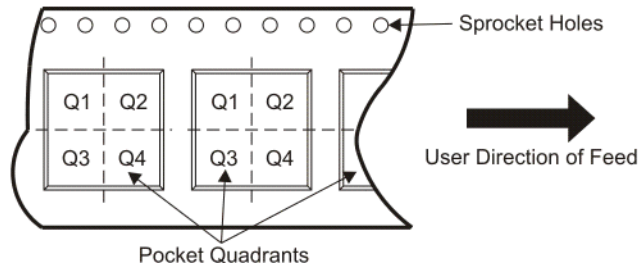
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**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

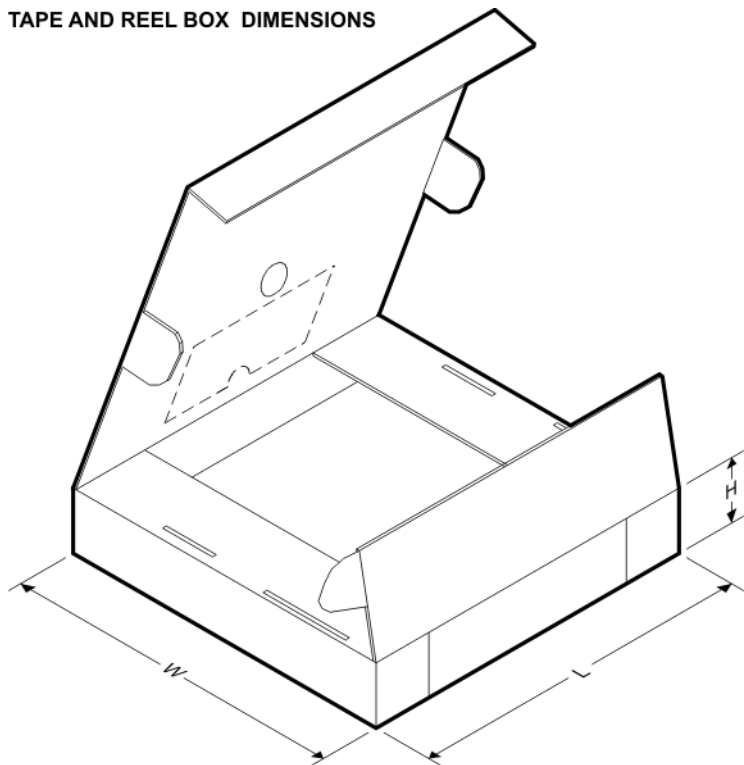


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9546ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9546ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
PCA9546ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9546APWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
PCA9546ARGVR	QFN	RGV	16	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
PCA9546ARGYR	QFN	RGY	16	1000	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**

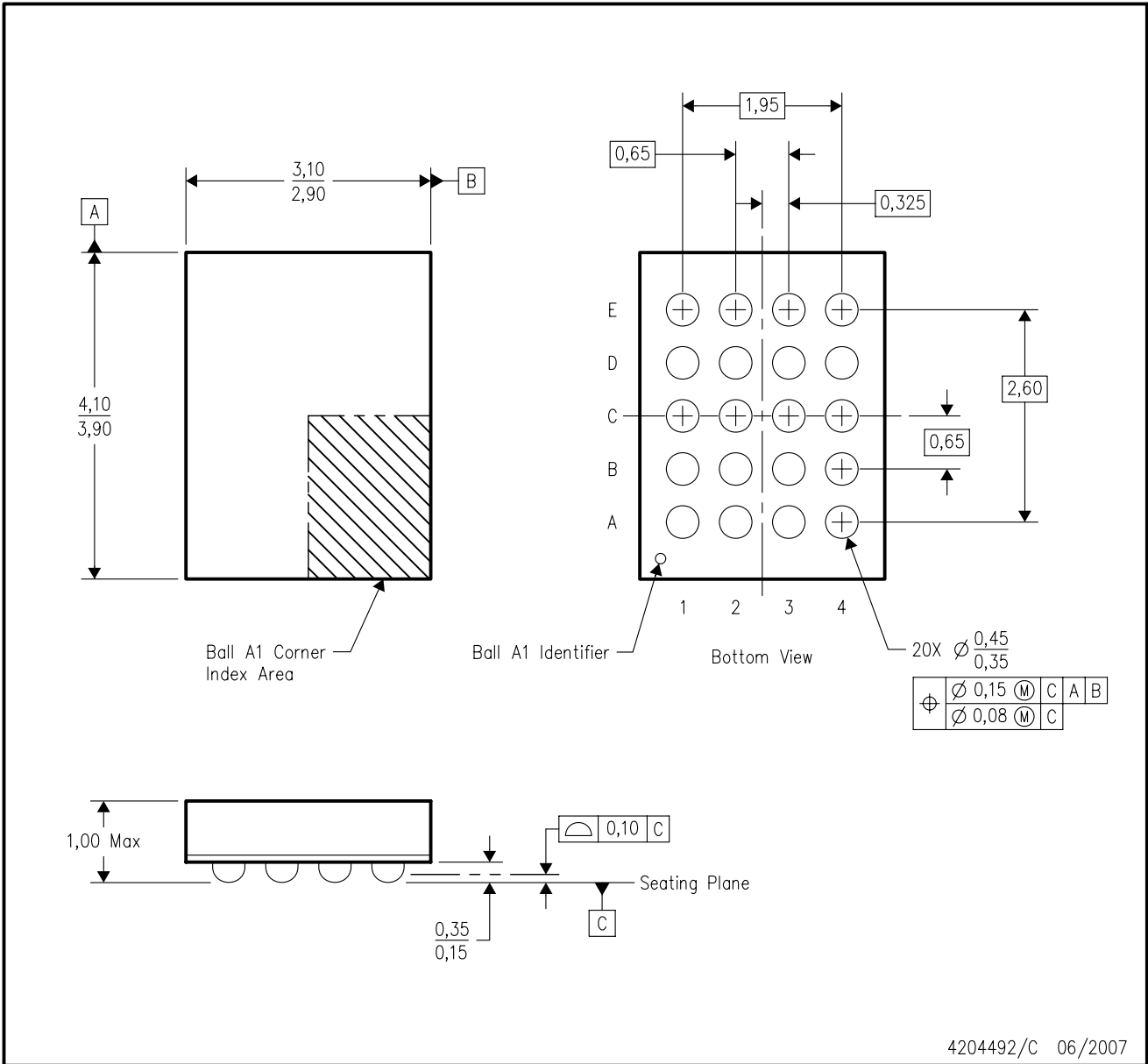


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9546ADGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
PCA9546ADR	SOIC	D	16	2500	333.2	345.9	28.6
PCA9546ADWR	SOIC	DW	16	2000	346.0	346.0	33.0
PCA9546APWR	TSSOP	PW	16	2000	346.0	346.0	29.0
PCA9546ARGVR	QFN	RGV	16	2500	346.0	346.0	29.0
PCA9546ARGYR	QFN	RGY	16	1000	190.5	212.7	31.8

ZQN (R-PBGA-N20)

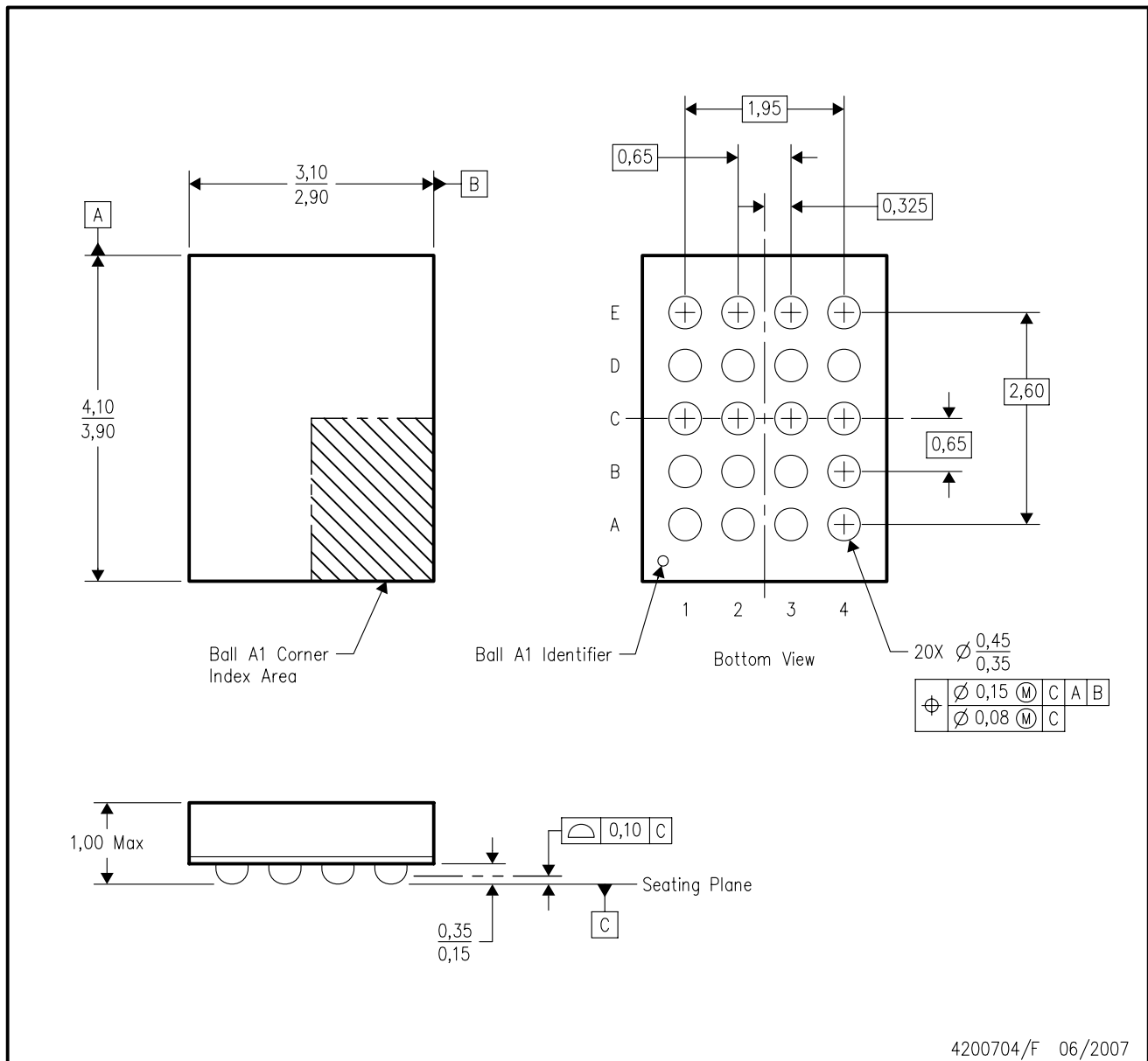
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BC-2.
  - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



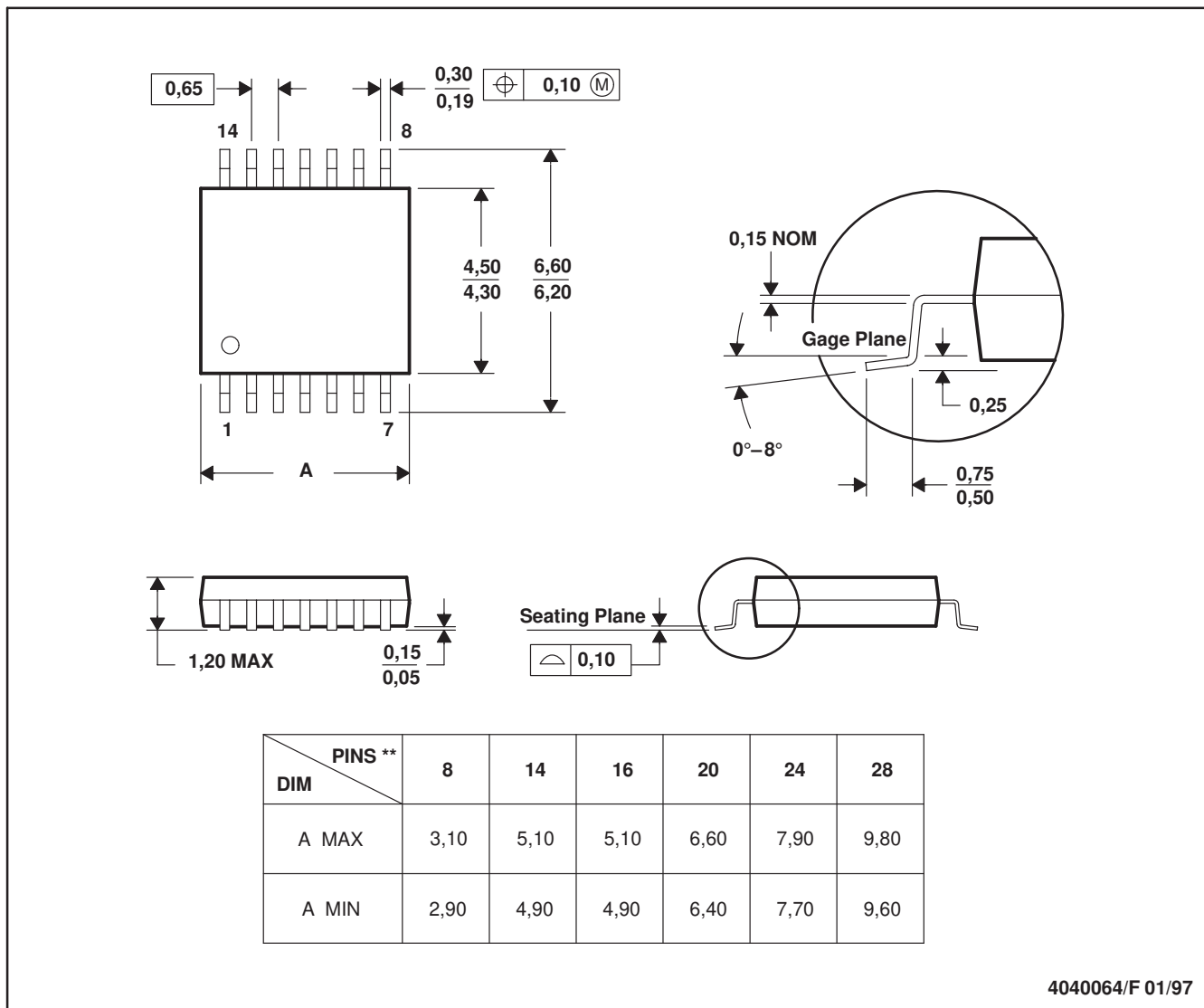
4200704/F 06/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BC-2.
  - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

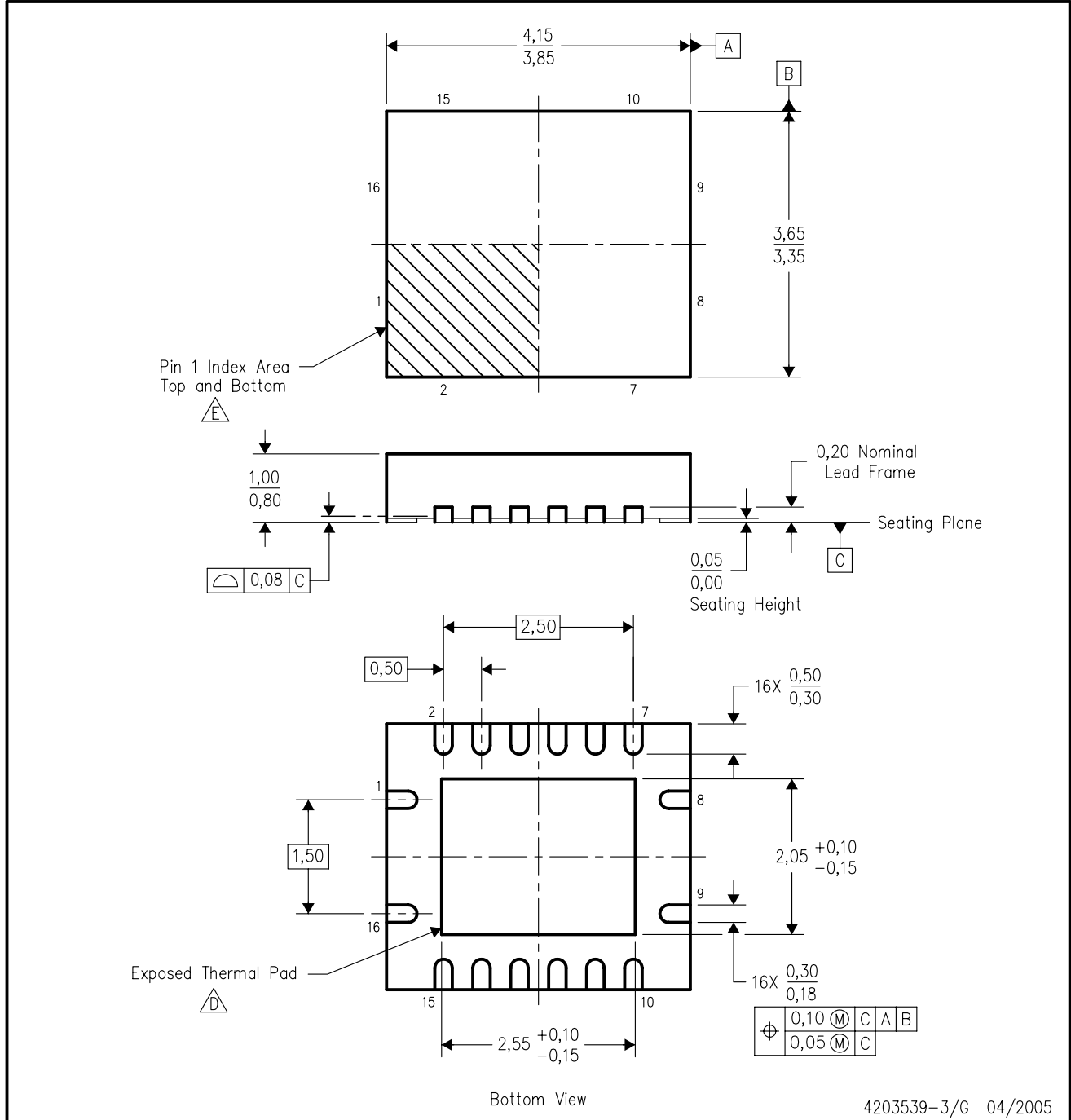


4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



4203539-3/G 04/2005

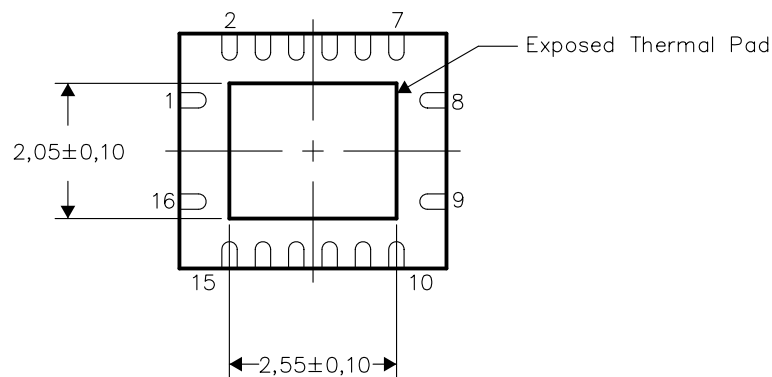
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BB.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

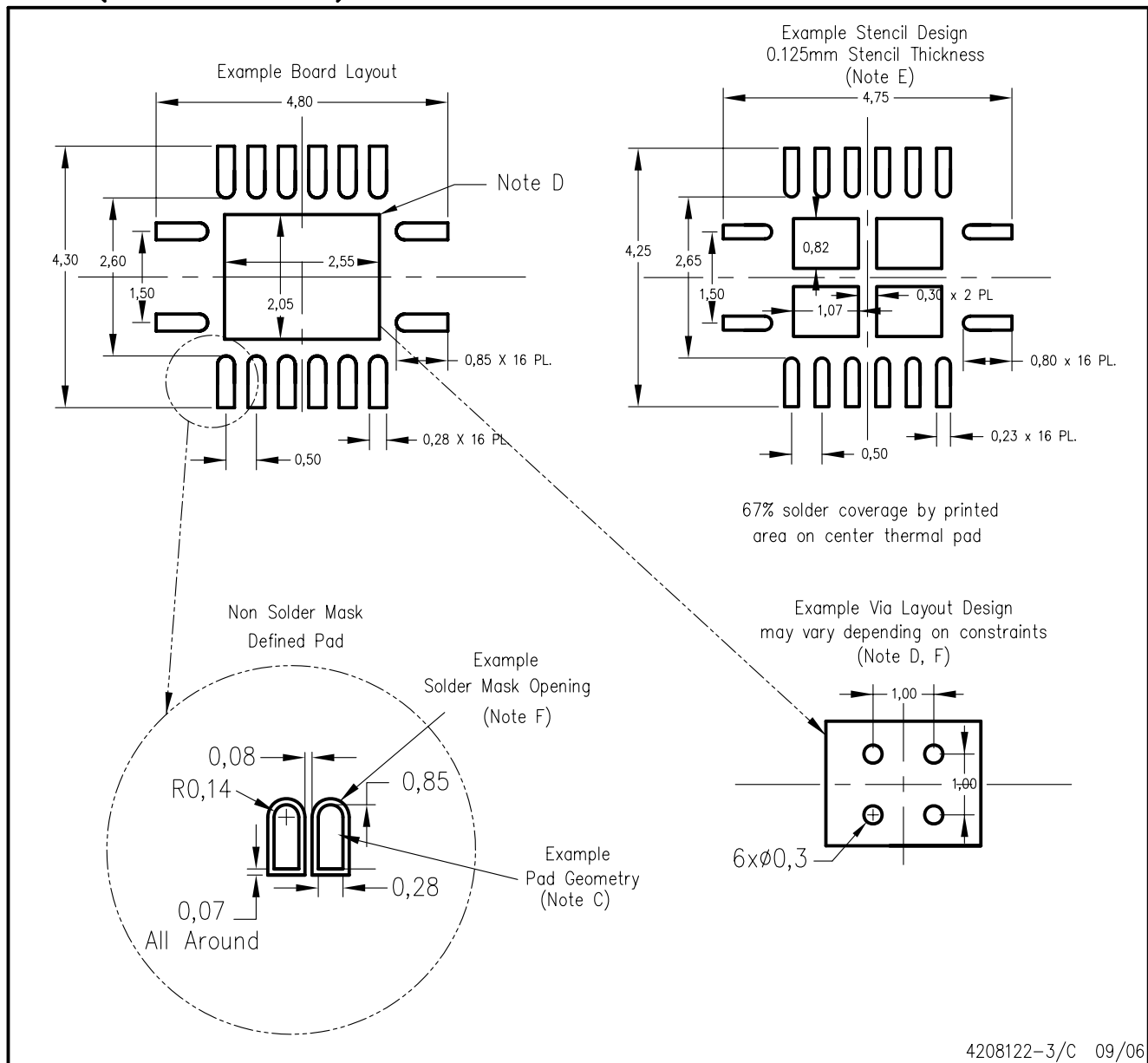


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

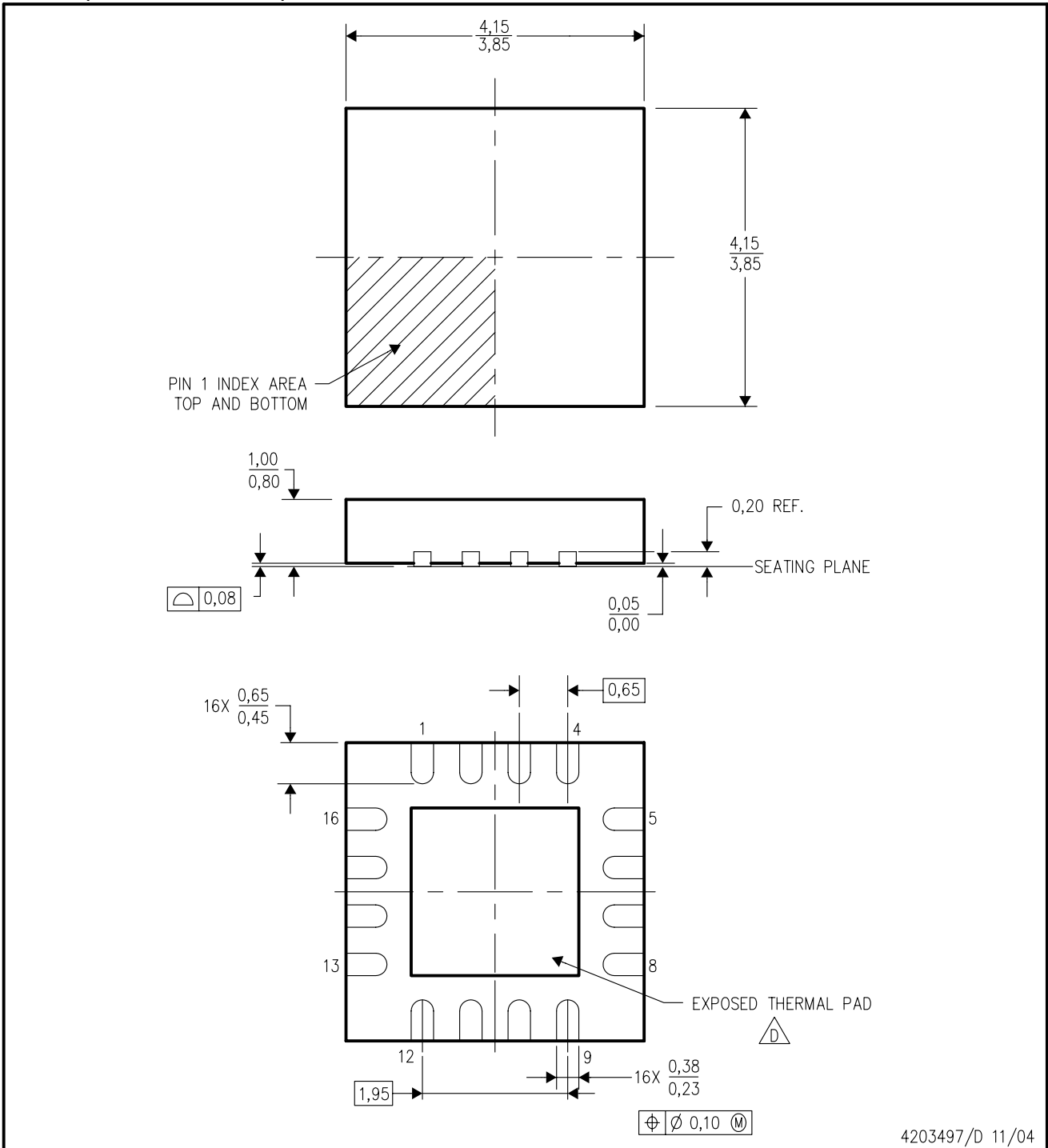
RGY (R-PQFP-N16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RGV (S-PQFP-N16)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

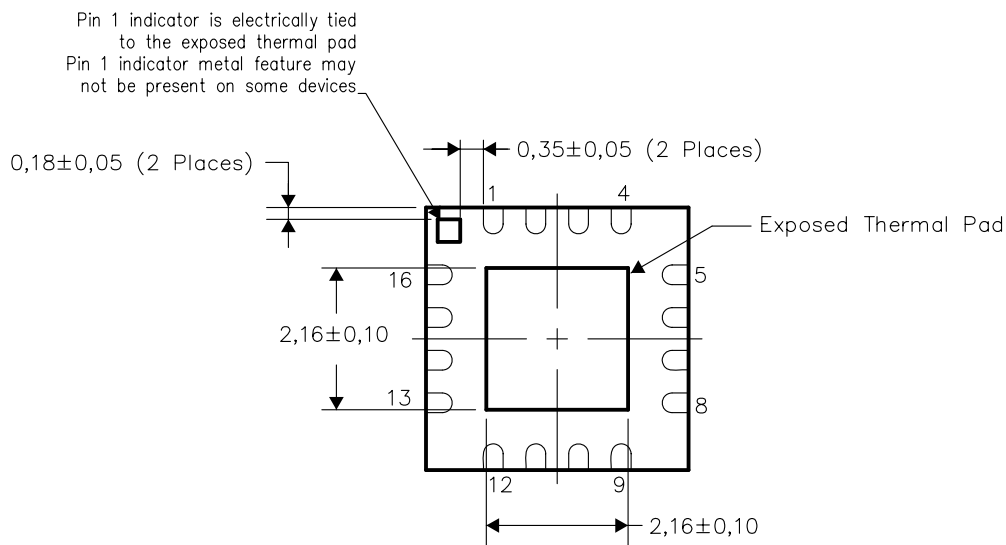


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

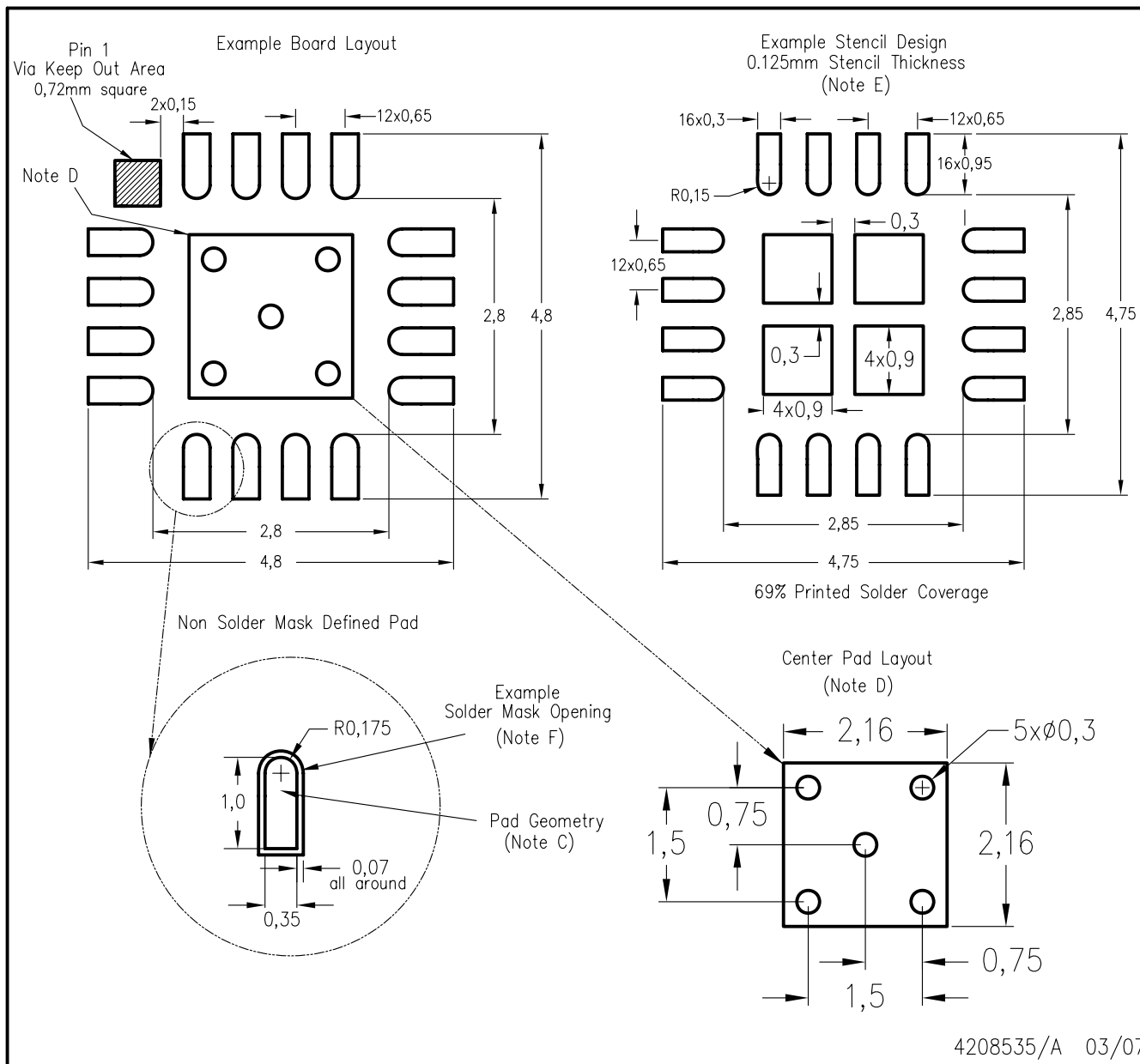


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

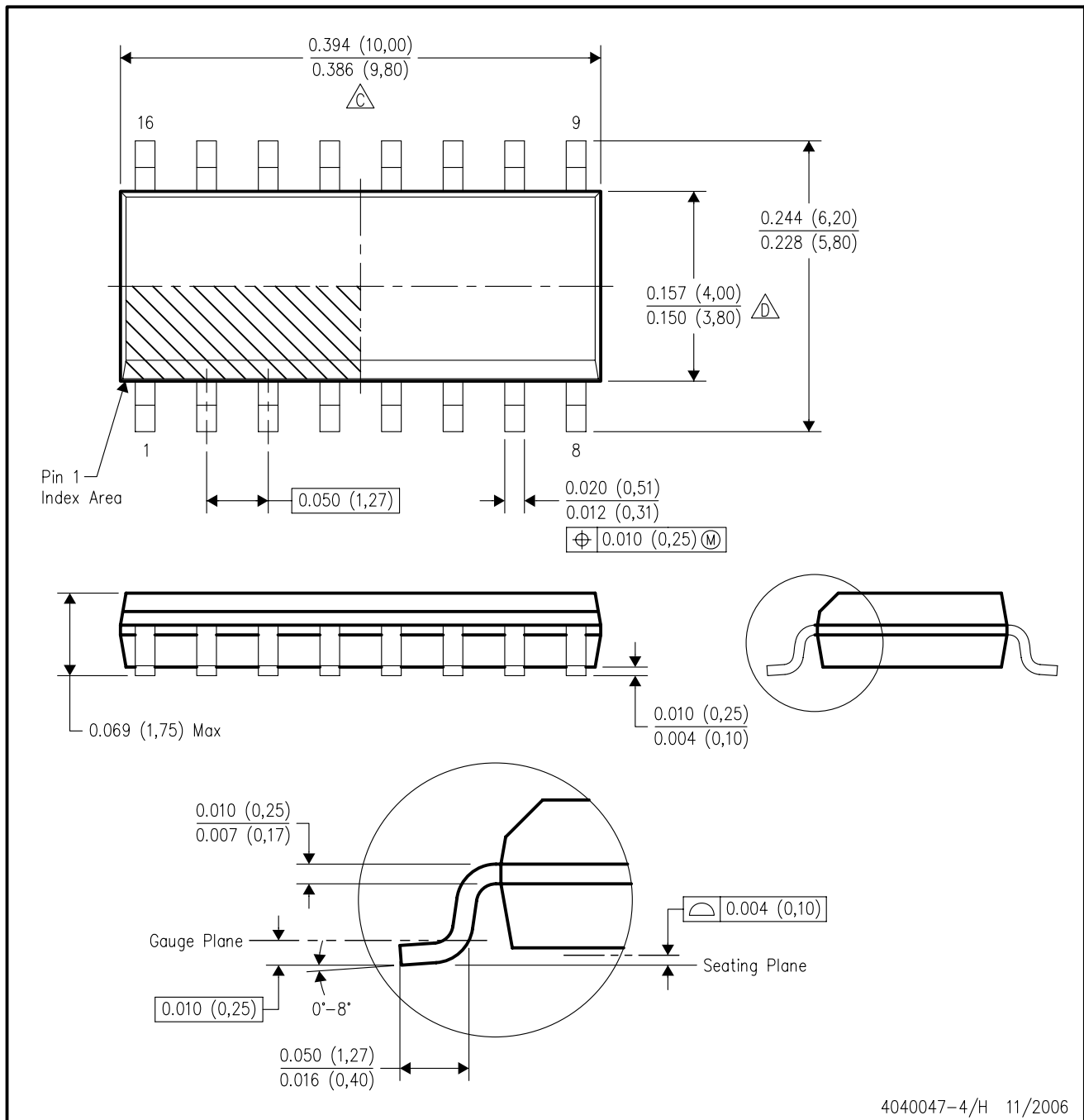
# RGV (S-PQFP-N16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.

D (R-PDSO-G16)

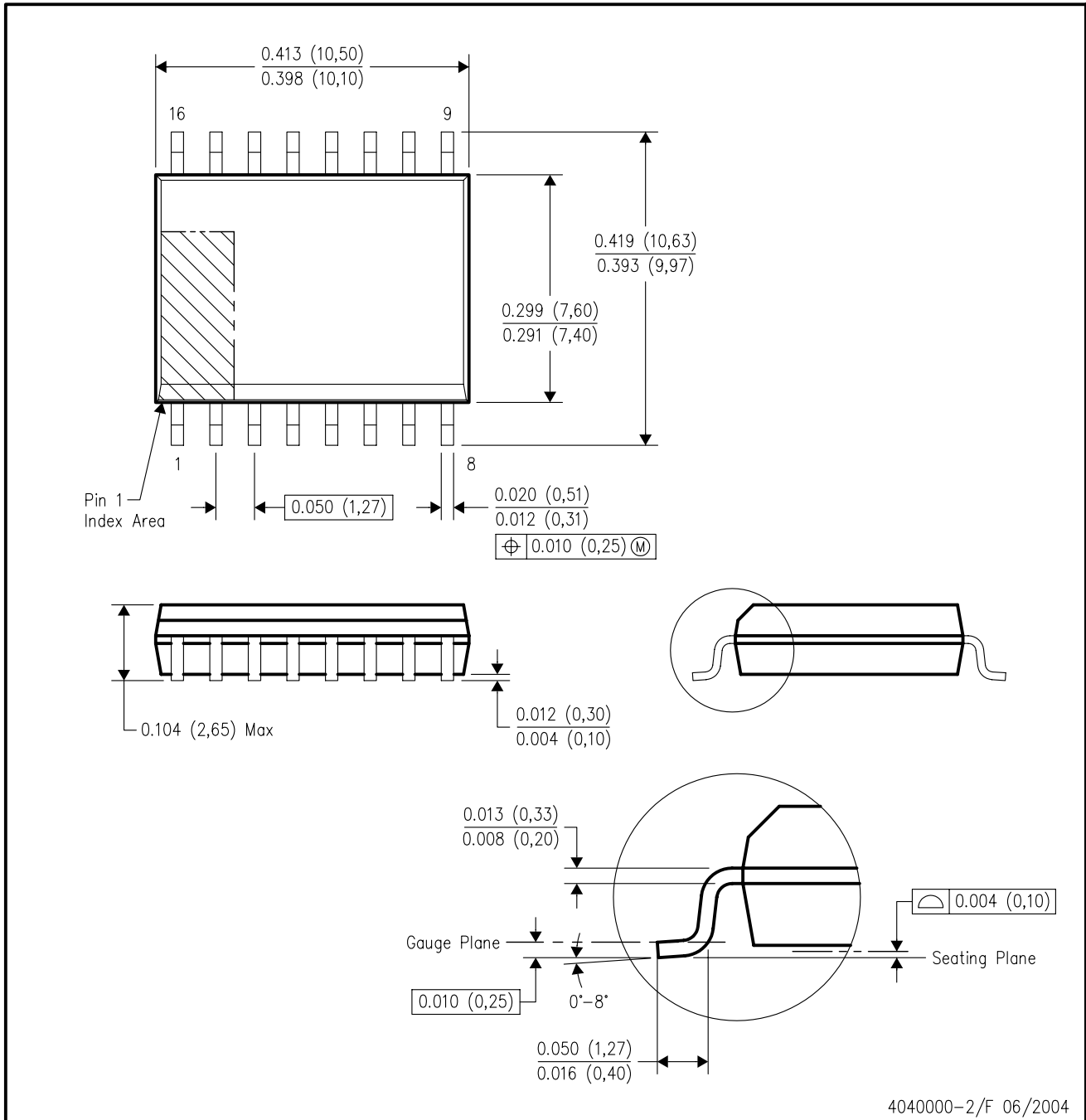
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

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