192-kHz STEREO ASYNCHRONOUS SAMPLE-RATE CONVERTER

Check for Samples: SRC4190-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Automatic Sensing of the Input-To-Output Sampling Ratio**
- **Wide Input-to-Output Sampling Range: 16:1 to 1:16**
- **Supports Input and Output Sampling Rates up to 212 kHz**
- **Dynamic Range: 128 dB (–60 dBFS Input, BW = 20 Hz to f_S/2, A-Weighted)**
- **THD+N: –125 db (0 dBFS Input, BW = 20 Hz to f_S/2)**
- **Attenuates Sampling and Reference Clock Jitter**
- **High Performance, Linear Phase Digital Filtering**
- **Flexible Audio Serial Ports**
- **Master or Slave Mode Operation**
- **Supports I^2S, Left Justified, Right Justified, and TDM Data Formats**
- **Supports 16, 18, 20, or 24-Bit Audio Data**
- **TDM Mode Allows Daisy Chaining of up to Eight Devices**
- **Supports 24-, 20-, 18-, or 16-Bit Input and Output Data**
- **All Output Data Is Dithered From the Internal 28-Bit Data Path**
- **Low Group Delay Option for Interpolation Filter**
- **Soft Mute Function**
- **Bypass Mode**
- **Power Down Mode**
- **Operates From a Single 3.3-V Power Supply**
- **Small SSOP-28 Package**
- **Pin Compatible With the SRC4192, AD1895, and AD1896**

APPLICATIONS

- **Digital Mixing Consoles**
- **Digital Audio Workstations**
- **Audio Distribution Systems**
- **Broadcast Studio Equipment**
- **High-End A/V Receivers**
- **General Digital Audio Processing**

DESCRIPTION

The SRC4190 is an asynchronous sample rate converter designed for professional and broadcast audio applications. The SRC4190 combines a wide input-to-output sampling ratio with outstanding dynamic range and low distortion. Input and output serial ports support standard audio formats, as well as a Time Division Multiplexed (TDM) mode. Flexible audio interfaces allow the SRC4190 to connect to a wide range of audio data converters, digital audio receivers and transmitters, and digital signal processors.

The SRC4190 is a standalone pin-programmed device, with control pins for mode, data format, mute, bypass, and low group delay functions.

The SRC4190 may be operated from a single 3.3-V power supply. A separate digital I/O supply (V_{IO}) operates over the 1.65-V to 3.6-V supply range, allowing greater flexibility when interfacing to current and future generation signal processors and logic devices. The SRC4190 is available in an SSOP-28 package.

ORDERING INFORMATION(1)

T_A	PACKAGE (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DB	Reel of 2000	SRC4190IDBRQ1	SRC4190Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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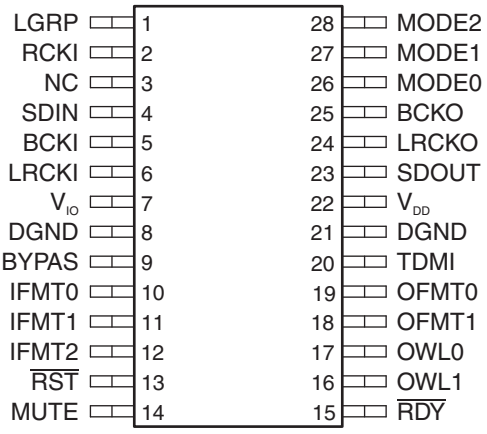
DB PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
LGRP	1	Low group delay control input (active high)
RCKI	2	Reference clock input
NC	3	No internal connection
SDIN	4	Audio serial data input
BCKI	5	Input port bit clock I/O
LRCKI	6	Input port left/right word clock I/O
V_{IO}	7	Digital I/O supply, 1.65 V to V_{DD}
DGND	8	Digital ground
BYPAS	9	ASRC bypass control input (active high)
IFMT0	10	Input port data format control input
IFMT1	11	Input port data format control input
IFMT2	12	Input port data format control input
$\overline{RST}$	13	Reset input (active low)
MUTE	14	Output mute control input (active high)
$\overline{RDY}$	15	ASRC ready status output (active low)
OWL1	16	Output port data word length control input
OWL0	17	Output port data word length control input
OFMT1	18	Output port data format control input
OFMT0	19	Output port data format control input
TDMI	20	TDM data input (connect to DGND when not in use)
DGND	21	Digital ground
V_{DD}	22	Digital core supply, 3.3 V
SDOUT	23	Audio serial data output
LRCKO	24	Output port left/right word clock I/O
BCKO	25	Output port bit clock I/O
MODE0	26	Serial port mode control input
MODE1	27	Serial port mode control input
MODE2	28	Serial port mode control input

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Core supply voltage range	–0.3 V to 4 V
V_{IO}	I/O supply voltage range	–0.3 V to 4 V
V_I	Digital input voltage	–0.3 V to 4 V
T_A	Operating free-air temperature range	–40°C to 85°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dynamic Performance(1)							
	Resolution				24		bits
f_{SIN}	Input sampling frequency			4		212	kHz
f_{SOUT}	Output sampling frequency			4		212	kHz
	Input:output sampling ratio	Upsampling				1:16	
		Downsampling				16:1	
	Dynamic range	BW = 20 Hz to f_{SOUT}/2, –60-dBFS Input, f_{IN} = 1 kHz, Unweighted (add 3 dB to specification for A-weighted result)	44.1 kHz : 48 kHz		125		dB
			48 kHz : 44.1 kHz		125		
			48 kHz : 96 kHz		125		
			44.1 kHz : 192 kHz		125		
			96 kHz : 48 kHz		125		
			192 kHz : 12 kHz		125		
			192 kHz : 32 kHz		125		
			192 kHz : 48 kHz		125		
			32 kHz : 48 kHz		125		
			12 kHz : 192 kHz		125		
	Total harmonic distortion + noise	BW = 20 Hz to f_{SOUT}/2, 0-dBFS Input, f_{IN} = 1 kHz, Unweighted	44.1 kHz : 48 kHz		–125		dB
			48 kHz : 44.1 kHz		–125		
			48 kHz : 96 kHz		–125		
			44.1 kHz : 192 kHz		–125		
			96 kHz : 48 kHz		–125		
			192 kHz : 12 kHz		–125		
			192 kHz : 32 kHz		–125		
			192 kHz : 48 kHz		–125		
			32 kHz : 48 kHz		–125		
			12 kHz : 192 kHz		–125		
	Interchannel gain mismatch				0		dB
	Interchannel phase deviation				0		°
	Mute attenuation	24-bit word length, A-weighted			–128		dB

(1) Dynamic performance measured with an Audio Precision System Two Cascade or Cascade Plus.

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ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Interpolation Filter Characteristics						
	Passband				0.4535 × f_{SIN}	Hz
	Passband ripple				±0.007	dB
	Transition band		0.4535 × f_{SIN}		0.5465 × f_{SIN}	Hz
	Stop band		0.5465 × f_{SIN}			Hz
	Stop band attenuation		–125			dB
	Normal group delay time (LGRP = 0)			102.53125 / f_{SIN}		s
	Low group delay time (LGRP = 1)			70.53125 / f_{SIN}		s
Digital Decimation Filter Characteristics						
	Passband				0.4535 × f_{SOUT}	Hz
	Passband ripple				±0.008	dB
	Transition band		0.4535 × f_{SOUT}		0.5465 × f_{SOUT}	Hz
	Stop band		0.5465 × f_{SOUT}			Hz
	Stop band attenuation		–125			dB
	Group delay			36.46875 / f_{SOUT}		s
Digital I/O Characteristics						
V_{IH}	High-level input voltage		0.7 × V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{IO}	V
I_{IH}	High-level input current			0.5	10	µA
I_{IL}	Low-level input current			0.5	10	µA
V_{OH}	High-level output voltage	I_O = –4 mA	0.8 × V_{IO}		V_{IO}	V
V_{OL}	Low-level output voltage	I_O = 4 mA	0		0.2 × V_{IO}	V
C_{IN}	Input capacitance			3		pF

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ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Switching Characteristics							
f_{RCKI}	RCKI frequency(2) (3)			128 × f_{SMIN}		50	MHz
t_{RCKIP}	RCKI pulse duration			20		1/(128 × f_{SMIN})	ns
t_{RCKIH}	RCKI pulse duration, high			0.4 × t_{RCKIP}			ns
t_{RCKIL}	RCKI pulse duration, low			0.4 × t_{RCKIP}			ns
t_{RSTL}	$\overline{RST}$ pulse duration, low			500			ns
t_{LRIS}	LRCKI to BCKI setup time			10			ns
t_{SIH}	BCKI pulse duration, high			10			ns
t_{SIL}	BCKI pulse duration, low			10			ns
t_{LDIS}	SDIN data setup time			10			ns
t_{LDIH}	SDIN data hold time			10			ns
t_{DOPD}	SDOUT data delay time					10	ns
t_{DOH}	SDOUT data hold time			2			ns
t_{SOH}	BCKO pulse duration, high			10			ns
t_{SOL}	BCKO pulse duration, low			5			ns
t_{LROS}	LRCKO setup time			10			ns
t_{LROH}	LRCKO hold time			10			ns
t_{TDMS}	TDMI data setup time			10			ns
t_{TDMH}	TDMI data hold time			10			ns
Power Supplies							
V_{DD}	Core supply voltage			3	3.3	3.6	V
V_{IO}	Digital I/O supply voltage			1.65	3.3	3.6	V
I_{DDPD}	V_{DD} supply current, power down	V_{DD} = 3.3 V, V_{IO} = 3.3 V	$\overline{RST}$ = 0, No clocks			100	µA
I_{DDD}	V_{DD} supply current, dynamic		f_{SIN} = f_{SOUT} = 192 kHz		66		mA
I_{IOPD}	V_{IO} supply current, power down		$\overline{RST}$ = 0, No clocks			100	µA
I_{IOD}	V_{IO} supply current, dynamic		f_{SIN} = f_{SOUT} = 192 kHz		2		mA
P_D	Total power dissipation, power down	V_{DD} = 3.3 V, V_{IO} = 3.3 V	$\overline{RST}$ = 0, No clocks			660	µW
P_D	Total power dissipation, dynamic		f_{SIN} = f_{SOUT} = 192 kHz		225		mW

(2) f_{SMIN} = min (f_{SIN}, f_{SOUT})
(3) f_{SMAX} = max (f_{SIN}, f_{SOUT})

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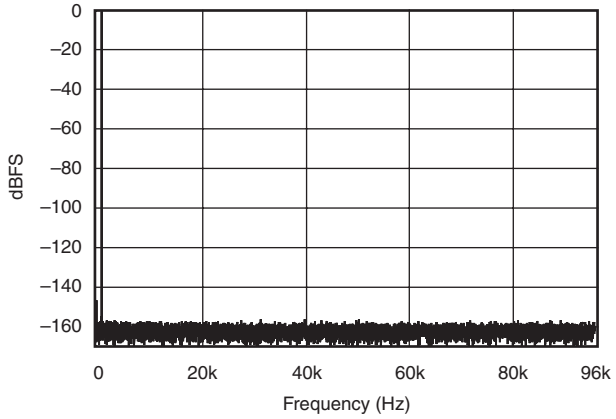
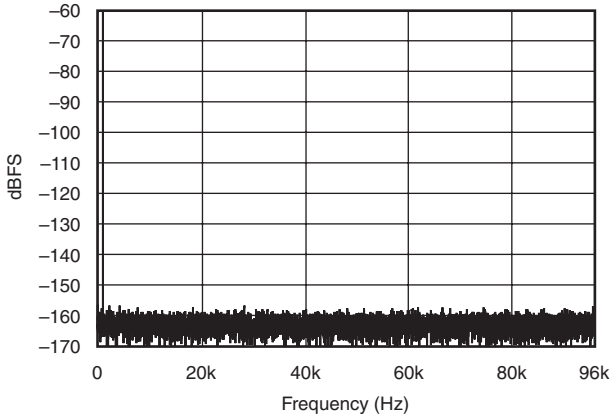
TYPICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

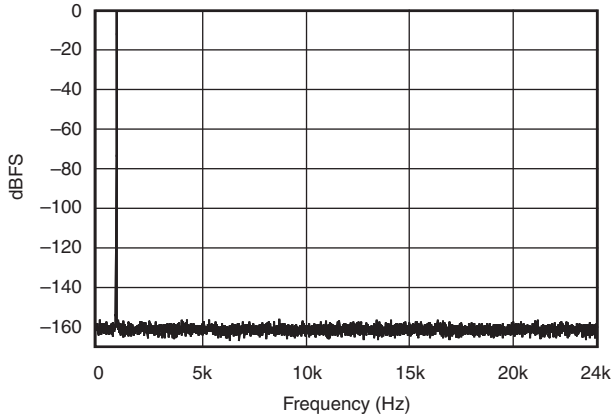
FFT with 1kHz INPUT TONE at 0dBFS
(12kHz:192kHz)



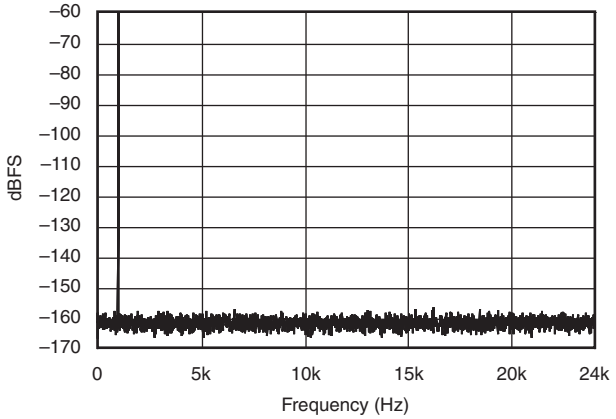
FFT with 1kHz INPUT TONE at –60dBFS
(12kHz:192kHz)



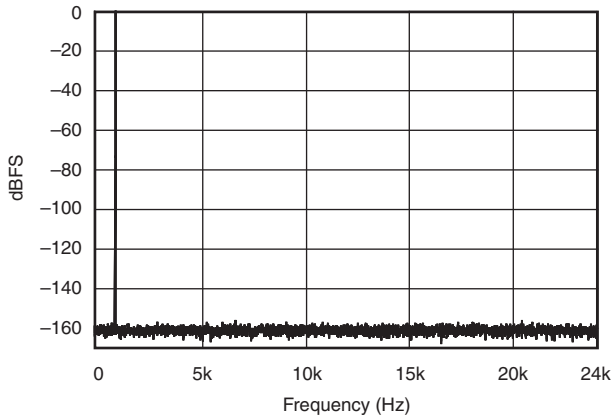
FFT with 1kHz INPUT TONE at 0dBFS
(32kHz:48kHz)



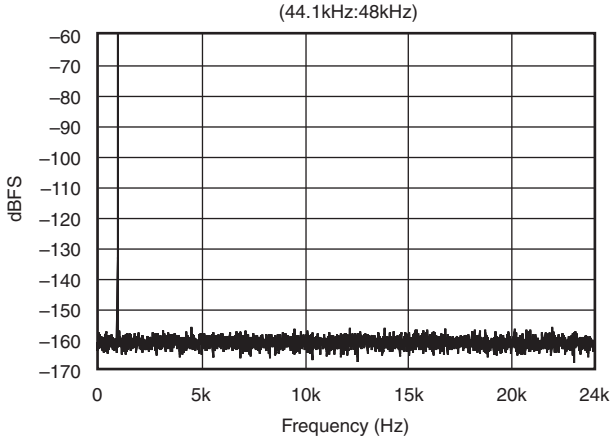
FFT with 1kHz INPUT TONE at –60dBFS
(32kHz:48kHz)



FFT with 1kHz INPUT TONE at 0dBFS
(44.1kHz:48kHz)



FFT with 1kHz INPUT TONE at –60dBFS
(44.1kHz:48kHz)



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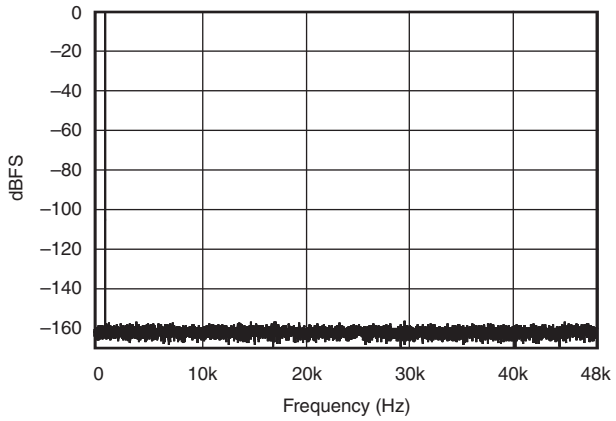
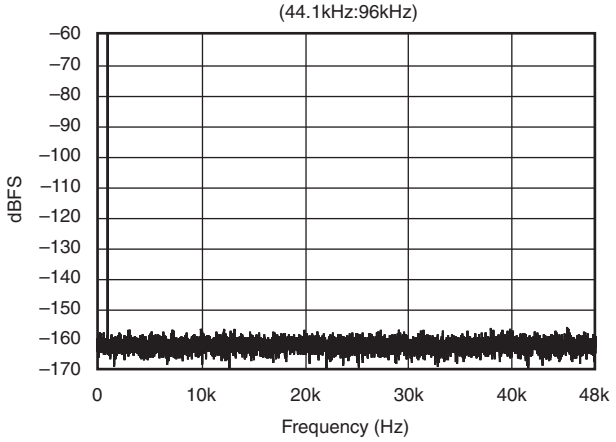
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

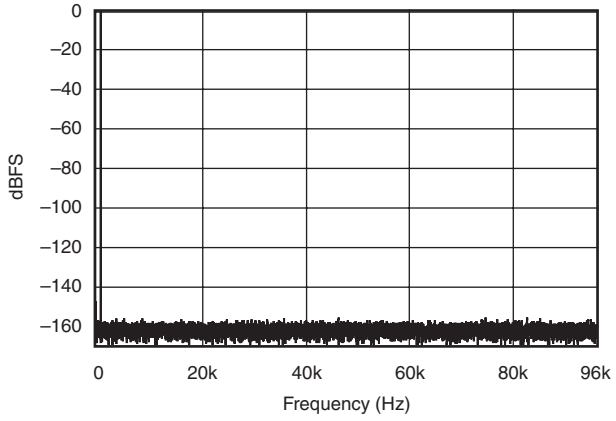
FFT with 1kHz INPUT TONE at 0dBFS
(44.1kHz:96kHz)



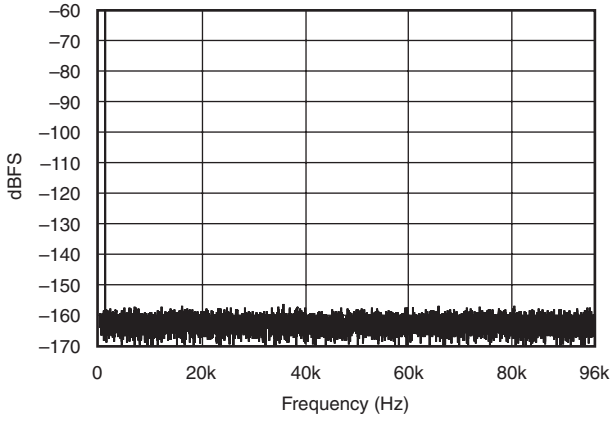
FFT with 1kHz INPUT TONE at –60dBFS
(44.1kHz:96kHz)



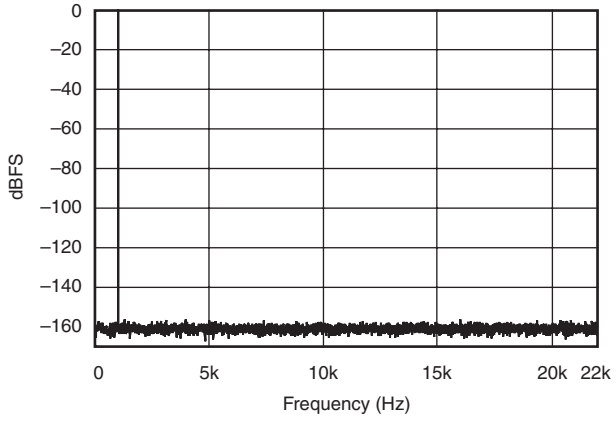
FFT with 1kHz INPUT TONE at 0dBFS
(44.1kHz:192kHz)



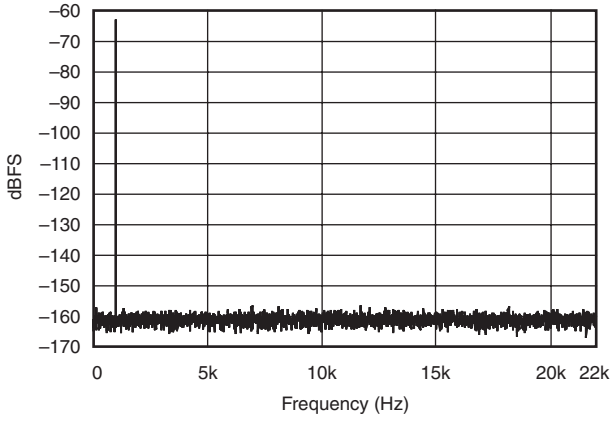
FFT with 1kHz INPUT TONE at –60dBFS
(44.1kHz:192kHz)



FFT with 1kHz INPUT TONE at 0dBFS
(48kHz:44.1kHz)



FFT with 1kHz INPUT TONE at –60dBFS
(48kHz:44.1kHz)



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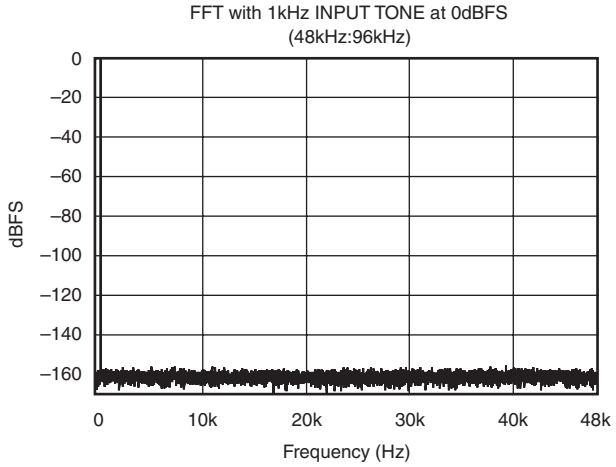
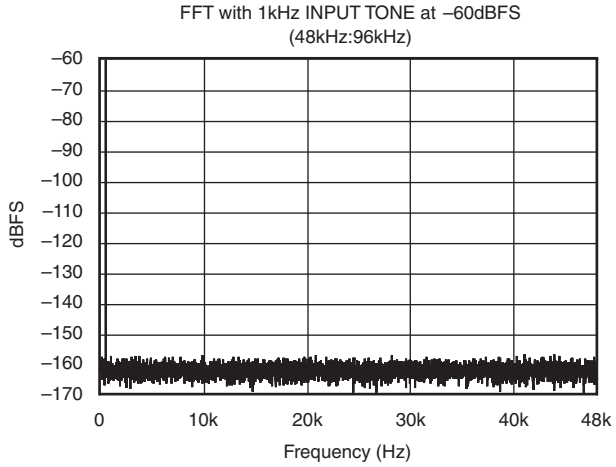
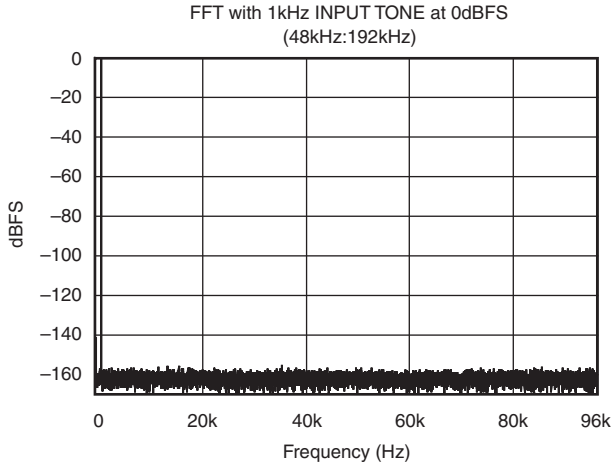
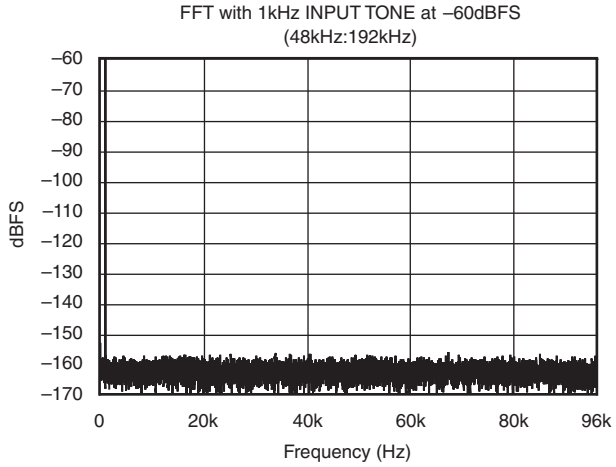
TYPICAL CHARACTERISTICS (continued)

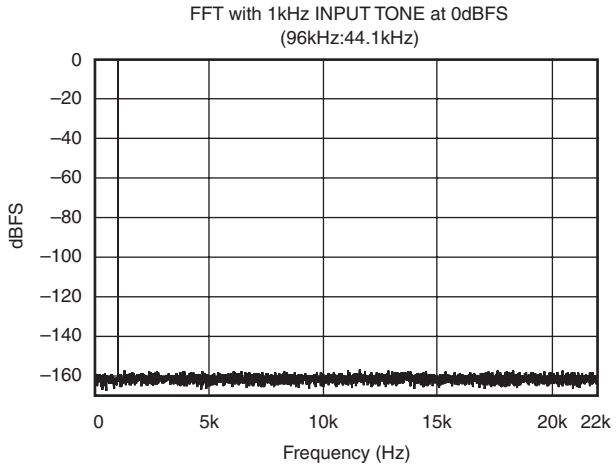
T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

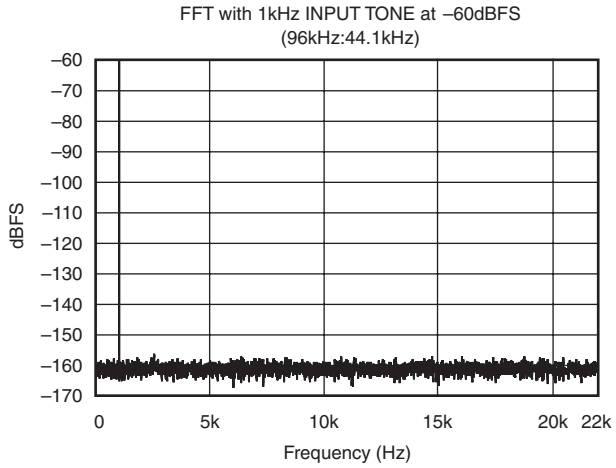












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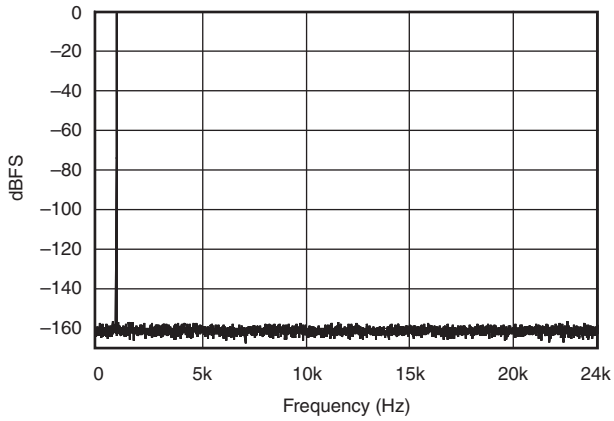
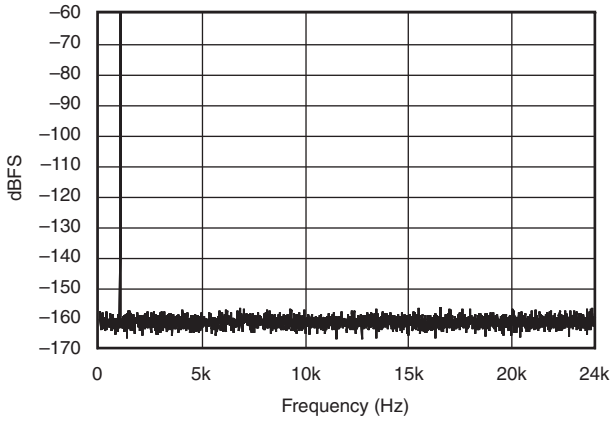
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

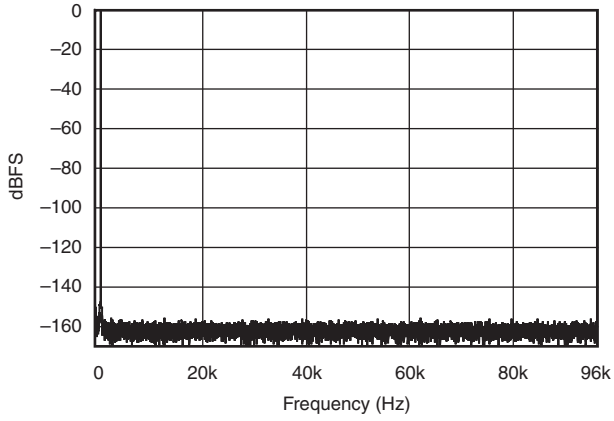
FFT with 1kHz INPUT TONE at 0dBFS
(96kHz:48kHz)



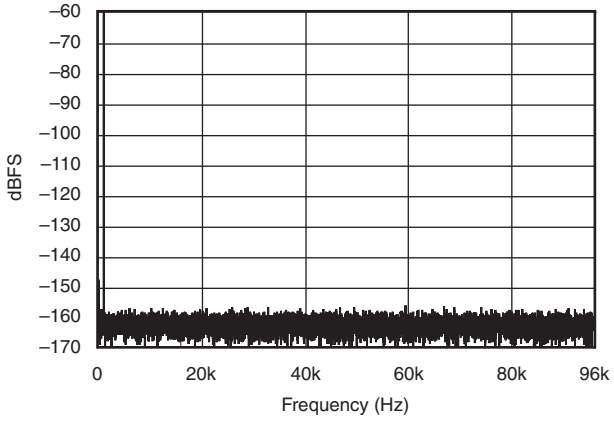
FFT with 1kHz INPUT TONE at –60dBFS
(96kHz:48kHz)



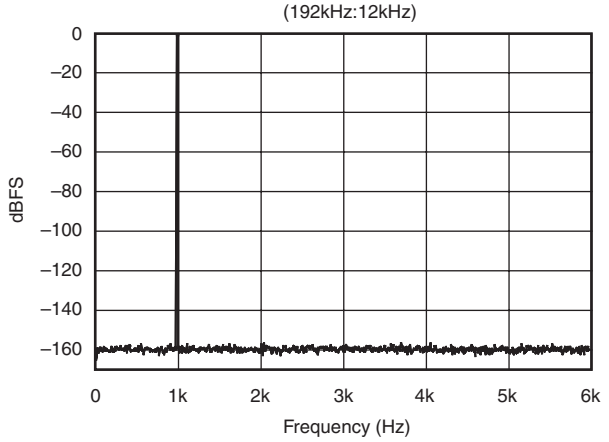
FFT with 1kHz INPUT TONE at 0dBFS
(96kHz:192kHz)



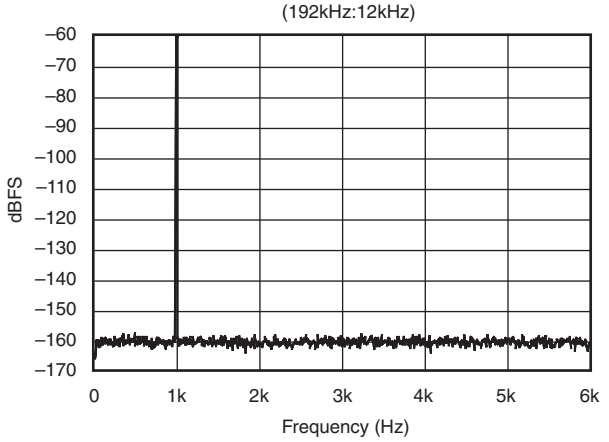
FFT with 1kHz INPUT TONE at –60dBFS
(96kHz:192kHz)



FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:12kHz)



FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:12kHz)



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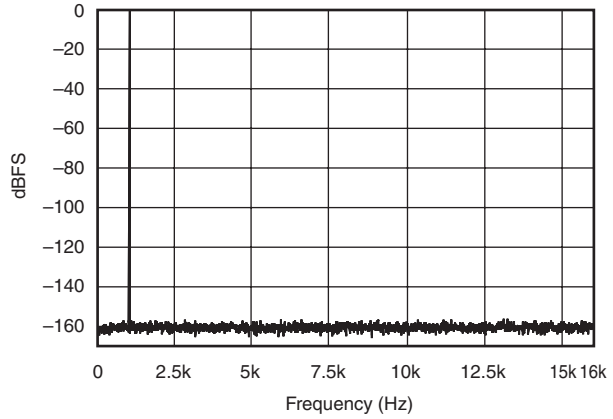
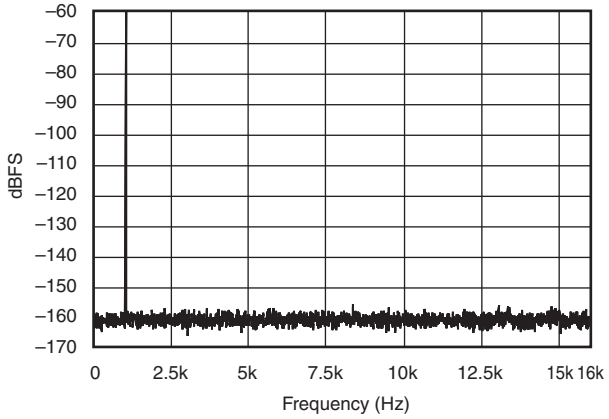
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

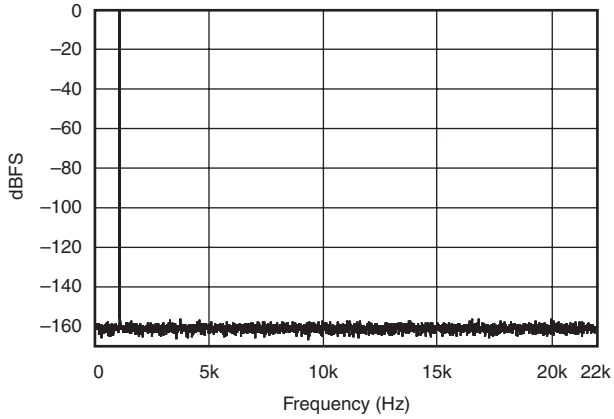
FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:32kHz)



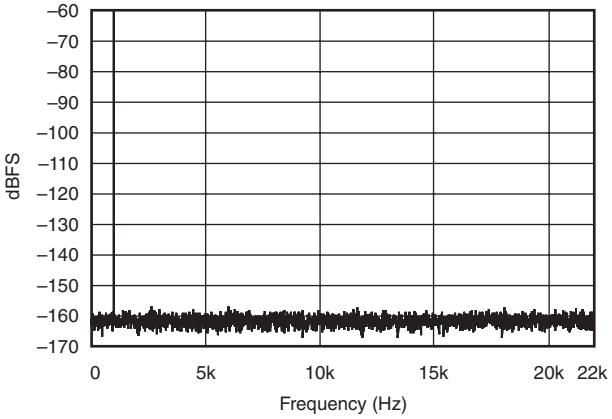
FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:12kHz)



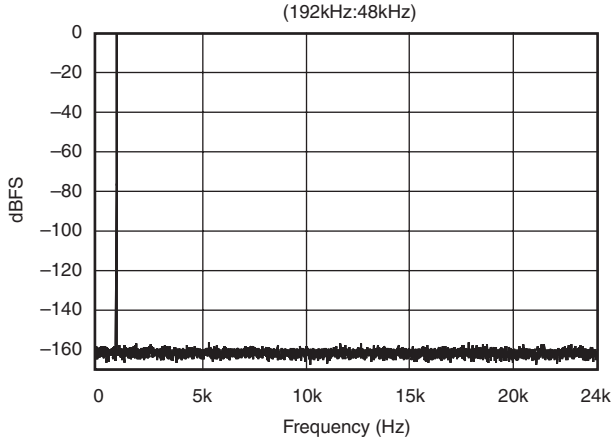
FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:44.1kHz)



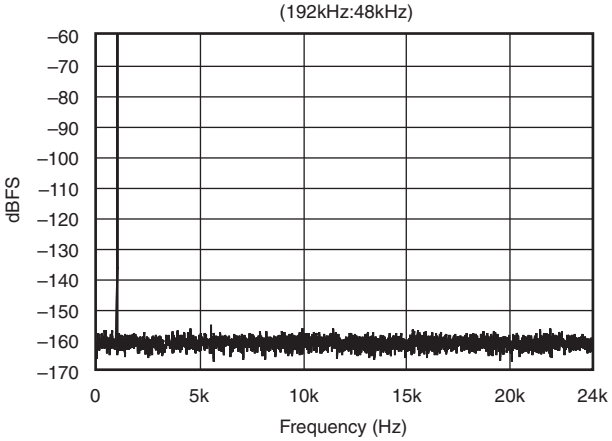
FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:44.1kHz)



FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:48kHz)



FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:48kHz)



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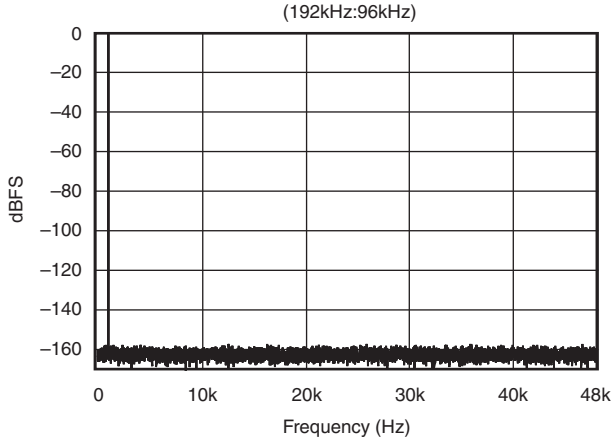
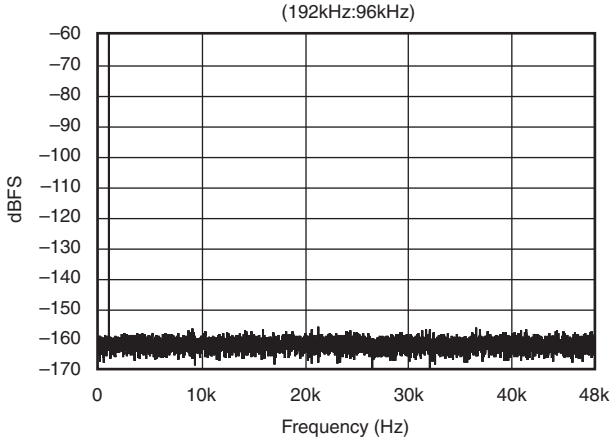
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

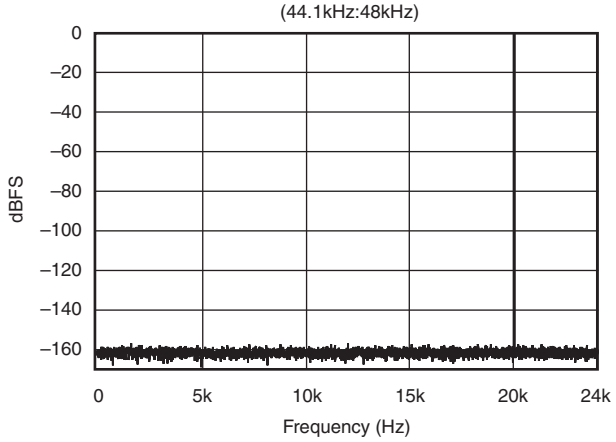
FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:96kHz)



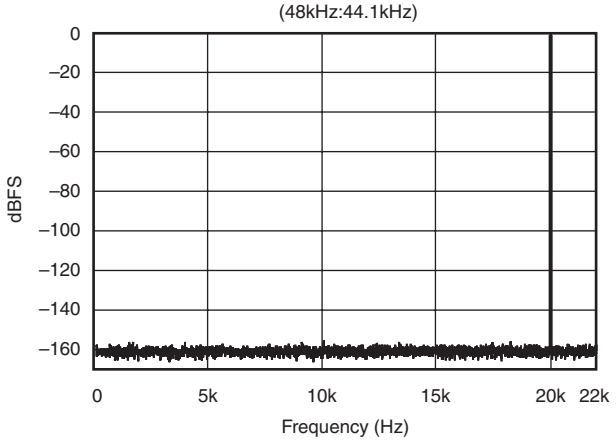
FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:96kHz)



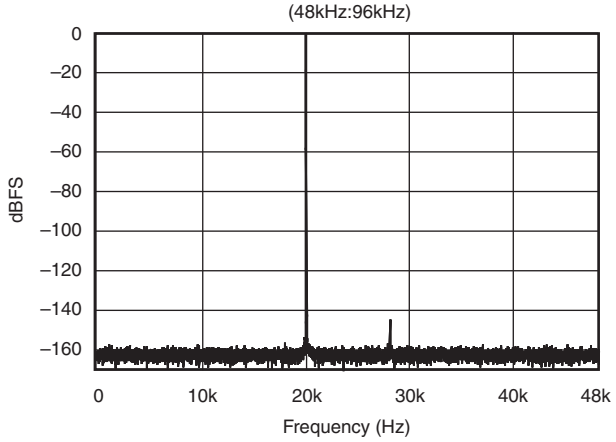
FFT with 20kHz INPUT TONE at 0dBFS
(44.1kHz:48kHz)



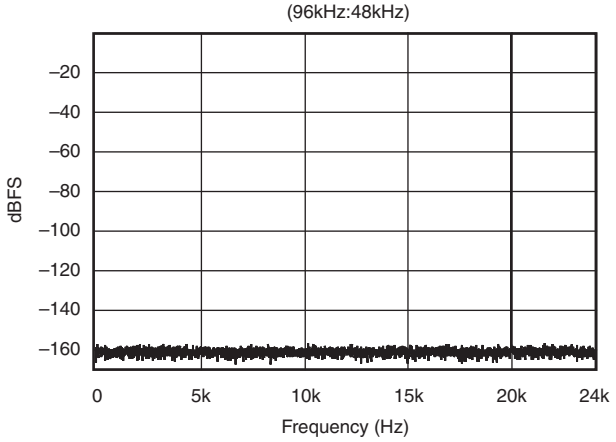
FFT with 20kHz INPUT TONE at 0dBFS
(48kHz:44.1kHz)



FFT with 20kHz INPUT TONE at 0dBFS
(48kHz:96kHz)



FFT with 20kHz INPUT TONE at 0dBFS
(96kHz:48kHz)



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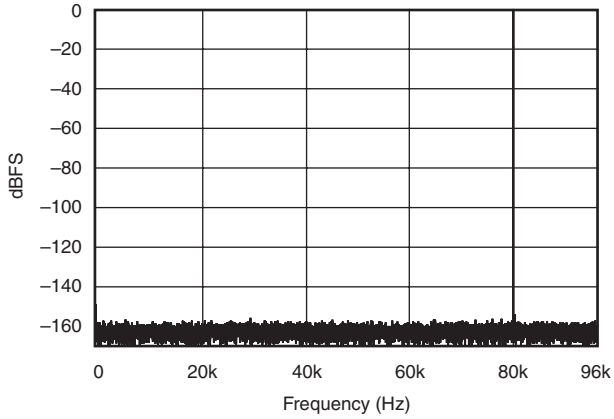
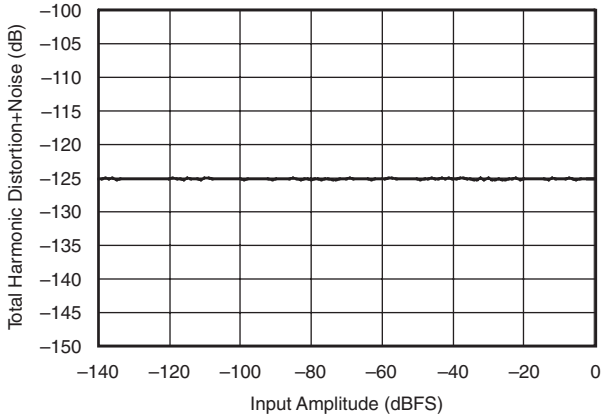
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

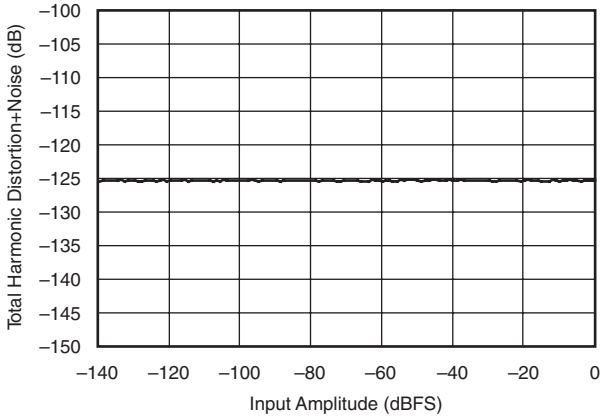
FFT with 80kHz INPUT TONE at 0dBFS
(192kHz:192kHz)



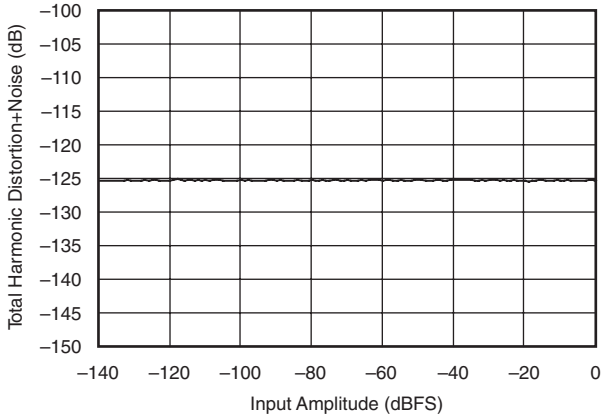
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(44.1kHz:48kHz)



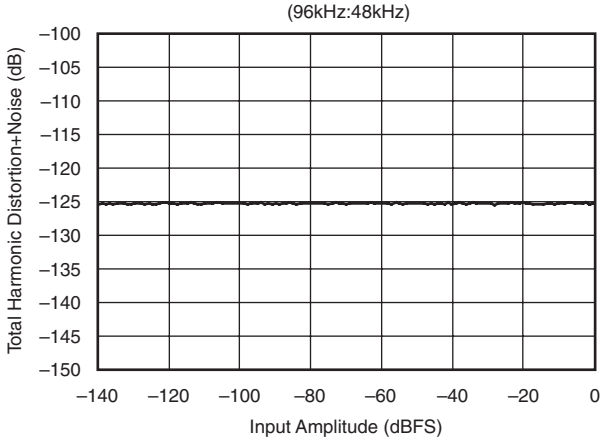
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(48kHz:44.1kHz)



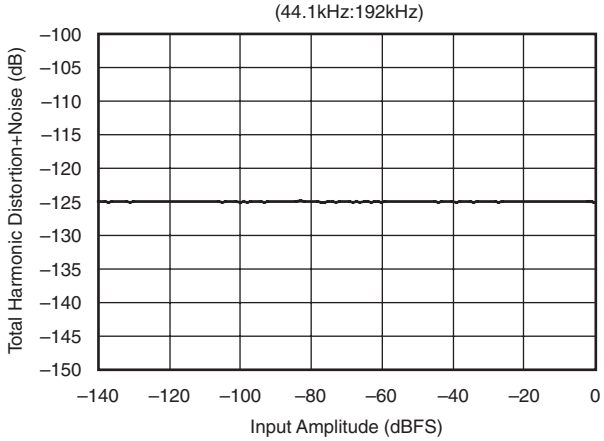
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(48kHz:96kHz)



THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(96kHz:48kHz)



THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(44.1kHz:192kHz)



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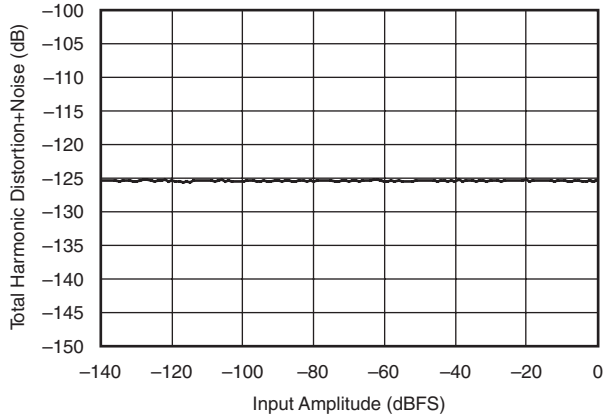
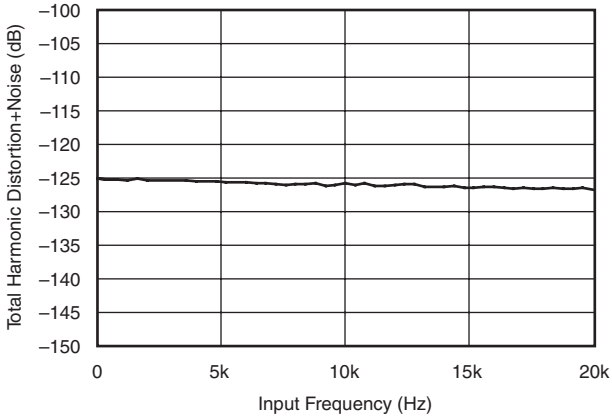
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

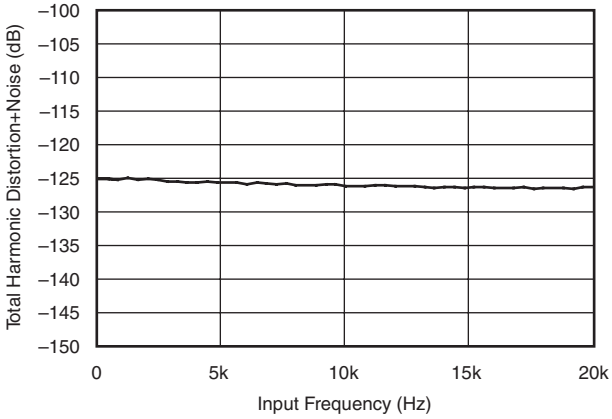
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(192kHz:44.1kHz)



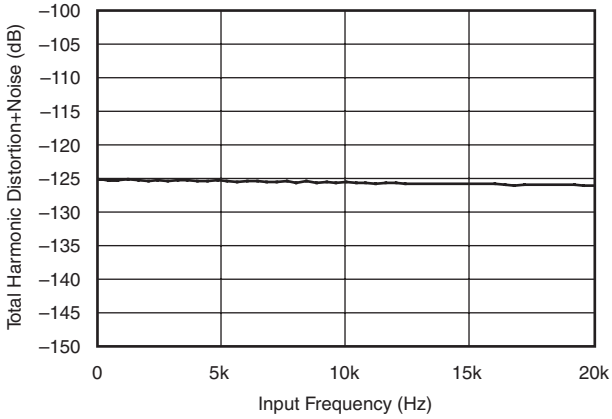
THD+N vs INPUT FREQUENCY WITH 0dBFS INPUT
(44.1kHz:48kHz)



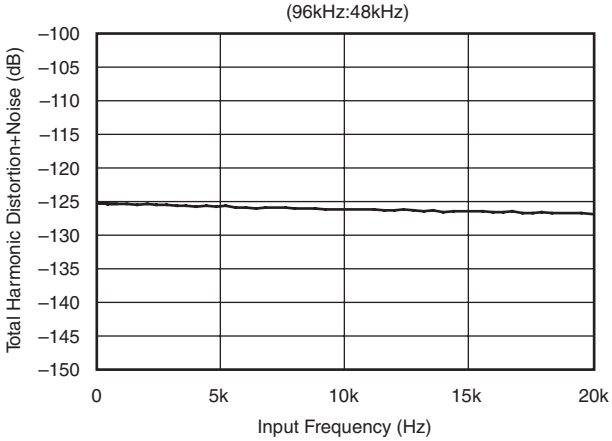
THD+N vs INPUT FREQUENCY WITH 0dBFS INPUT = 1kHz
(48kHz:44.1kHz)



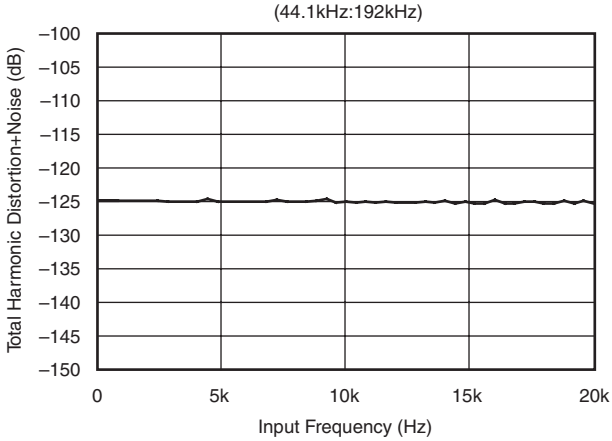
THD+N vs INPUT FREQUENCY WITH 0dBFS
(48kHz:96kHz)



THD+N vs INPUT FREQUENCY WITH 0dBFS
(96kHz:48kHz)



THD+N vs INPUT FREQUENCY WITH 0dBFS
(44.1kHz:192kHz)



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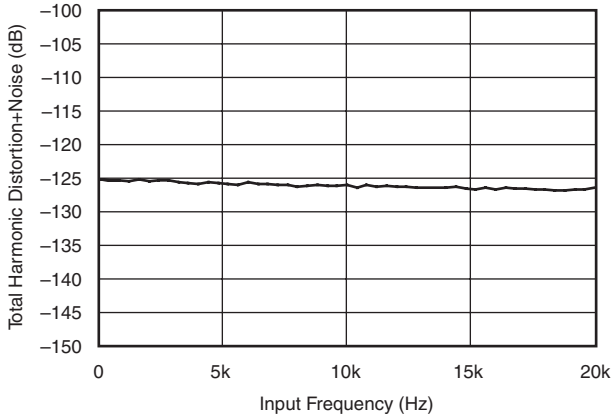
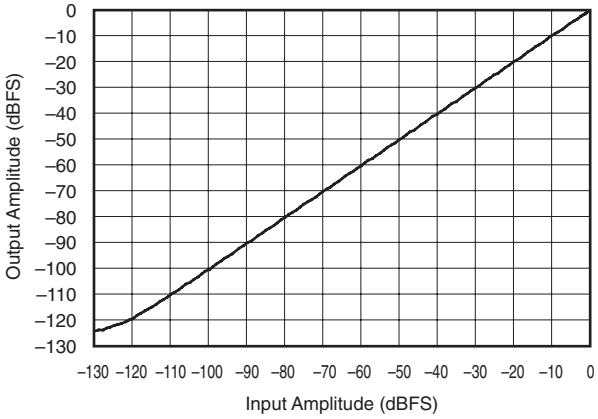
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

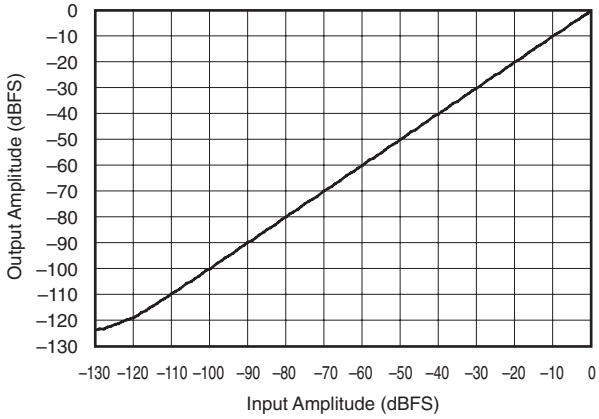
THD+N vs INPUT FREQUENCY WITH 0dBFS
(192kHz:44.1kHz)



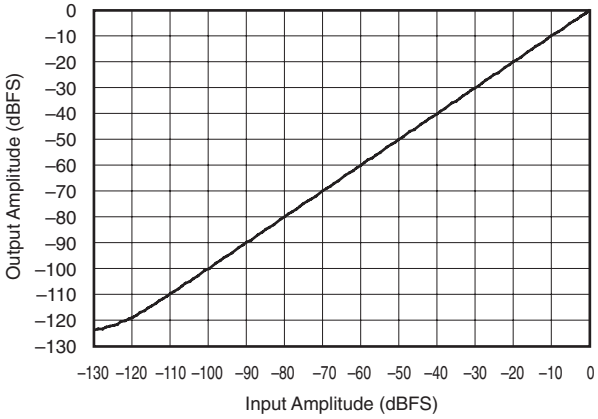
LINEARITY with f_{IN} = 200Hz
(44.1kHz:48kHz)



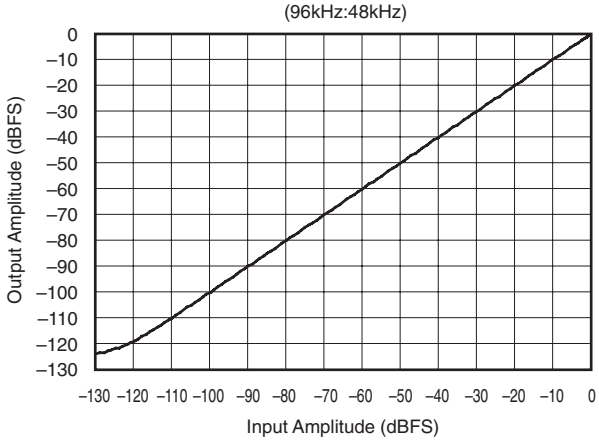
LINEARITY with f_{IN} = 200Hz
(48kHz:44.1kHz)



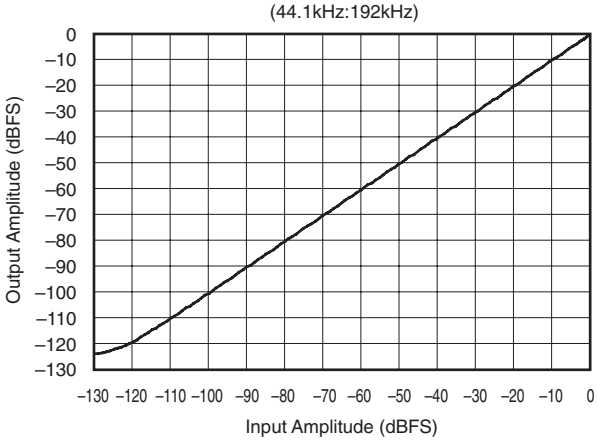
LINEARITY with f_{IN} = 200Hz
(48kHz:96kHz)



LINEARITY with f_{IN} = 200Hz
(96kHz:48kHz)



LINEARITY with f_{IN} = 200Hz
(44.1kHz:192kHz)



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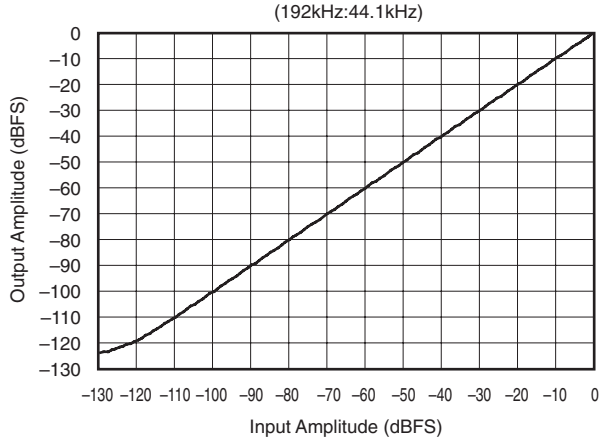
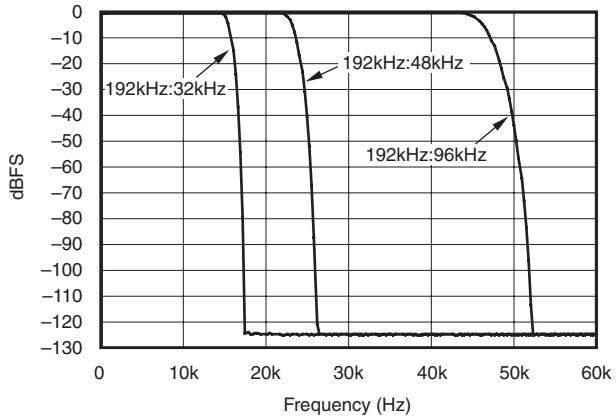
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V (unless otherwise noted)

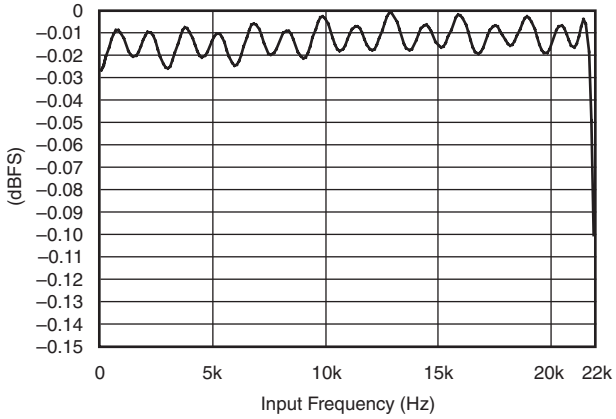
LINEARITY with f_{IN} = 200Hz
(192kHz:44.1kHz)



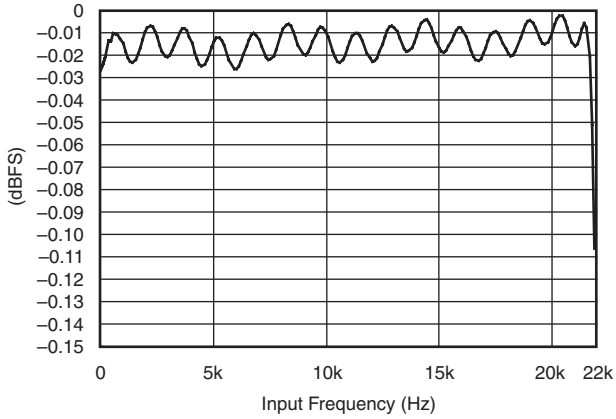
FREQUENCY RESPONSE with 0dBFS INPUT



PASS BAND RIPPLE
(48k:48k)



PASS BAND RIPPLE
(192k:48k)



DETAILED DESCRIPTION

The SRC4190 is an asynchronous sample rate converter (ASRC) designed for professional audio applications. Operation at input and output sampling frequencies up to 212 kHz is supported, with an input/output sampling ratio range of 16:1 to 1:16. Excellent dynamic range and Total Harmonic Distortion + Noise (THD+N) are achieved by employing high performance and linear phase digital filtering. Digital filtering options allow for lower group delay processing.

The audio input and output ports support standard audio data formats, as well as a TDM interface mode. Word lengths of 24, 20, 18, and 16 bits are supported. Both ports may operate in slave mode, deriving their word and bit clocks from external input and output devices. Alternatively, one port may operate in master mode while the other remains in slave mode. In master mode, the LRCK and BCK clocks are derived from the reference clock input, RCKI. The flexible configuration of the input and output ports allows connection to a wide variety of audio data converters, interface devices, digital signal processors, and programmable logic.

A bypass mode is included, which allows audio data to be passed directly from the input port to the output port, bypassing the ASRC function. The bypass option is useful for passing through encoded or compressed audio data, or nonaudio control or status data.

A soft mute function is available providing artifact-free operation while muting the audio output signal. The mute attenuation is typically –128 dB.

Functional Block Diagram

Figure 1 shows a functional block diagram of the SRC4190. Audio data is received at the input port, clocked by either the audio data source in Slave mode or by the SRC4190 in Master mode. The output port data is clocked by either the audio data source in Slave mode, or by the SRC4190 in Master mode. The input data is passed through interpolation filters which up-sample the data, which is then passed on to the re-sampler. The rate estimator compares the input and output sampling frequencies by comparing LRCKI, LRCKO, and a reference clock. The results include an offset for the FIFO pointer and the coefficients needed for re-sampling function.

The output of the re-sampler is then passed on to the decimation filter. The decimation filter performs down-sampling and anti-alias filtering functions.

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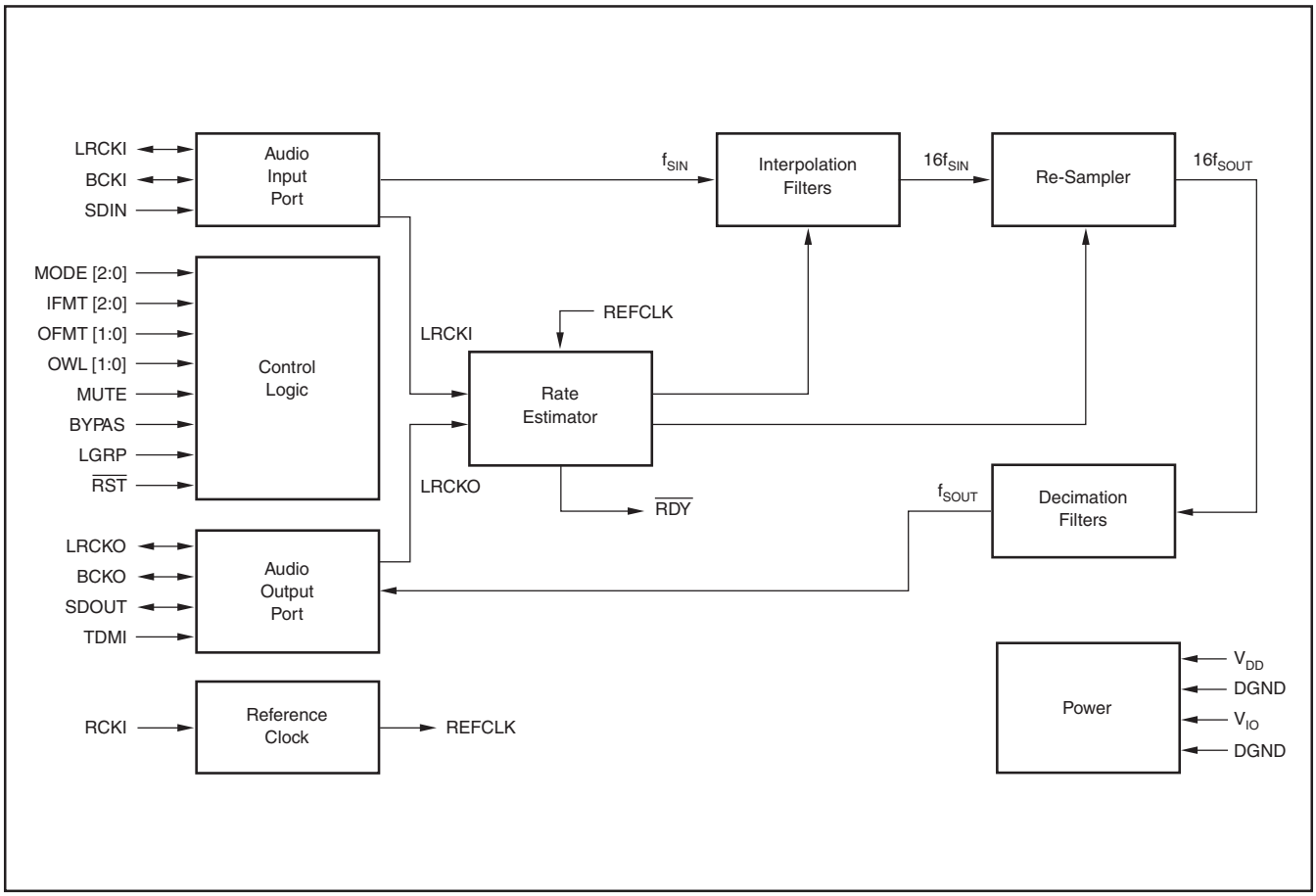

Figure 1. Functional Block Diagram

Reference Clock

The SRC4190 requires a reference clock for operation. The reference clock is applied at the RCKI input, pin 2. Figure 2 illustrates the reference clock connections and requirements for the SRC4190. The reference clock may operate at $128f_S$, $256f_S$, or $512f_S$, where f_S is the input or output sampling frequency. The maximum external reference clock input frequency is 50 MHz.

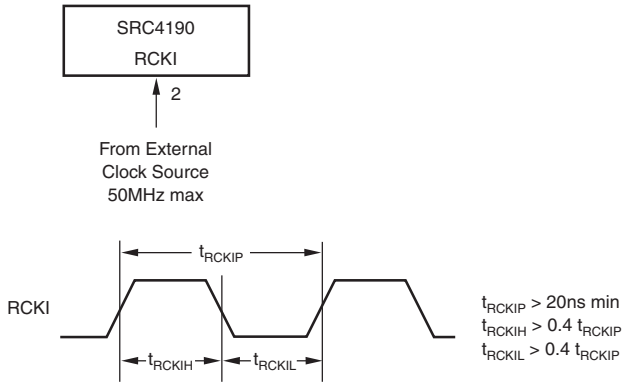

Figure 2. Reference Clock Input Connections and Timing Requirements

Reset and Power Down Operation

The SRC4190 may be reset using the $\overline{RST}$ input (pin 13). There is no internal power on reset, so the user should force a reset sequence after power up in order to initialize the device. In order to force a reset, the reference clock input must be active, with an external clock source supplying a valid reference clock signal (see Figure 2). The user must assert $\overline{RST}$ low for a minimum of 500 ns and then bring $\overline{RST}$ high again to force a reset. Figure 3 shows the reset timing for the SRC4190.

The SRC4190 also supports a power-down mode. Powerdown mode may be set by holding the $\overline{RST}$ input low.

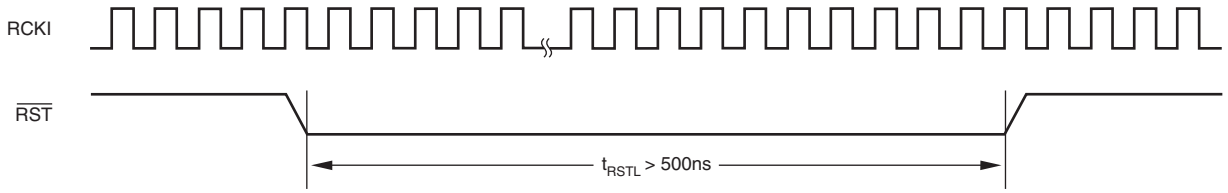

Figure 3. Reset Pulse Width Requirement

Audio Port Modes

The SRC4190 supports seven serial port modes, which are shown in Table 1. The audio port mode is selected using the MODE0 (pin 26), MODE1 (pin 27), and MODE2 (pin 28) inputs.

In slave mode, the port LRCK and BCK clocks are configured as inputs, and receive their clocks from an external audio device. In master mode, the LRCK and BCK clocks are configured as outputs, being derived from the reference clock input (RCKI). Only one port can be set to master mode at any given time, as indicated in Table 1.

Table 1. Setting the Serial Port Modes

MODE2	MODE1	MODE0	SERIAL PORT MODE
0	0	0	Both input and output ports are slave mode
0	0	1	Output port is master mode with RCKI = $128f_S$
0	1	0	Output port is master mode with RCKI = $512f_S$
0	1	1	Output port is master mode with RCKI = $256f_S$
1	0	0	Both input and output ports are slave mode
1	0	1	Input port is master mode with RCKI = $128f_S$
1	1	0	Input port is master mode with RCKI = $512f_S$
1	1	1	Input port is master mode with RCKI = $256f_S$

Input Port Operation

The audio input port is a three-wire synchronous serial interface that may operate in either slave or master mode. The SDIN input (pin 4) is the serial audio data input. Audio data is input at this pin in one of three standard audio data formats: Philips I^2S, left justified, or right justified. The audio data word length may be up to 24 bits for I^2S and left justified formats, while the right justified format supports 16-, 18-, 20-, or 24-bit data. The data formats are shown in Figure 4, while critical timing parameters are shown in Figure 5 and listed in the Electrical Characteristics table.

The bit clock is either an input or output at BCKI (pin 5). In slave mode, BCKI is configured as an input pin, and may operate at rates from $32f_S$ to $128f_S$, with a minimum of one clock cycle per data bit. In master mode, BCKI operates at a fixed rate of $64f_S$.

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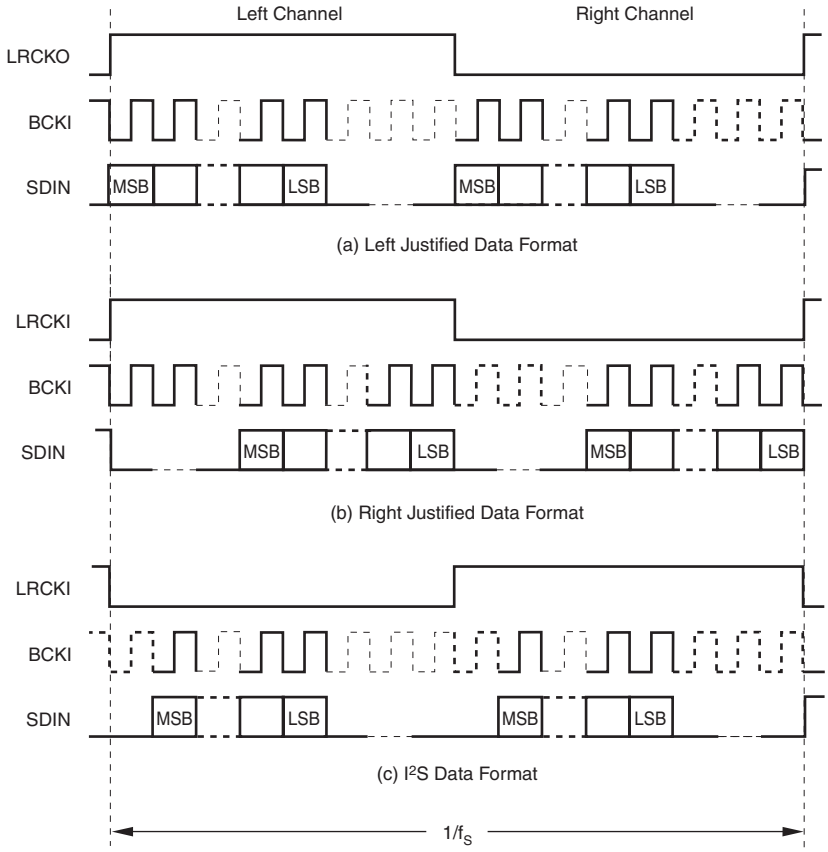

Figure 4. Input Data Formats

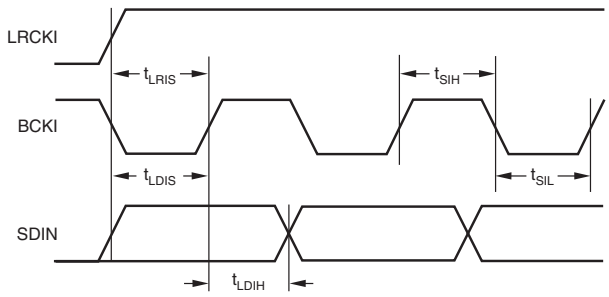

Figure 5. Input Port Timing

The left/right word clock, LRCKI (pin 6), may be configured as an input or output pin. In slave mode, LRCKI is an input pin, while in master mode LRCKI is an output pin. In either case, the clock rate is equal to f_S, the input sampling frequency. The LRCKI duty cycle is fixed to 50% for master mode operation.

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Table 2 illustrates data format selection for the input port. The IFMT0 (pin 10), IFMT1 (pin 11), and IFMT2 (pin 12) inputs are utilized to set the input port data format.

Table 2. Input Port Data Format Selection

IFMT2	IFMT1	IFMT0	INPUT PORT DATA FORMAT
0	0	0	24-bit left justified
0	0	1	24-bit I^2S
0	1	0	Unused
0	1	1	Unused
1	0	0	16-bit right justified
1	0	1	18-bit right justified
1	1	0	20-bit right justified
1	1	1	24-bit right justified

Output Port Operation

The audio output port is a four-wire synchronous serial interface that may operate in either slave or master mode. The SDOUT output (pin 23) is the serial audio data output. Audio data is output at this pin in one of four data formats: Philips I^2S, left justified, right justified, or TDM. The audio data word length may be 16, 18, 20, or 24 bits. For all word lengths, the data is triangular PDF dithered from the internal 28-bit data path. The data formats (with the exception of TDM mode) are shown in Figure 6, while critical timing parameters are shown in Figure 7 and listed in the Electrical Characteristics table. The TDM format and timing are shown in Figure 11 and Figure 12, respectively, while examples of standard TDM configurations are shown in Figure 13 and Figure 14.

The bit clock is either input or output at BCKO (pin 25). In slave mode, BCKO is configured as an input pin, and may operate at rates from $32f_S$ to $128f_S$, with a minimum of one clock cycle for each data bit. The exception is the TDM mode, where the BCKO must operate at $N \times 64f_S$, where N is equal to the number of SRC4190 devices included on the TDM interface. In master mode, BCKO operates at a fixed rate of $64f_S$ for all data formats except TDM, where BCKO operates at the reference clock (RCKI) frequency. Additional information regarding TDM mode operation is included in the *Application Information* section of this data sheet.

The left/right word clock, LRCKO (pin 24), may be configured as an input or output pin. In slave mode, LRCKO is an input pin, while in master mode it is an output pin. In either case, the clock rate is equal to f_S, the output sampling frequency. The clock duty cycle is fixed to 50% for I^2S, left justified, and right justified formats in master mode. The LRCKO pulse width is fixed to 32 BCKO cycles for the TDM format in master mode.

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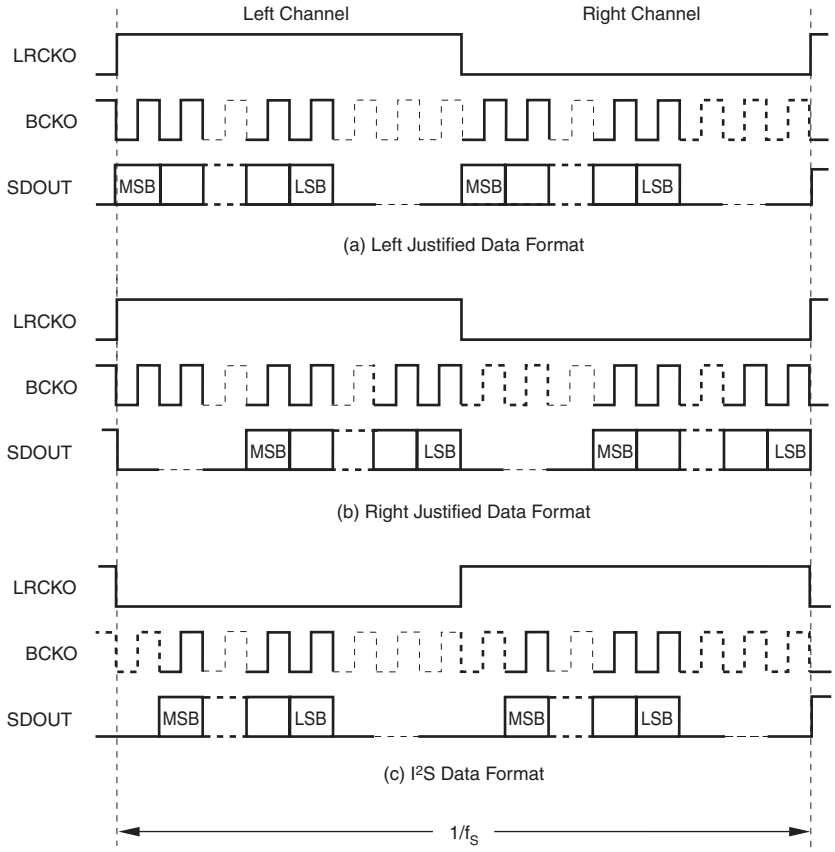

Figure 6. Output Data Formats

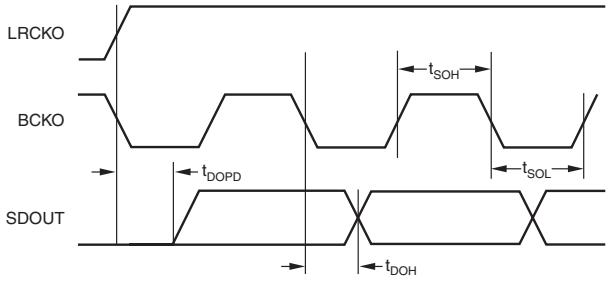

Figure 7. Output Port Timing

Table 3 illustrates data format selection for the output port. The OFMT0 (pin 19), OFMT1 (pin 18), OWL0 (pin 17), and OWL1 (pin 16) inputs are utilized to set the output port data format and word length.

Table 3. Output Port Data Format Selection

OFMT1	OFMT0	OUTPUT PORT DATA FORMAT
0	0	Left justified
0	1	I^2S
1	0	TDM
1	1	Right justified
OWL1	**OWL0**	**OUTPUT PORT DATA WORD LENGTH**
0	0	24 bits
0	1	20 bits
1	0	18 bits
1	1	16 bits

Bypass Mode

The SRC4190 includes a bypass function, which routes the input port data directly to the output port, bypassing the ASRC function. Bypass mode may be invoked by forcing the BYPAS input (pin 9) high. For normal ASRC operation, the BYPAS pin should be set to 0.

No dithering is applied to the output data in bypass mode; digital attenuation and mute functions are also unavailable in this mode.

Soft Mute Function

The soft mute function of the SRC4190 may be invoked by forcing the MUTE input (pin 14) high. The Soft mute function slowly attenuates the output signal level down to all zeroes plus ±4 LSB of dither. This provides an artifact-free muting of the audio output port.

Ready Output

The SRC4190 includes an active-low ready output named $\overline{\text{RDY}}$ (pin 15). This is an output from the rate estimator block, which indicates that the input-to-output sampling frequency ratio has been determined. The ready signal can be used as a flag or indicator output. The ready signal can also be connected to the active-high MUTE input (pin 14) to provide an auto-mute function, so that the output port is muted when the rate estimator is in transition.

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APPLICATION INFORMATION

This section of the data sheet provides practical applications information for hardware and systems engineers who will be designing the SRC4190 into end equipment.

Recommended Circuit Configuration

The typical connection diagram for the SRC4190 is shown in Figure 8. Recommended values for power-supply bypass capacitors are included. These capacitors should be placed as close to the IC package as possible.

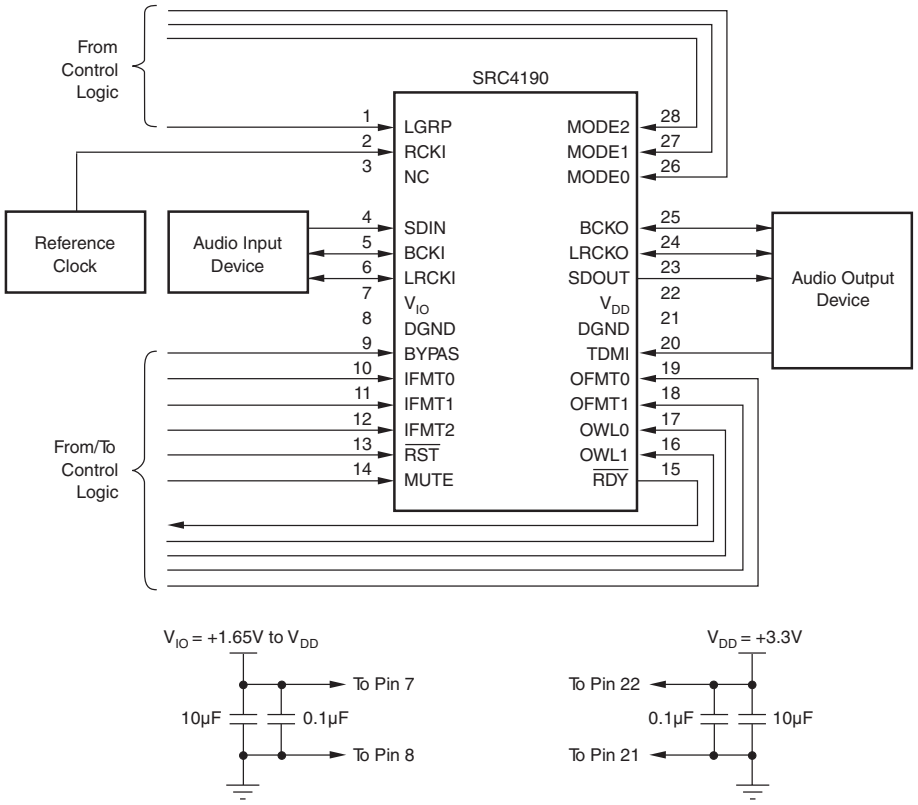

Figure 8. Typical Connection Diagram

Interfacing to Digital Audio Receivers and Transmitters

The SRC4190 input and output ports are designed to interface to a variety of audio devices, including receivers and transmitters commonly used for AES/EBU, S/PDIF, and CP1201 communications.

Texas Instruments manufactures the DIR1703 digital audio interface receiver and DIT4096/4192 digital audio transmitters to address these applications.

Figure 9 illustrates interfacing the DIR1703 to the SRC4190 input port. The DIR1703 operates from a single 3.3-V supply, which requires the V_{IO} supply (pin 7) for the SRC4190 to be set to 3.3 V for interface compatibility.

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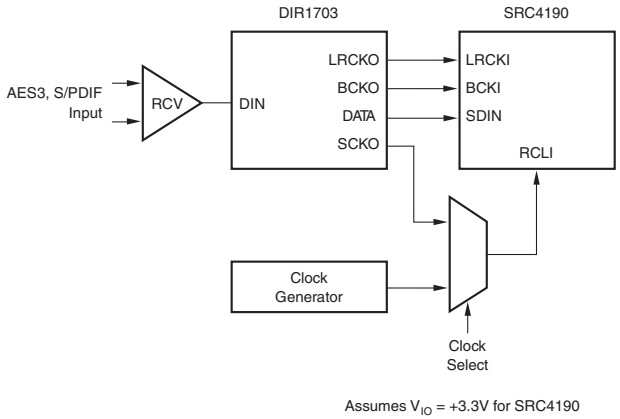

Figure 9. Interfacing the SRC4190 to the DIR1703 Digital Audio Interface Receiver

Figure 10 shows the interface between the SRC4190 output port and the DIT4096 or DIT4192 audio serial port. Once again, the V_{IO} supplies for both the SRC4190 and DIT4096/4192 are set to 3.3 V for compatibility.

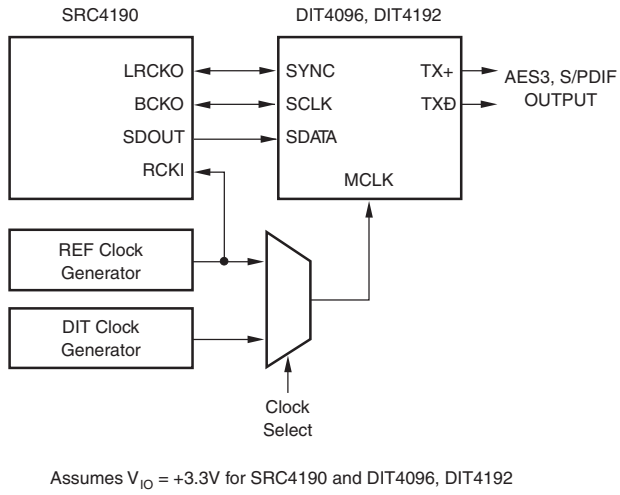

Figure 10. Interfacing the SRC4190 to the DIT4096/4192 Digital Audio Interface Transmitter

Like the SRC4190 output port, the DIT4096 and DIT4192 audio serial port may be configured as a Master or Slave. In cases where the SRC4190 output port is set to Master mode, it is recommended to use the reference clock source (RCKI) as the master clock source (MCLK) for the DIT4096/4192, to ensure that the transmitter is synchronized to the SRC4190 output port data.

TDM Applications

The SRC4190 supports a TDM output mode, which allows multiple devices to be daisy-chained together to create a serial frame. Each device occupies one sub-frame within a frame, and each sub-frame carries two channels (Left followed by Right). Each sub-frame is 64 bits long, with 32 bits allotted for each channel. The audio data for each channel is left justified within the allotted 32 bits. Figure 11 illustrates the TDM frame format, while Figure 12 shows the TDM input timing parameters, which are listed in the Electrical Characteristics table of this data sheet.

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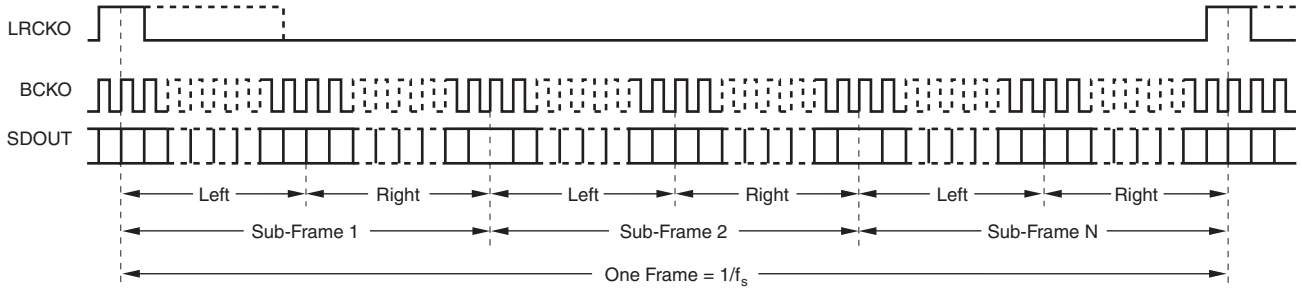

N = Number of Daisy-Chained Devices
One Sub-Frame contains 64 bits, with 32 bits per channel.
For each channel, the audio data is Left Justified, MSB first format, with the word length determined by the OWL[1:0] pins/bits.

Figure 11. TDM Frame Format

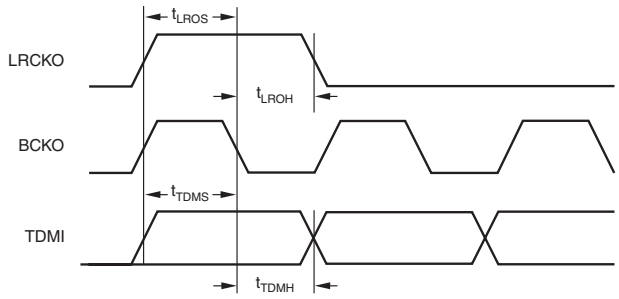

Figure 12. TDM Input Timing

The frame rate is equal to the output sampling frequency, f_S. The BCKO frequency for the TDM interface is N × 64f_S, where N is the number of devices included in the daisy chain. For Master mode, the output BCKO frequency is fixed to the reference clock (RCKI) input frequency. The number of devices that can be daisy-chained in TDM mode is dependent upon the output sampling frequency and the BCKO frequency, leading to the following numerical relationship:

Number of daisy-chained devices = (f_{BCKO} / f_S) / 64

Where:

f_{BCKO} = Output port bit clock (BCKO), 27.136 MHz maximum

f_S = Output port sampling (or LRCKO) frequency, 212 kHz maximum

This relationship holds true for both slave and master modes.

Figure 13 and Figure 14 show typical connection schemes for the TDM mode. Although the TMS320C671x DSP family is shown as the audio processing engine in these figures, other TI digital signal processors with a multi-channel buffered serial port (McBSPTM) may also function with this arrangement. Interfacing to processors from other manufacturers is also possible. See Figure 7 in this data sheet, along with the equivalent serial port timing diagrams shown in the DSP data sheet, to determine compatibility.

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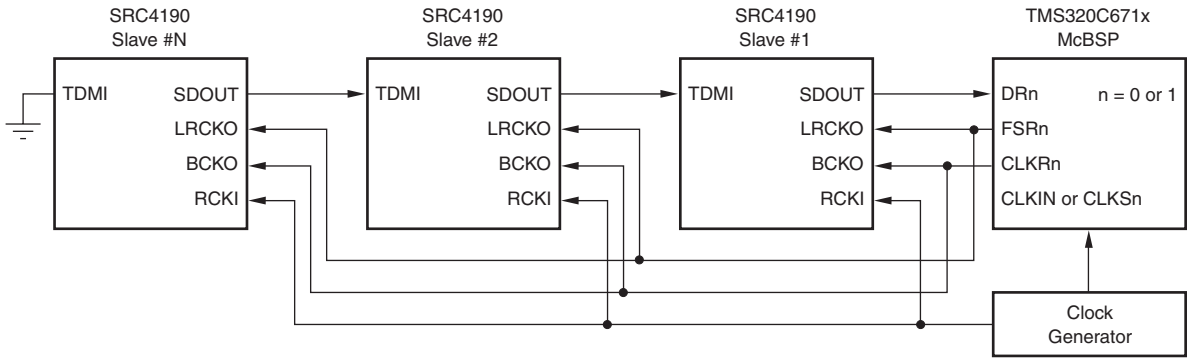

Figure 13. TDM Interface Where All Devices are Slaves

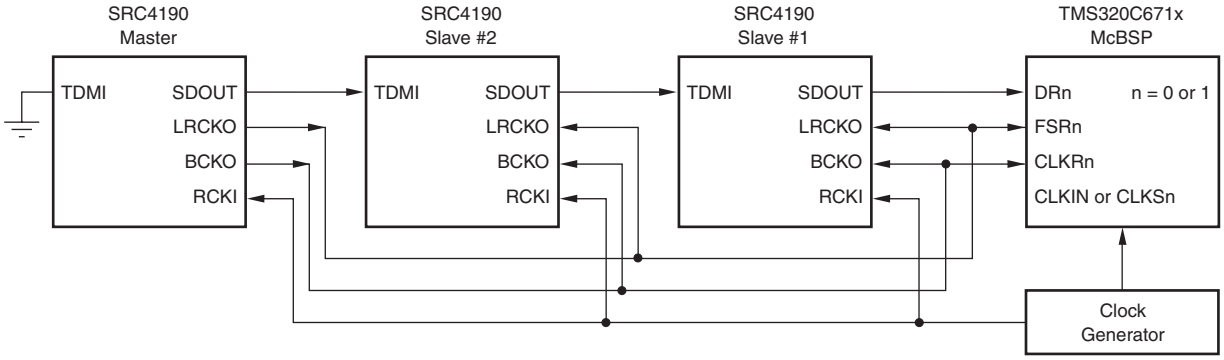

Figure 14. TDM Interface Where One Device is Master to Multiple Slaves

Pin Compatibility With the Analog Devices AD1895 and AD1896

The SRC4190 is pin-compatible and function-compatible with the AD1895 and AD1896 when observing the guidelines indicated in the following paragraphs.

Power Supplies. To ensure compatibility, the V_{DD_IO} and V_{DD_CORE} supplies of the AD1895 and AD1896 must be set to 3.3 V, while the V_{IO} and V_{DD} supplies of the SRC4190 must be set to 3.3 V.

Pin 1 connection. For the AD1895, pin 1 is a no connect (NC) pin. For the SRC4190, pin 1 functions as the low group delay selection input and should not be left unconnected. Pin 1 must be connected to either digital ground or the V_{IO} supply, dependent upon the desired group delay.

Crystal Oscillator. The SRC4190 does not have an on-chip crystal oscillator. An external reference clock is required at the RCKI input (pin 2).

Reference Clock Frequency. The reference clock input frequency for the SRC4190 must be no higher than 30 MHz, in order to match the master clock frequency specification of the AD1895 and AD1896. In addition, the SRC4190 does not support the $768f_S$ reference clock rate.

Master Mode Maximum Sampling Frequency. When the input or output ports are set to Master mode, the maximum sampling frequency must be limited to 96 kHz in order to support the AD1895 and AD1896 specification. This is despite the fact that the SRC4190 supports a maximum sampling frequency of 212 kHz in Master mode. The user should consider building an option into the design to support the higher sampling frequency of the SRC4190.

Matched Phase Mode. Due to the internal architecture of the SRC4190, it does not require or support the matched phase mode of the AD1896. Given multiple SRC4190 devices, if all reference clock (RCKI) inputs are driven from the same clock source, the devices will be phase matched.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SRC4190IDBRQ1	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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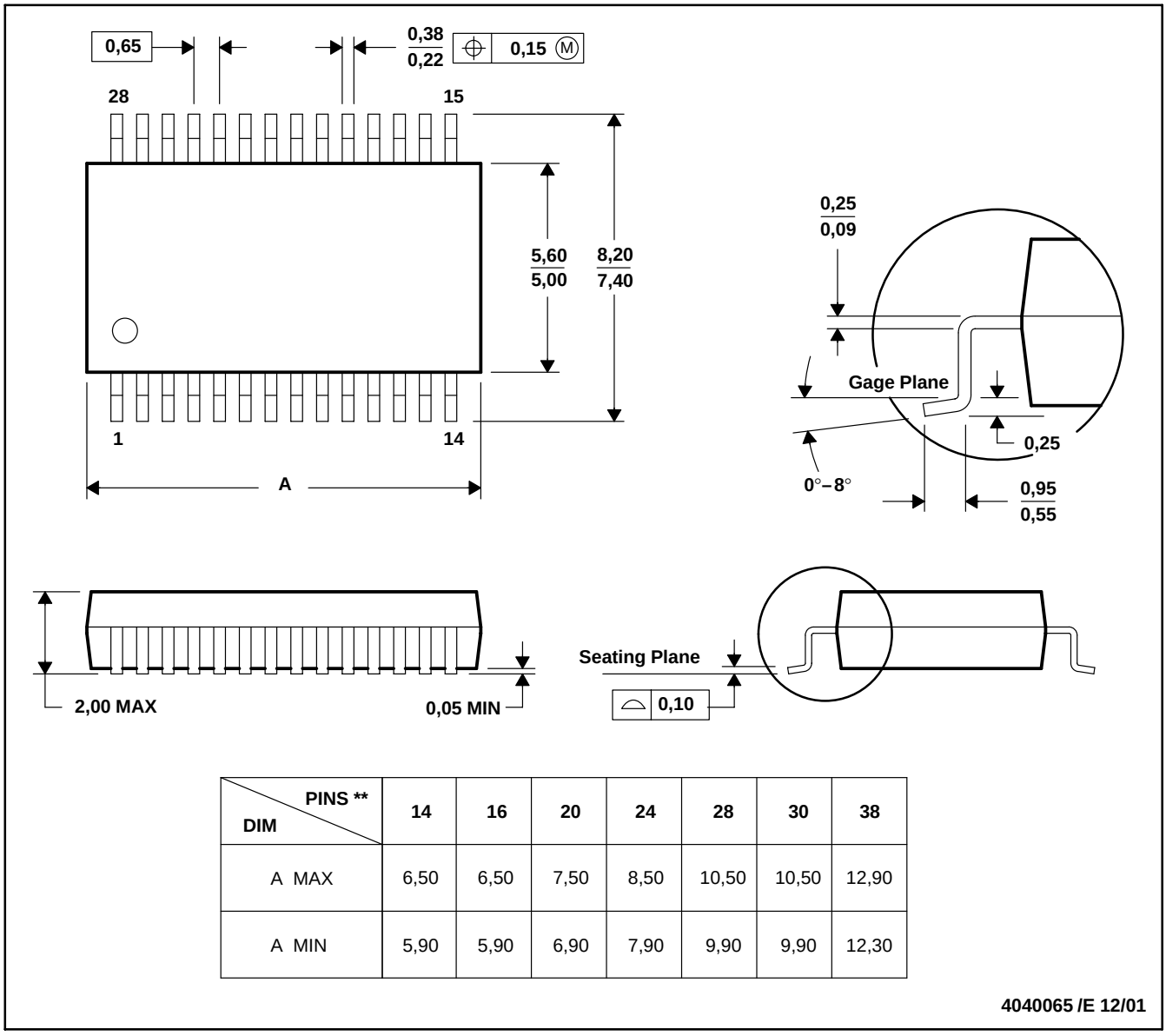
OTHER QUALIFIED VERSIONS OF SRC4190-Q1 :
- Catalog: SRC4190

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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