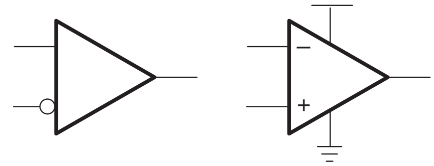
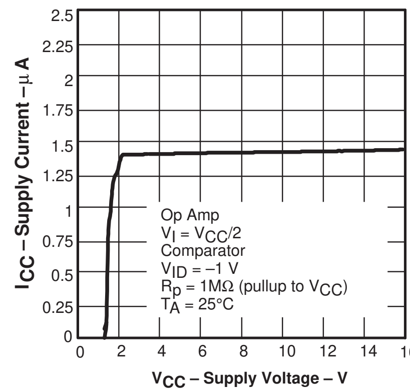
- **Micro-Power Operation . . . 1.4 μA**
- **Input Common-Mode Range Exceeds the Rails . . . –0.1 V to V_{CC} + 5 V**
- **Supply Voltage Range . . . 2.5 V to 16 V**
- **Rail-to-Rail Input/Output (Amplifier)**
- **Reverse Battery Protection Up to 18 V**
- **Gain Bandwidth Product . . . 5.5 kHz (Amplifier)**
- **Open-Drain CMOS Output Stage (Comparator)**
- **Specified Temperature Range**
  - **T_A = –40°C to 125°C . . . Industrial Grade**
- **Ultrasmall Packaging**
  - **8-Pin MSOP (TLV2302)**
- **Universal Op-Amp EVM (See the SLOU060 for More Information)**



SUPPLY CURRENT vs SUPPLY VOLTAGE



The TLV230x combines sub-micropower operational amplifier and comparator into a single package that produces excellent micropower signal conditioning with only 1.4 μA of supply current. This combination gives the designer more board space and reduces part counts in systems that require an operational amplifier and comparator. The low supply current makes it an ideal choice for battery-powered portable applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an over-current condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

The TLV230x's low supply current is coupled with extremely low input bias currents enabling them to be used with mega-ohm resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as 390 μV, CMRR of 90 dB and minimum open loop gain of 130 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 16 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V, and 15 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micropower microcontrollers available today including TI's MSP430.

All members are available in PDIP and SOIC with the duals (one op-amp and one comparator) in the small MSOP package, and the quads (two operational amplifiers and two comparators) in the TSSOP package.

A SELECTION OF OUTPUT COMPARATORS†

DEVICE	V_{CC} (V)	V_{IO} (μV)	I_{CC}/Ch (μA)	GBW (kHz)	SR (V/μs)	t_{PLH} (μs)	t_{PHL} (μs)	t_f (μs)	RAIL-TO-RAIL	OUTPUT STAGE
TLV230x	2.5 – 16	390	1.4‡	5.5	0.0025	55	30	5	I/O	OD
TLV270x	2.5 – 16	390	1.4‡	5.5	0.0025	55	30	5	I/O	PP
TLV240x	2.5 – 16	390	880	5.5	0.0025	—	—	—	I/O	—
TLV224x	2.5 – 12	600	1	5.5	0.002	—	—	—	I/O	—
TLV340x	2.5 – 16	250	0.47	—	—	55	30	5	I	OD
TLV370x	2.5 – 16	250	0.47	—	—	55	30	5	I	PP

† All specifications are typical values measured at 5 V.
‡ I_{CC} is specified as one op-amp and one comparator.

TLV2302 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	MSOP: MSOP† (DGK)	MSOP: SYMBOLS	PLASTIC DIP (P)
-40°C to 125°C	4000 µV	TLV2302ID	TLV2302IDGK	xxTIAQG	TLV2302IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2302IDR).

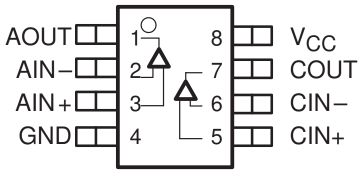
TLV2304 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE† (D)	TSSOP (PW)	PLASTIC DIP (N)
−40°C to 125°C	4000 µV	TLV2304ID	TLV2304IPW	TLV2304IN

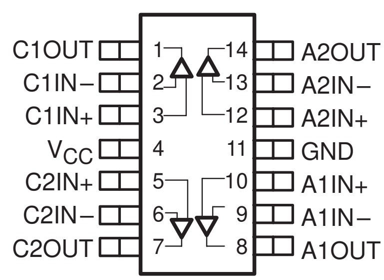
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2304IDR).

TLV230x PACKAGE PINOUTS

TLV2302
D, DGK, OR P PACKAGE
(TOP VIEW)



TLV2304
D, N, OR PW PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 17 V
Differential input voltage, V_{ID} . . . . V_{CC}
Input voltage range, V_I (see Notes 1 and 2) . . . . 0 to V_{CC} + 5 V
Input current range, I_I (any input) . . . . ±10 mA
Output current range, I_O . . . . ±10 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: I suffix . . . . –40°C to 125°C
Maximum junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND
2. Input voltage range is limited to 20 V max or V_{CC} + 5 V, whichever is smaller.

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.3	1022 mW	204.4 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	Single supply	2.5	16	V
	Split supply	±1.25	±8	
Common-mode input voltage range, V_{ICR}	Amplifier and comparator	–0.1	V_{CC}+5	V
Operating free-air temperature, T_A		–40	125	°C

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted)

amplifier dc performance

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, $R_S = 50\ \Omega$		25°C		390	4000	µV
				Full range			6000	
α_{VIO}	Offset voltage draft			25°C		3		µV/°C
CMRR	Common-mode rejection ratio	V_{IC} = 0 to V_{CC}, $R_S = 50\ \Omega$	V_{CC} = 2.7 V	25°C	55	73		dB
				Full range	52			
			V_{CC} = 5 V	25°C	60	80		
				Full range	55			
			V_{CC} = 15 V	25°C	66	90		
				Full range	60			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 2.7 V, $V_{O(pp)}$ = 1.5 V, R_L = 500 kΩ		25°C	130	400		V/mV
				Full range	30			
		V_{CC} = 5 V, $V_{O(pp)}$ = 3 V, R_L = 500 kΩ		25°C	300	1000		
				Full range	100			
		V_{CC} = 15 V, $V_{O(pp)}$ = 8 V, R_L = 500 kΩ		25°C	400	1400		
				Full range	120			
PSRR	Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{IC} = V_{CC}/2$ V, No load	V_{CC} = 2.7 to 5 V	25°C	90	120		dB
				Full range	85			
			V_{CC} = 5 to 15 V	25°C	94	120		
				Full range	90			

† Full range is –40°C to 125°C.

amplifier and comparator input characteristics

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
I_{IO}	Input offset current	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, R_p = 1 MΩ (pullup to V_{CC}), $R_S = 50\ \Omega$	25°C		25	250	pA
			0 to 70°C			300	
			Full range			500	
I_{IB}	Input bias current		25°C		100	500	pA
			0 to 70°C			550	
			Full range			1000	
$r_{i(d)}$	Differential input resistance		25°C		300		MΩ
$C_{i(c)}$	Common-mode input capacitance	f = 100 kHz	25°C		3		pF

† Full range is –40°C to 125°C.

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted) (continued)

amplifier output characteristics

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{IC} = V_{CC}/2$, I_{OH} = –50 µA	V_{CC} = 2.7 V	25°C	2.55	2.65		V
				Full range	2.5			
			V_{CC} = 5 V	25°C	4.85	4.95		
				Full range	4.8			
			V_{CC} = 15 V	25°C	14.85	14.95		
				Full range	14.8			
V_{OL}	Low-level output voltage	$V_{IC} = V_{CC}/2$, I_{OL} = 50 µA		25°C		180	260	mV
				Full range			300	
I_O	Output current	V_O = 0.5 V from rail		25°C		±200		µA

† Full range is –40°C to 125°C.

amplifier dynamic performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	R_L = 500 kΩ, C_L = 100 pF		25°C		5.5		kHz
SR	Slew rate at unity gain	$V_{O(pp)}$ = 0.8 V, R_L = 500 kΩ, C_L = 100 pF		25°C		2.5		V/ms
φM	Phase margin	R_L = 500 kΩ, C_L = 100 pF		25°C		60°		
	Gain margin					15		dB
t_s	Settling time	V_{CC} = 2.7 or 5 V, $V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 100 pF, R_L = 100 kΩ	0.1%	25°C		1.84		ms
		V_{CC} = 15 V, $V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 100 pF, R_L = 100 kΩ	0.1%			6.1		
			0.01%			32		
V_n	Equivalent input noise voltage	f = 0.1 to 10 Hz		25°C		5.3		μV_{pp}
		f = 100 Hz				500		$nV/\sqrt{Hz}$
I_n	Equivalent input noise current	f = 100 Hz		25°C		8		$fA/\sqrt{Hz}$

supply current

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{CC}	Supply current (one op-amp and one comparator)	R_p = No pullup, Output state high	V_{CC} = 2.7 V or 5 V	25°C		1.4		µA
			V_{CC} = 15 V	25°C		1.4	1.7	
				Full range			2.3	
	Reverse supply current	V_{CC} = –18 V, V_I = 0 V, V_O = open		25°C		50		nA

† Full range is –40°C to 125°C.

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted) (continued)

comparator dc performance

PARAMETER		TEST CONDITIONS†		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{CC}/2$, $R_S = 50\ \Omega$, $R_p = 1\ M\Omega$ (pullup to V_{CC})		25°C		250	5000	μV
				Full range			7000	
α_{VIO}	Offset voltage drift			25°C		3		μV/°C
CMRR	Common-mode rejection ratio	V_{IC} = 0 to V_{CC}, $R_S = 50\ \Omega$	V_{CC} = 2.7 V	25°C	55	72		dB
				Full range	50			
			V_{CC} = 5 V	25°C	60	76		
				Full range	55			
			V_{CC} = 15 V	25°C	65	88		
				Full range	60			
A_{VD}	Large-signal differential voltage amplification	$R_p = 1\ M\Omega$ (pullup to V_{CC})		25°C		1000		V/mV
PSRR	Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{IC} = V_{CC}/2$ V, No load	V_{CC} = 2.7 to 5 V	25°C	75	100		dB
				Full range	70			
			V_{CC} = 5 to 15 V	25°C	85	105		
				Full range	80			

† Full range is –40°C to 125°C.

comparator output characteristics

PARAMETER		TEST CONDITIONS†	T_A†	MIN	TYP	MAX	UNIT
I_{OZ}	High-impedance output leakage current	$V_{IC} = V_{CC}/2$, $V_O = V_{CC}$, V_{ID} = 1 V	25°C		50		pA
V_{OL}	Low-level output voltage	$V_{IC} = V_{CC}/2$, I_{OL} = 50 μA, V_{ID} = –1 V	25°C		80	200	mV
			Full range			300	

† Full range is –40°C to 125°C.

switching characteristics at recommended operating conditions, V_{CC} = 2.7 V, 5 V, 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$t_{(PLH)}$	Propagation delay time, low-to-high-level output	f = 10 kHz, V_{STEP} = 1 V, C_L = 10 pF, $R_p = 1\ M\Omega$ (pullup to V_{CC})	Overdrive = 2 mV	25°C		175		μs
			Overdrive = 10 mV			55		
			Overdrive = 50 mV			25		
$t_{(PHL)}$	Propagation delay time, high-to-low-level output		Overdrive = 2 mV	25°C		300		
			Overdrive = 10 mV			60		
			Overdrive = 50 mV			30		
t_f	Fall time	C_L = 10 pF		25°C		5		μs

NOTE: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IB}	Input bias current	vs Free-air temperature	3, 5, 7
		vs Common-mode input voltage	4, 6
I_{IO}	Input offset current	vs Free-air temperature	3, 5, 7
		vs Common-mode input voltage	4, 6
I_{CC}	Supply current	vs Supply voltage	8
		vs Free-air temperature	9
Amplifier			
CMRR	Common-mode rejection ratio	vs Frequency	10
V_{OH}	High-level output voltage	vs High-level output current	11, 13
V_{OL}	Low-level output voltage	vs Low-level output current	12, 14
$V_{O(PP)}$	Output voltage, peak-to-peak	vs Frequency	15
PSRR	Power supply rejection ratio	vs Frequency	16
	Voltage noise over a 10 Second Period		17
ϕ_m	Phase margin	vs Capacitive load	18
A_{VD}	Differential voltage gain	vs Frequency	19
	Phase	vs Frequency	19
	Gain bandwidth product	vs Supply voltage	20
SR	Slew rate	vs Free-air temperature	21
	Large signal follower pulse response		22
	Small signal follower pulse response		23
	Large signal inverting pulse response		24
	Small signal inverting pulse response		25
Comparator			
V_{OL}	Low-level output voltage	vs Low-level output current	26, 27
	Open collector leakage current	vs Free-air temperature	28
	Output fall time	vs Supply voltage	29
	Low-to-high level output response for various input overdrives		30, 31
	High-to-low level output response for various input overdrives		32, 33

AMPLIFIER AND COMPARATOR TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

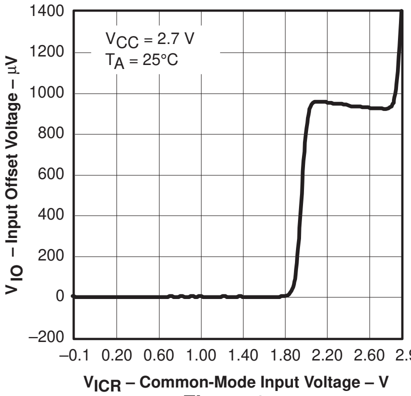


Figure 1

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

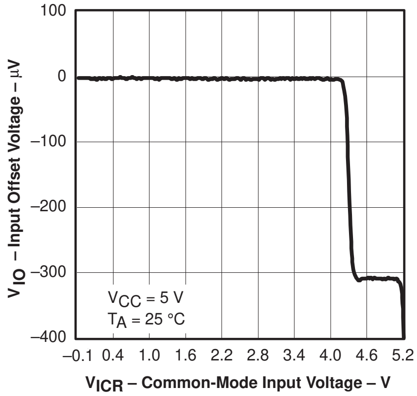


Figure 2

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

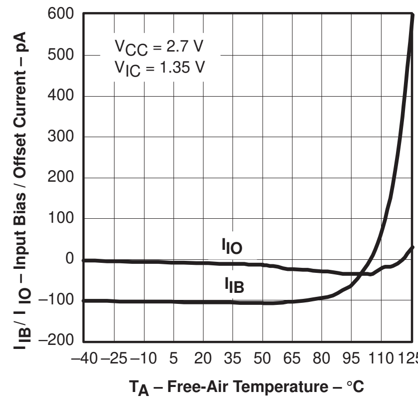


Figure 3

INPUT BIAS/OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

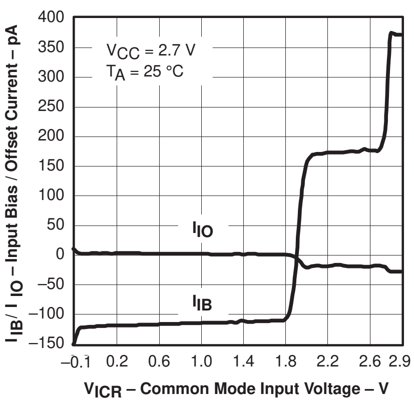


Figure 4

INPUT BIAS/OFFSET CURRENT vs FREE-AIR TEMPERATURE

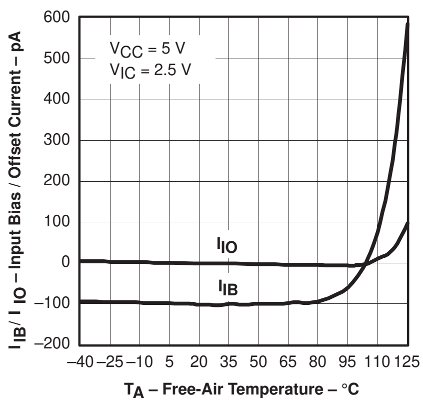


Figure 5

INPUT BIAS/OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

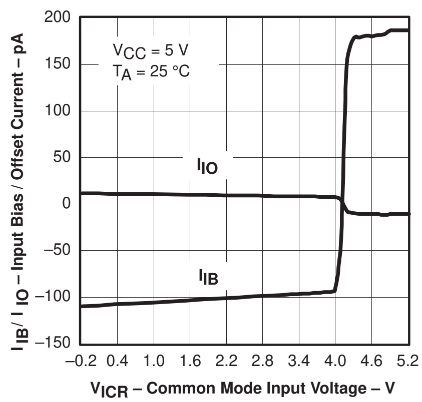


Figure 6

INPUT BIAS/OFFSET CURRENT vs FREE-AIR TEMPERATURE

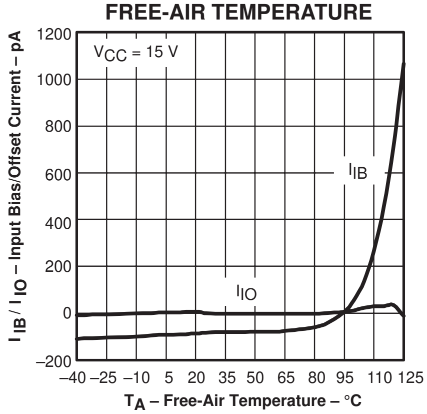


Figure 7

SUPPLY CURRENT vs SUPPLY VOLTAGE

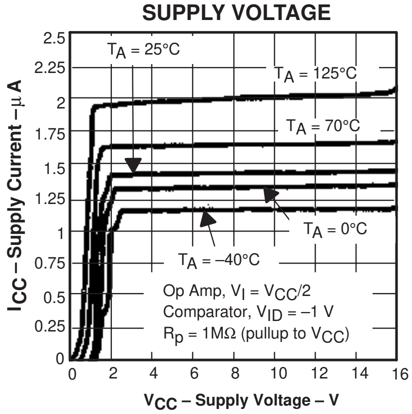


Figure 8

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

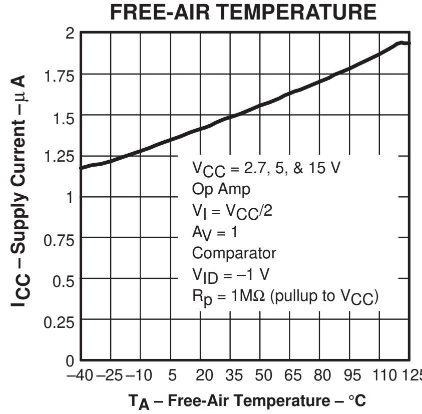


Figure 9

AMPLIFIER TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

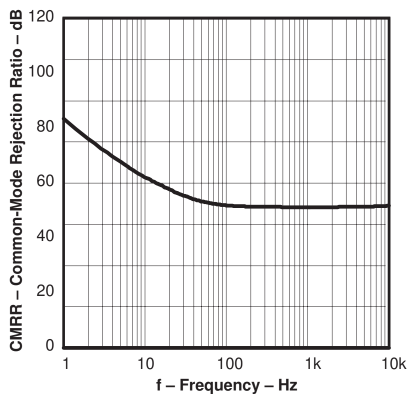


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

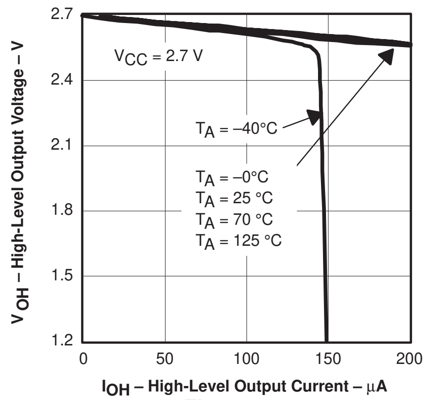


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

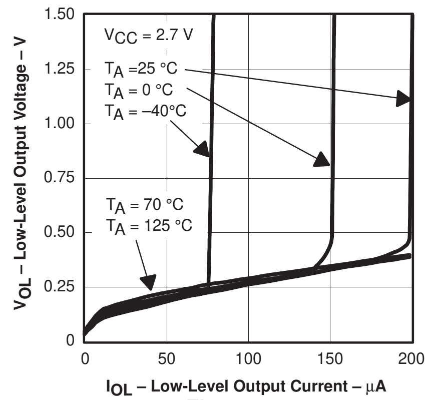


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

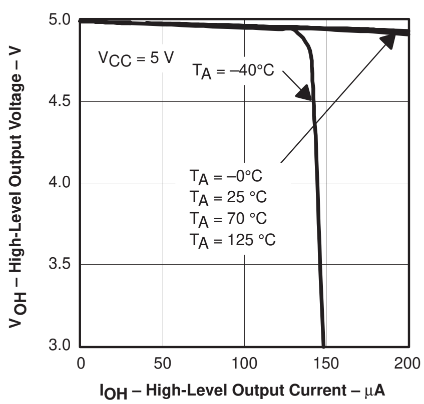


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

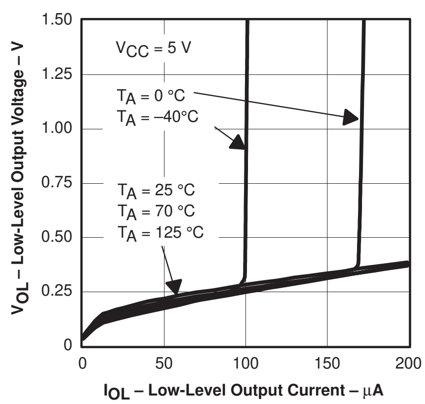


Figure 14

OUTPUT VOLTAGE PEAK-TO-PEAK vs FREQUENCY

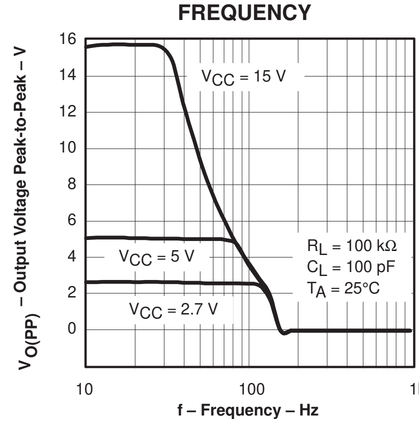


Figure 15

POWER SUPPLY REJECTION RATIO vs FREQUENCY

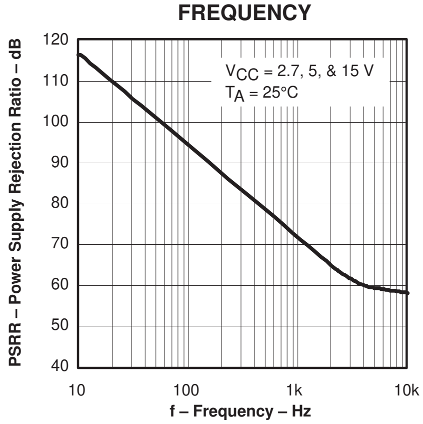


Figure 16

VOLTAGE NOISE OVER A 10 SECOND PERIOD

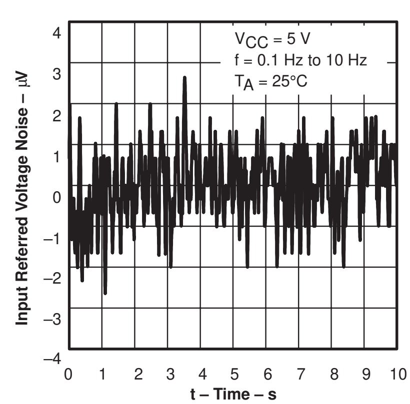


Figure 17

PHASE MARGIN vs CAPACITIVE LOAD

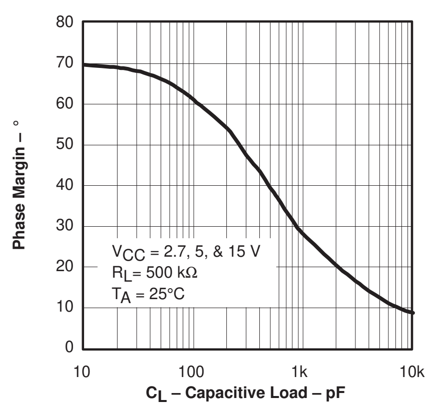


Figure 18

AMPLIFIER TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

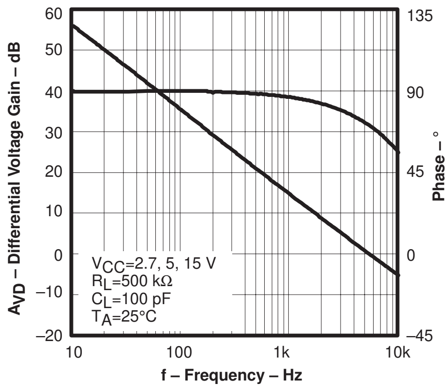


Figure 19

GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

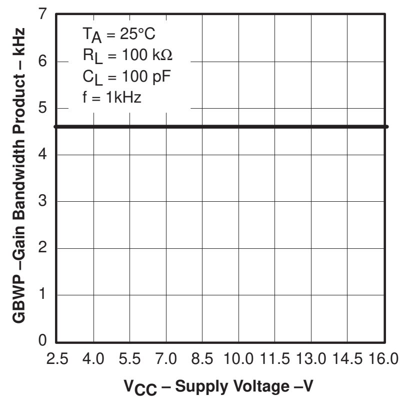


Figure 20

SLEW RATE vs FREE-AIR TEMPERATURE

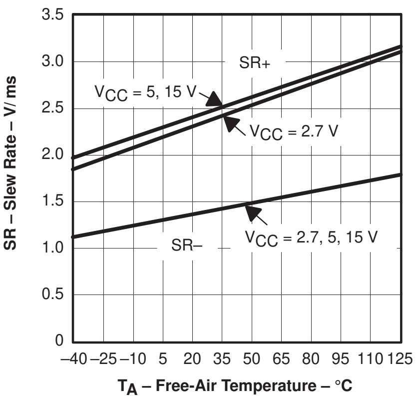


Figure 21

LARGE SIGNAL FOLLOWER PULSE RESPONSE

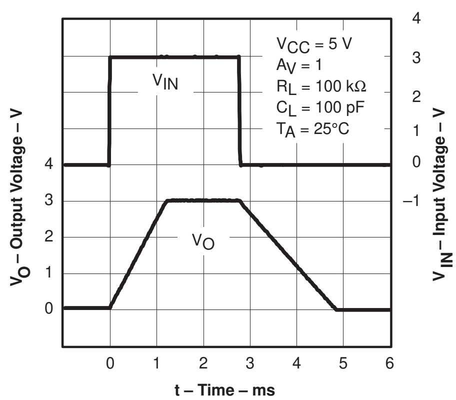


Figure 22

SMALL SIGNAL FOLLOWER PULSE RESPONSE

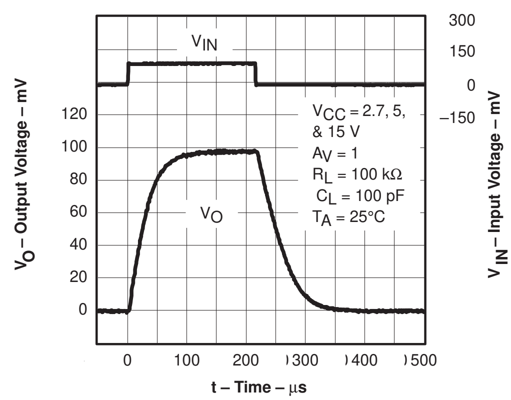


Figure 23

LARGE SIGNAL INVERTING PULSE RESPONSE

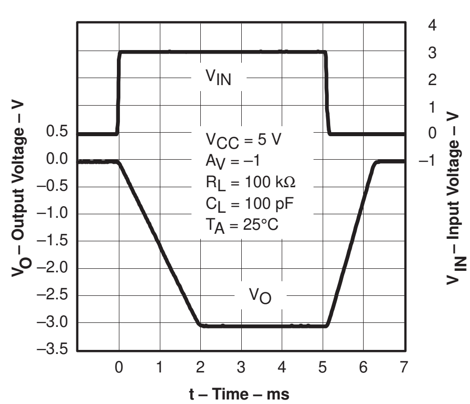


Figure 24

SMALL SIGNAL INVERTING PULSE RESPONSE

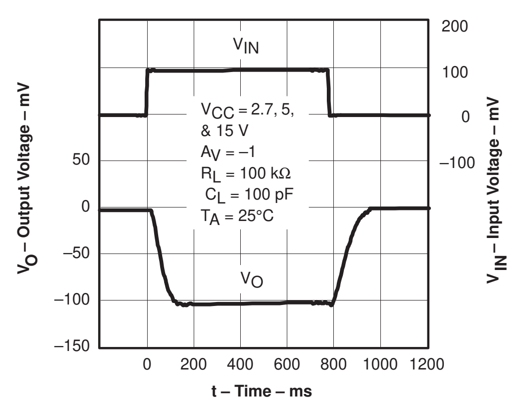


Figure 25

COMPARATOR TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

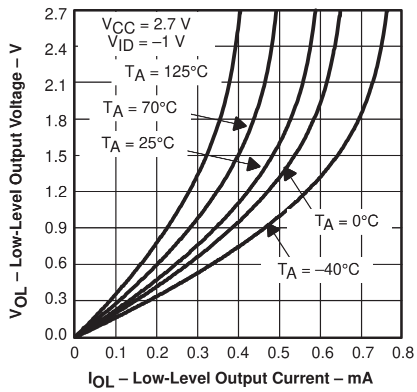


Figure 26

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

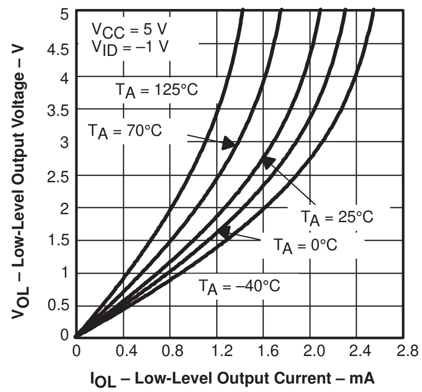


Figure 27

OPEN COLLECTOR LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

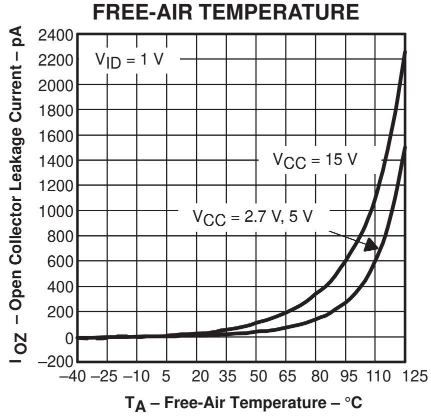


Figure 28

OUTPUT FALL TIME vs SUPPLY VOLTAGE

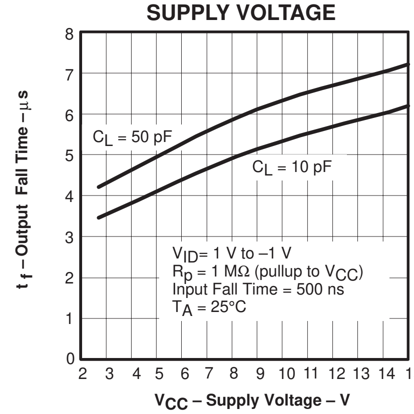


Figure 29

LOW-TO-HIGH LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

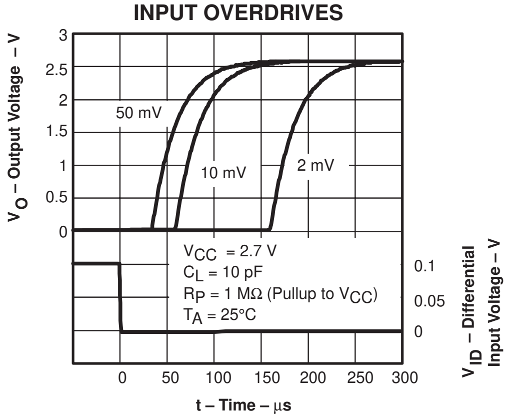


Figure 30

LOW-TO-HIGH LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

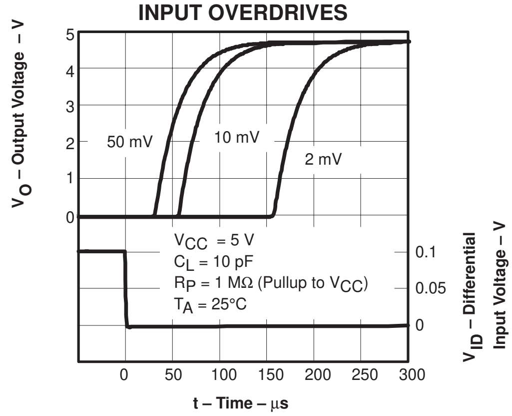


Figure 31

COMPARATOR TYPICAL CHARACTERISTICS

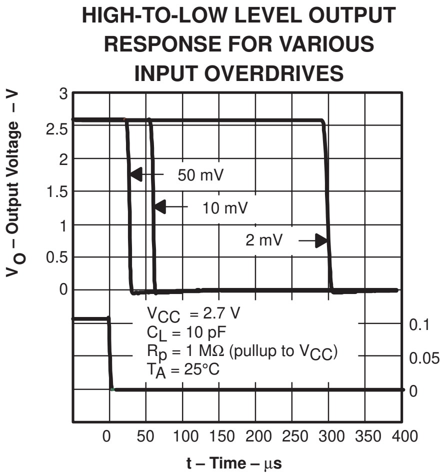


Figure 32

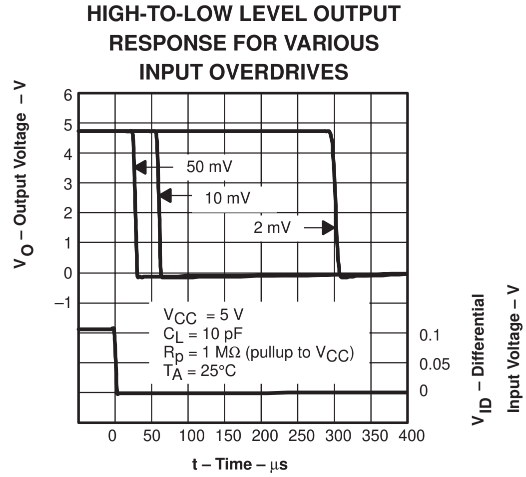


Figure 33

APPLICATION INFORMATION

reverse battery protection

The TLV2302/4 is protected against reverse battery voltage up to 18 V. When subjected to reverse battery condition, the supply current is typically less than 100 nA at 25°C (inputs grounded and outputs open). This current is determined by the leakage of six Schottky diodes and will therefore increase as the ambient temperature increases.

When subjected to reverse battery conditions and negative voltages applied to the inputs or outputs, the input ESD structure will turn on—this current should be limited to less than 10 mA. If the inputs or outputs are referred to ground, rather than midrail, no extra precautions need be taken.

common-mode input range

The TLV2302/4 has rail-rail input and outputs. For common-mode inputs from –0.1 V to V_{CC} – 0.8 V a PNP differential pair will provide the gain.

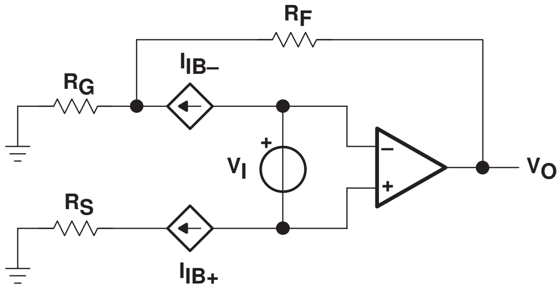
For inputs between V_{CC} – 0.8 V and V_{CC}, two NPN emitter followers buffering a second PNP differential pair provide the gain. This special combination of NPN/PNP differential pair enables the inputs to be taken 5 V above the rails; because as the inputs go above V_{CC}, the NPNs switch from functioning as transistors to functioning as diodes. This will lead to an increase in input bias current. The second PNP differential pair continues to function normally as the inputs exceed V_{CC}.

The TLV2302/4 has a negative common-input range that exceeds ground by 100 mV. If the inputs are taken much below this, reduced open loop gain will be observed with the ultimate possibility of phase inversion.

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage.

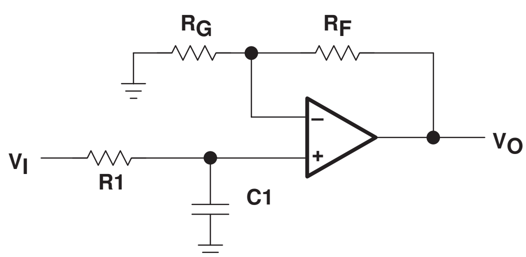


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 34. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 35).

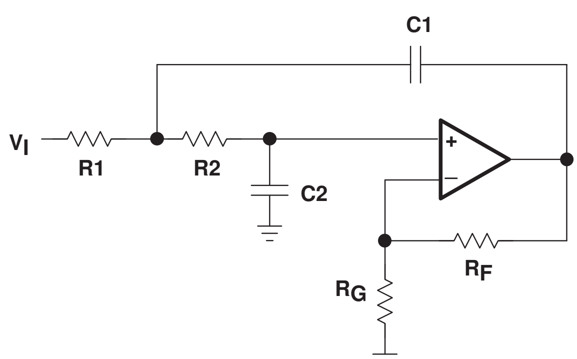


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 35. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 36. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV230x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

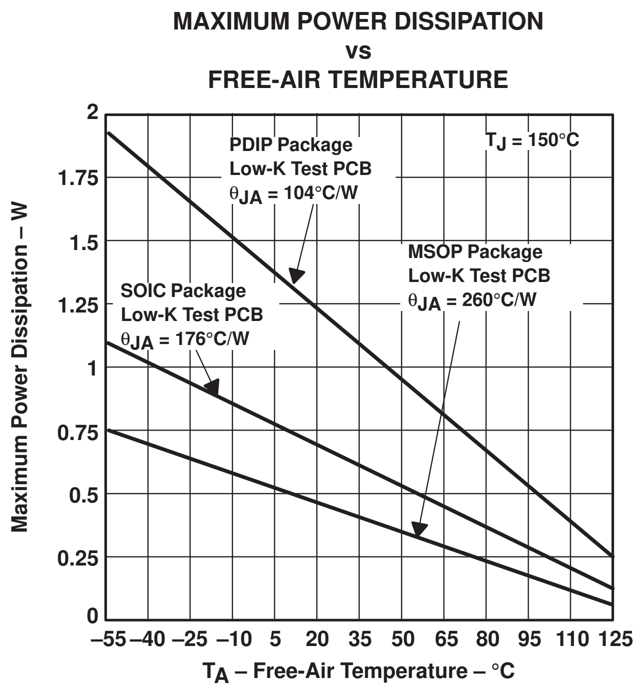
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 37 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV230x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 37. Maximum Power Dissipation vs Free-Air Temperature

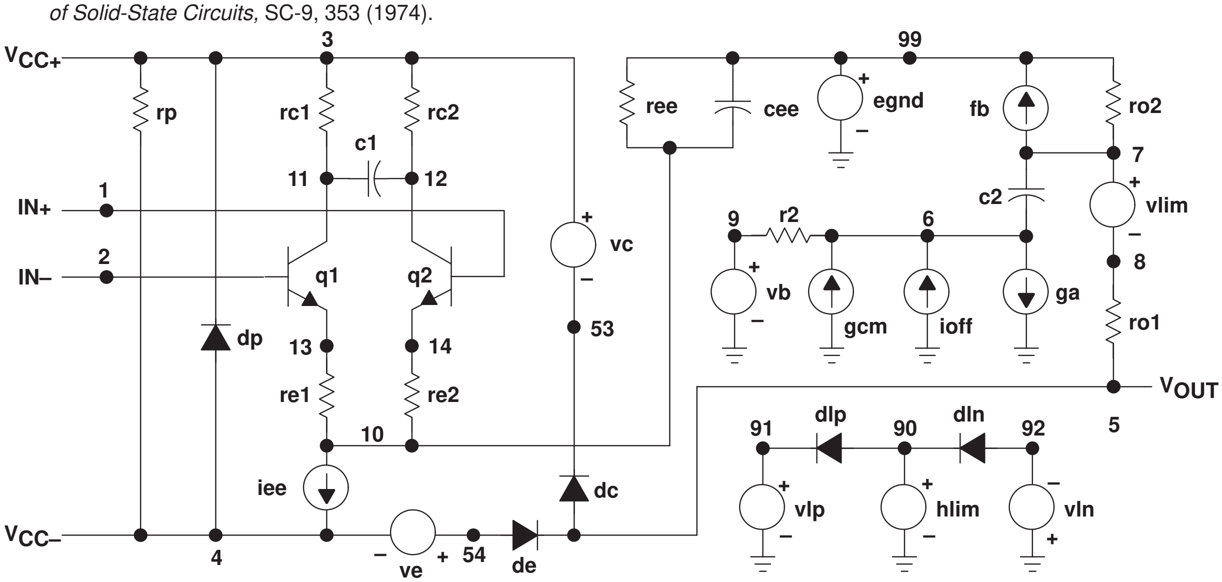
APPLICATION INFORMATION

amplifier macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 38 are generated using the TLV230x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 3: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.subckt 230X_5V–X  1 2 3 4 5
 *
 c1     11  12  9.8944E–12
 c2     6   7   30.000E–12
 cee    10  99  8.8738E–12
 dc     5   53  dy
 de     54  5   dy
 dlp    90  91  dx
 dln    92  90  dx
 dp     4   3   dx
 egnd   99  0   poly(2) (3,0) (4,0) 0 .5 .5
 fb     7   99  poly(5) vb vc ve vlp vln 0 61.404E6 –1E3 1E3 61E6 –61E6
 ga     6   0   11 12 1.0216E–6
 gcm    0   6   10 99 10.216E–12
 iee    10  4   dc 54.540E–9
 ioff   0   6   dc 5e–12
 hlim   90  0   vlim 1K
 q1     11  2   13 qx1
 q2     12  1   14 qx2
 r2     6   9   100.00E3
 rc1    3   11  978.81E3
 rc2    3   12  978.81E3
 re1    13  10  30.364E3
 re2    14  10  30.364E3
 ree    10  99  3.6670E9
 ro1    8   5   10
 ro2    7   99  10
 rp     3   4   1.4183E6
 vb     9   0   dc  0
 vc     3   53  dc  .88315
 ve     54  4   dc  .88315
 vlim   7   8   dc  0
 vlp    91  0   dc  540
 vln    0   92  dc  540
.model  dx   D(Is=800.00E–18)
.model  dy   D(Is=800.00E–18 Rs=1m Cjo=10p)
.model  qx1  NPN(Is=800.00E–18 Bf=27.270E21)
.model  qx2  NPN(Is=800.0000E–18 Bf=27.270E21)
.ends
```

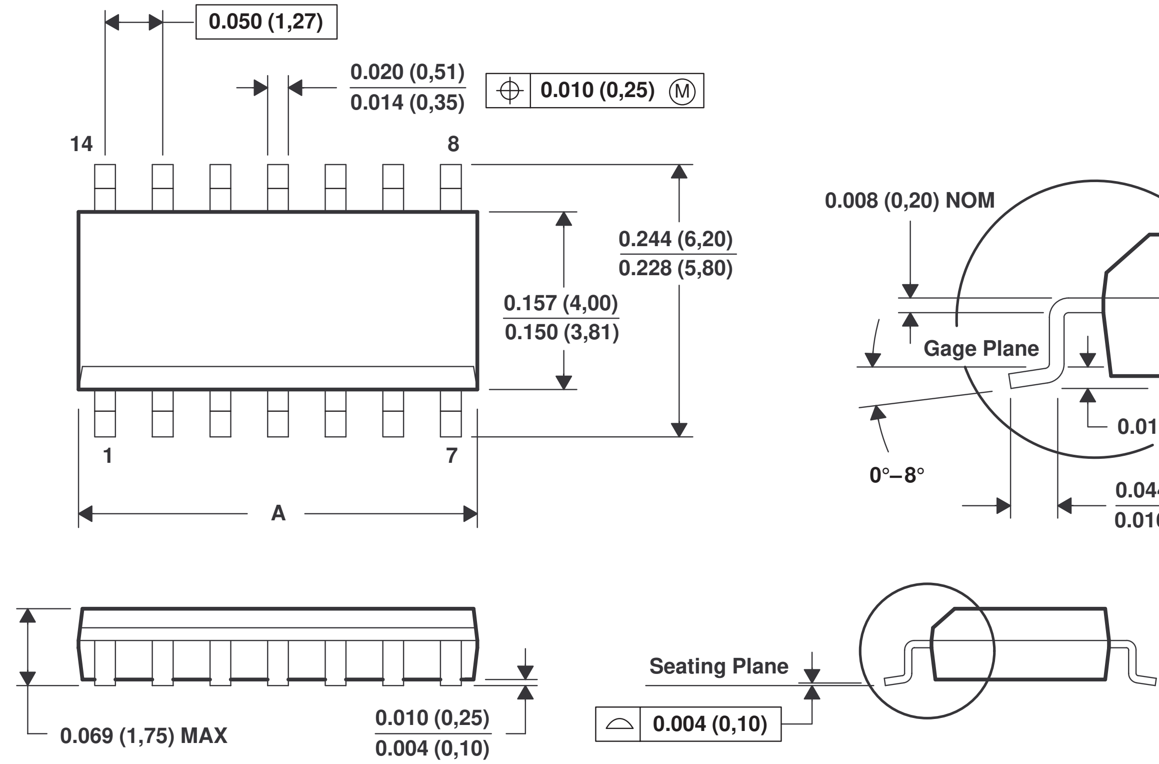
Figure 38. Boyle Macromodels and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



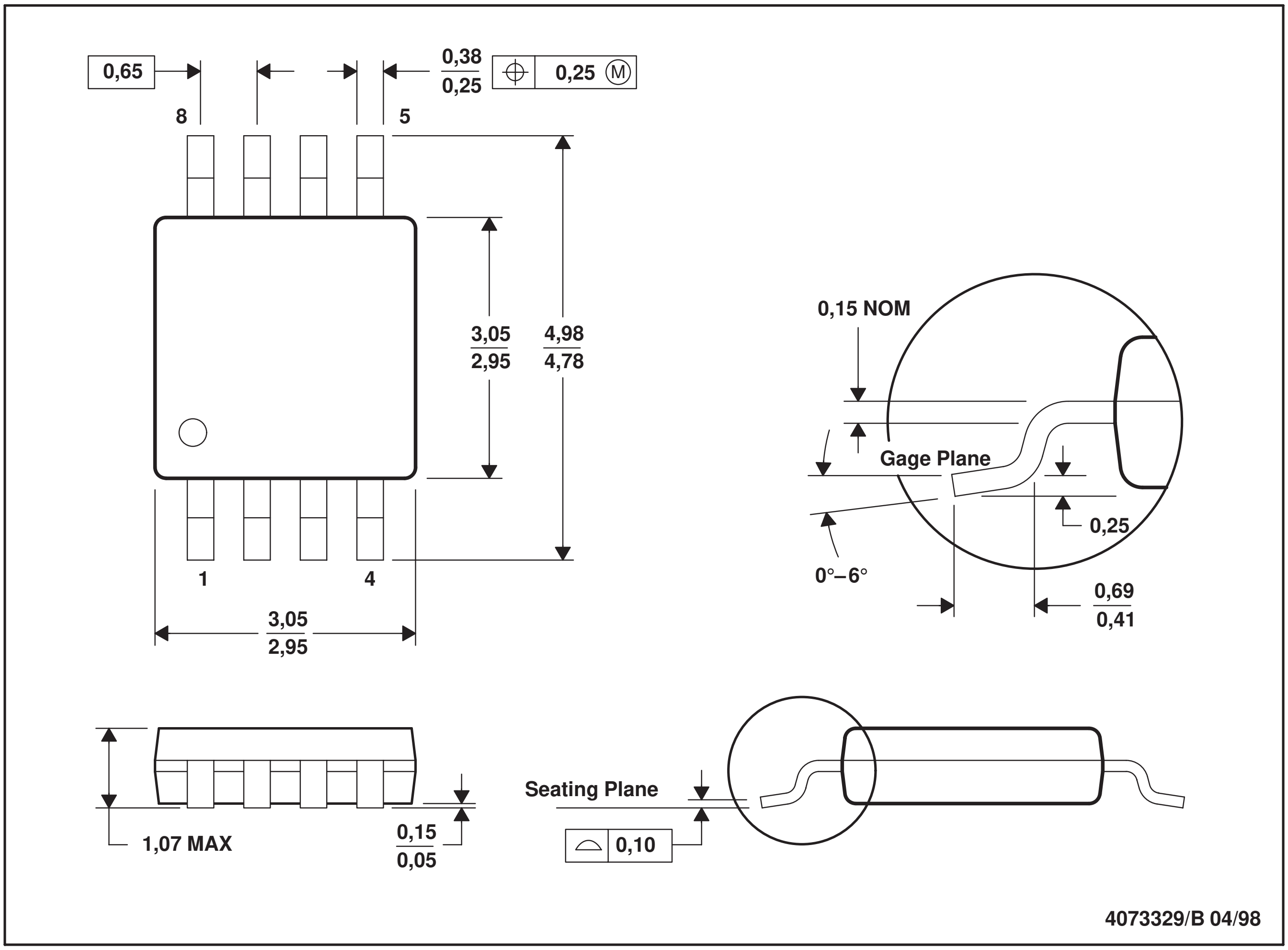
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

MECHANICAL INFORMATION

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



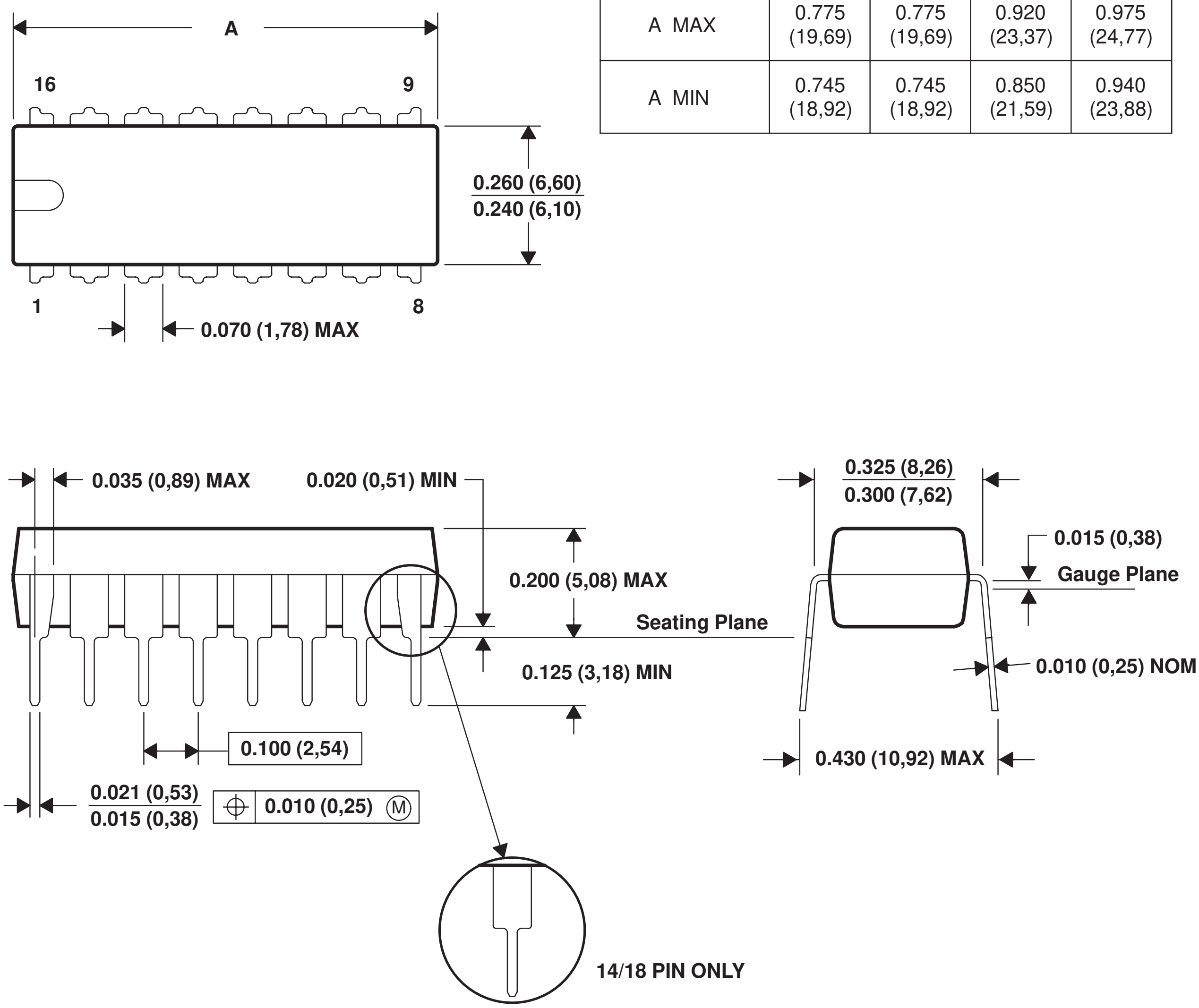
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

MECHANICAL INFORMATION

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)

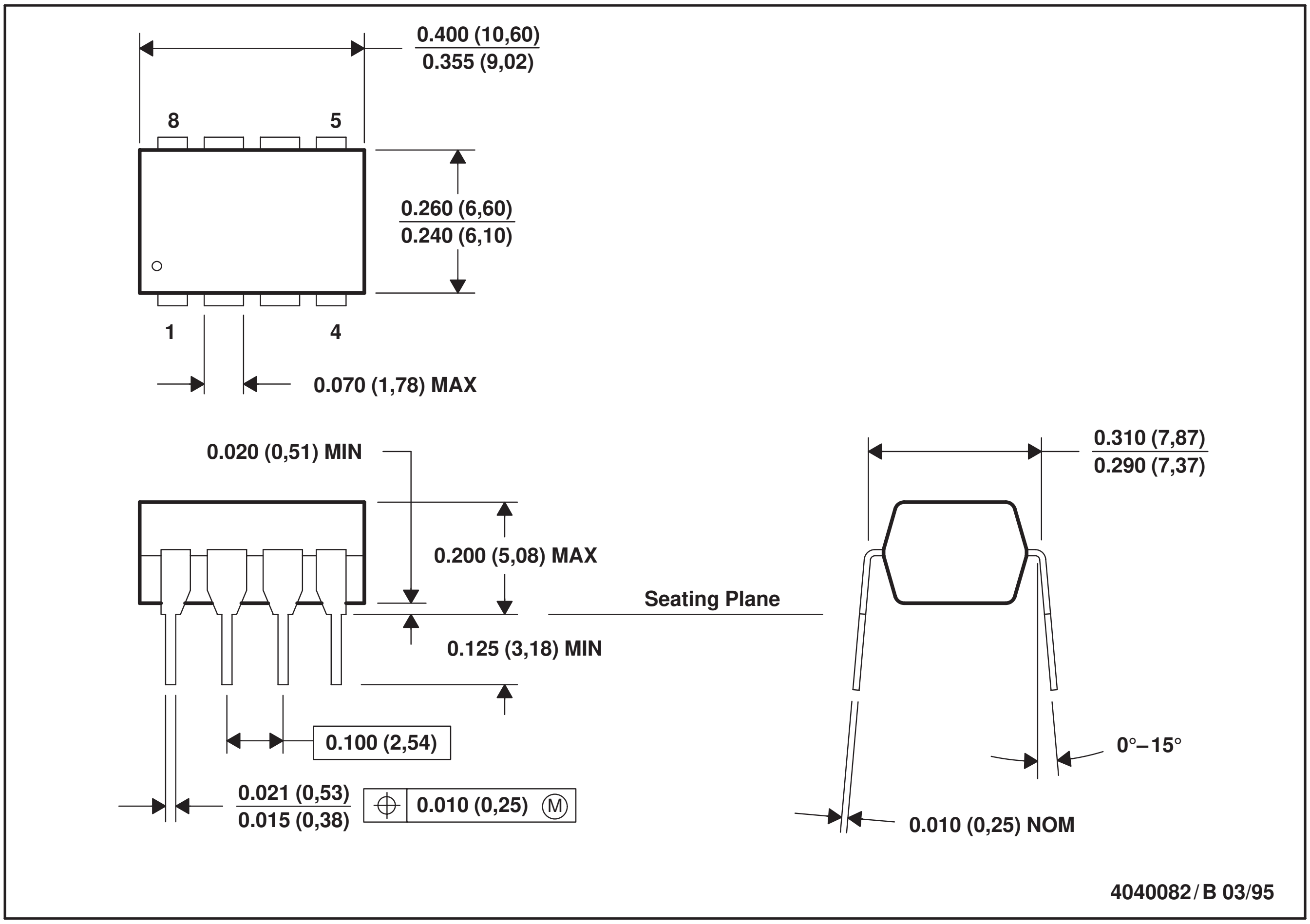


4040049/D 02/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

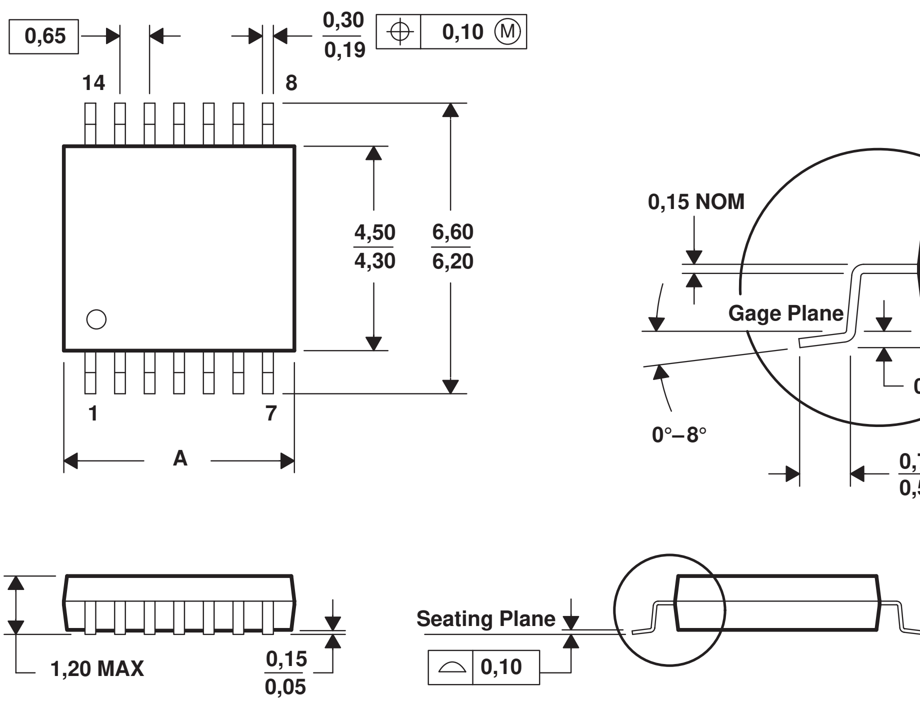


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLV2302ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2302IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2302IDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2302IDGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2302IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2302IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2302IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2302IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2302IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2302IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2304ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2304IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2304IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2304IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2304IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2304INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2304IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2304IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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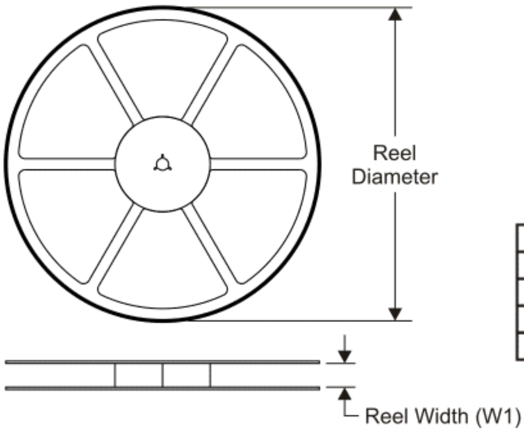
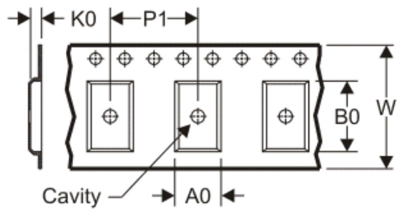
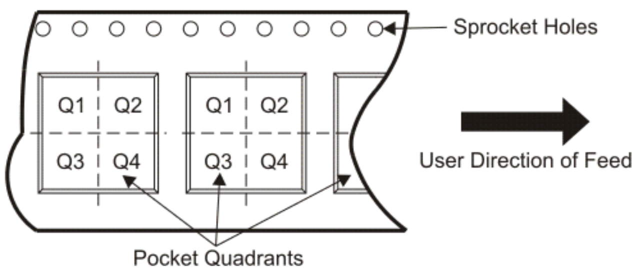
TAPE AND REEL INFORMATION





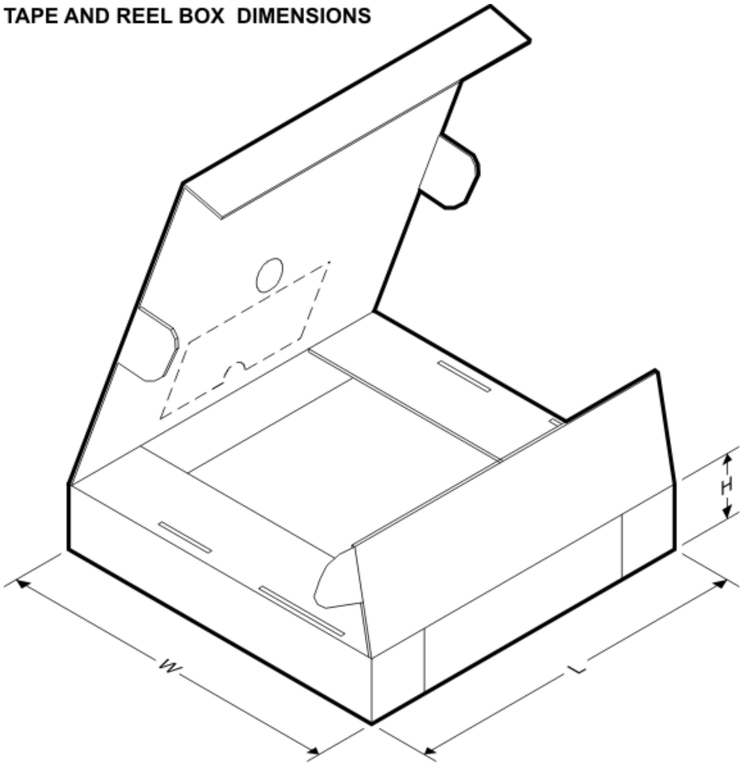
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2302IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2302IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2304IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2304IPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2302IDGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
TLV2302IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2304IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2304IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0