64-Position OTP Digital Potentiometer

AD5273

FEATURES

64 positions
One-time-programmable (OTP)[1] set-and-forget
  Resistance setting—low cost alternative over EEMEM
  Unlimited adjustments prior to OTP activation
1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ end-to-end terminal resistance
Compact SOT-23-8 standard package
Ultralow power: I_{DD} = 5 µA maximum
Fast settling time: t_S = 5 µs typ during power-up
I²C®-compatible digital interface
Computer software[2] replaces µC in
  factory programming applications
Wide temperature range: −40°C to +105°C
Low operating voltage: 2.7 V to 5.5 V
OTP validation check function

APPLICATIONS

System calibrations
Electronics level settings
Mechanical potentiometers and trimmer replacement
Automotive electronics adjustments
Transducer circuit adjustments
Programmable filters up to 6 MHz BW[3]

GENERAL DESCRIPTION

The AD5273 is a 64-position, one-time-programmable (OTP) digital potentiometer[4] that employs fuse link technology to achieve permanent program setting. This device performs the same electronic adjustment function as most mechanical trimmers and variable resistors. It allows unlimited adjustments before permanently setting the resistance values. The AD5273 is programmed using a 2-wire, I²C-compatible digital control. During write mode, a fuse blow command is executed after the final value is determined, thereby freezing the wiper position at a given setting (analogous to placing epoxy on a mechanical trimmer). When permanent setting is achieved, the value will not change, regardless of the supply variations or environmental stresses under normal operating conditions. To verify the success of permanent programming, Analog Devices patterned the OTP validation such that the fuse status can be discerned from two validation bits in the read mode.
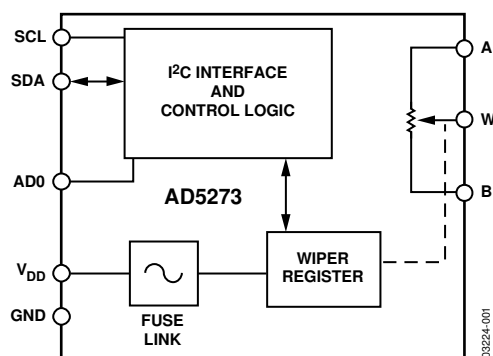
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

In addition, for applications that program the AD5273 at the factory, Analog Devices offers device programming software running on Windows® NT, Windows 2000, and Windows XP operating systems. This software application effectively replaces any external I²C controllers, which in turn enhances the user system's time-to-market.

The AD5273 is available in 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ resistances and in a compact SOT-23 8-lead standard package. It operates from −40°C to +105°C.

Along with its unique OTP feature, the AD5273 lends itself well to general digital potentiometer applications due to its effective resolution, array resistance options, small footprint, and low cost.

An AD5273 evaluation kit and software are available. The kit includes the connector and cable that can be converted for factory programming applications.

For applications that require dynamic adjustment of resistance settings with nonvolatile EEMEM, users should refer to the AD523x and AD525x families of nonvolatile memory digital potentiometers.

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[1] OTP allows unlimited adjustments before permanent setting.
[2] ADI cannot guarantee the software to be 100% compatible to all systems due to the wide variation in computer configurations.
[3] Applies to 1 kΩ parts only.
[4] The terms digital potentiometer, VR, and RDAC are used interchangeably.

AD5273

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REVISION HISTORY

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, $V_A < V_{DD}$, V_B = 0 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 1. Electrical Characteristics 1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ Versions

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS						
RHEOSTAT MODE						
Resolution	N				6	Bits
Resistor Differential Nonlinearity[2]	R-DNL					
10 kΩ, 50 kΩ, 100 kΩ		R_{WB}, V_A = NC	−0.5	+0.05	+0.5	LSB
1 kΩ		R_{WB}, V_A = NC	−1	+0.25	+1	LSB
Resistor Nonlinearity	R-INL					LSB
10 kΩ, 50 kΩ, 100 kΩ		R_{WB}, V_A = NC	−0.5	+0.10	+0.5	LSB
1 kΩ		R_{WB}, V_A = NC	−5	+2	+5	LSB
Nominal Resistance Tolerance[3]	$\Delta R_{AB}/R_{AB}$	T_A = 25°C				
10 kΩ, 50 kΩ, 100 kΩ			−30		+30	%
Nominal Resistance, 1 kΩ	R_{AB}		0.8	1.2	1.6	kΩ
Rheostat Mode Temperature Coefficient[4]	$(\Delta R_{AB}/R_{AB})/\Delta T$	Wiper = NC		300		ppm/°C
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 3 V or 5 V		60	100	Ω
DC CHARACTERISTICS						
POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[5]	DNL		−0.5	+0.1	+0.5	LSB
Integral Nonlinearity[5]	INL		−0.5		+0.5	LSB
Voltage Divider[4]						
Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x20		10		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x3F	−1		0	LSB
10 kΩ, 50 kΩ, 100 kΩ			−1		0	LSB
1 kΩ			−6		0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	−6		0	LSB
10 kΩ, 50 kΩ, 100 kΩ			0		1	LSB
1 kΩ			0		5	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance[7] A, B	C_A, C_B	f = 5 MHz, measured to GND, code = 0x20		25		pF
Capacitance[7] W	C_W	f = 1 MHz, measured to GND, code = 0x20		55		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High (SDA and SCL)[8]	V_{IH}		0.7 V_{DD}		V_{DD} + 0.5	V
Input Logic Low (SDA and SCL)[8]	V_{IL}		−0.5		0.3 V_{DD}	V
Input Logic High (ADO)	V_{IH}		3.0		V_{DD}	V
Input Logic Low (ADO)	V_{IL}	V_{IN} = 0 V or 5 V	0		0.4	V
Input Logic Current	I_{IL}			0.01	1	μA
Input Capacitance	C_{IL}			3		pF
Output Logic Low (SDA)	V_{OL}				0.4	V
Three-State Leakage Current	I_{OZ}				±1	μA
Output Capacitance[7]	C_{OZ}			3		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Power Supply[8, 9]	V_{DD_OTP}	T_A = 25°C	5.25		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V V_{IL} = 0 V		0.1	5	μA
OTP Supply Current[8, 10]	I_{DD_OTP}	T_A = 25°C, V_{DD_OTP} = 5.5 V	100			mA
Power Dissipation[11]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{IL} = 0 V, V_{DD} = 5 V		0.2	0.03	mW
Power Supply Sensitivity	PSRR	R_{AB} = 1 kΩ	−0.3		+0.3	%/%
	PSRR	R_{AB} = 10 kΩ, 50 kΩ, 100 kΩ	−0.05		+0.05	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[7, 12, 13]						
Bandwidth, −3 dB	BW_1 kΩ	R_{AB} = 1 kΩ, code = 0x20		6000		kHz
	BW_10 kΩ	R_{AB} = 10 kΩ, code = 0x20		600		kHz
	BW_50 kΩ	R_{AB} = 50 kΩ, code = 0x20		110		kHz
	BW_100 kΩ	R_{AB} = 100 kΩ, code = 0x20		60		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, R_{AB} = 1 kΩ, V_B = 0 V, f = 1 kHz		0.05		%
Adjustment Settling Time	t_{S1}	V_A = 5 V ± 1 LSB error band, V_B = 0, measured at V_W		5		µs
OTP Settling Time[14]	t_{S_OTP}	V_A = 5 V ± 1 LSB error band, V_B = 0, measured at V_W, V_{DD} = 5 V		400		ms
Power-Up Settling Time—After Fuses Blown	t_{S2}	V_A = 5 V ± 1 LSB error band, V_B = 0, measured at V_W, V_{DD} = 5 V		5		µs
Resistor Noise Voltage	e_{N_WB}	R_{AB} = 1 kΩ, f = 1 kHz, code = 0x20		3		nV/√Hz
		R_{AB} = 20 kΩ, f = 1 kHz, code = 0x20		13		nV/√Hz
		R_{AB} = 50 kΩ, f = 1 kHz, code = 0x20		20		nV/√Hz
		R_{AB} = 100 kΩ, f = 1 kHz, code = 0x20				nV/√Hz
INTERFACE TIMING CHARACTERISTICS (Applies to All Parts[7, 13, 15])						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time Between Stop and Start	t_1		1.3			µs
$t_{HD; STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU; STA}$ Setup Time for Start Condition	t_5		0.6			
$t_{HD; DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU; DAT}$ Data Setup Time	t_7		0.1			µs
t_F Fall Time of Both SDA and SCL Signals	t_8				0.3	µs
t_R Rise Time of Both SDA and SCL Signals	t_9				0.3	µs
$t_{SU; STO}$ Setup Time for Stop Condition	t_{10}		0.6			µs

[1] Typicals represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] V_{AB} = V_{DD}, Wiper (V_W) = no connect.
[4] $\Delta R_{WB}/\Delta T$ = $\Delta R_{WA}/\Delta T$. Temperature coefficient is code-dependent; see the Typical Performance Characteristics.
[5] INL and DNL are measured at V_W. INL V with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB max are guaranteed monotonic operating conditions.
[6] Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.
[7] Guaranteed by design; not subject to production test.
[8] The minimum voltage requirement on the V_{IH} is 0.7 V × V_{DD}. For example, V_{IH} min = 3.5 V when V_{DD} = 5 V. It is typical for the SCL and SDA resistors to be pulled up to V_{DD}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.
[9] Different from the operating power supply; the power supply for OTP is used one time only.
[10] Different from the operating current; the supply current for OTP lasts approximately 400 ms for the one time it is needed.
[11] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[12] Bandwidth, noise, and settling time depend on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[13] All dynamic characteristics use V_{DD} = 5 V.
[14] Different from the settling time after the fuses are blown. The OTP settling time occurs once only.
[15] See Figure 28 for the location of the measured values.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min
V_{DD} to GND	−0.3 V, +6.5 V
V_A, V_B, V_W to GND	GND, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous ($R_{WB} \leq 1$ kΩ, A Open)[1]	±4 mA
I_{WA} Continuous ($R_{WA} \leq 1$ kΩ, B Open)	±4 mA
Digital Input and Output Voltage to GND	0 V, V_{DD}
Operating Temperature Range	−40°C to +105°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Thermal Resistance θ_{JA}, SOT-23[2]	230°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, the maximum power dissipation of the package; the maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_J max − T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
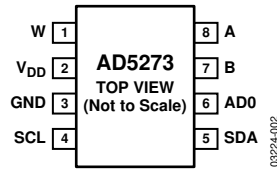
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No.	Mnemonic	Description
1	W	Wiper Terminal W. $GND \leq V_W \leq V_{DD}$.
2	V_{DD}	Positive Power Supply. Specified for non-OTP operation from 2.7 V to 5.5 V. For OTP programming, V_{DD_OTP} must be a minimum of 5.25 V and a have 100 mA driving capability.
3	GND	Common Ground.
4	SCL	Serial Clock Input. Requires a pull-up resistor. If it is driven directly from a logic controller without the pull-up resistor, ensure that V_{IH} min is 0.7 V × V_{DD}.
5	SDA	Serial Data Input/Output. Requires a pull-up resistor. If it is driven directly from a logic controller without the pull-up resistor, ensure that V_{IH} min is 0.7 V × V_{DD}.
6	AD0	I²C Device Address Bit. Allows a maximum of two AD5273s to be addressed.
7	B	Resistor Terminal B. $GND \leq V_B \leq V_{DD}$.
8	A	Resistor Terminal A. $GND \leq V_A \leq V_{DD}$.

TYPICAL PERFORMANCE CHARACTERISTICS
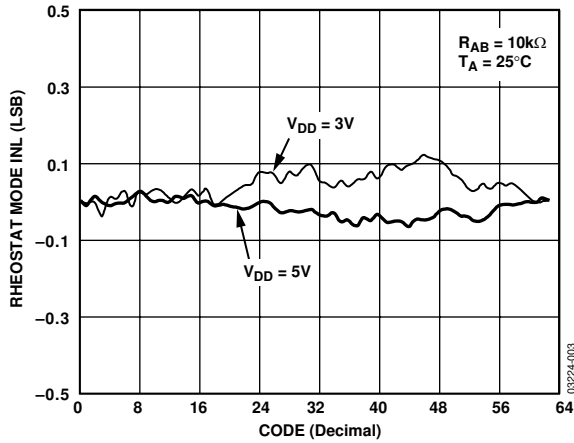
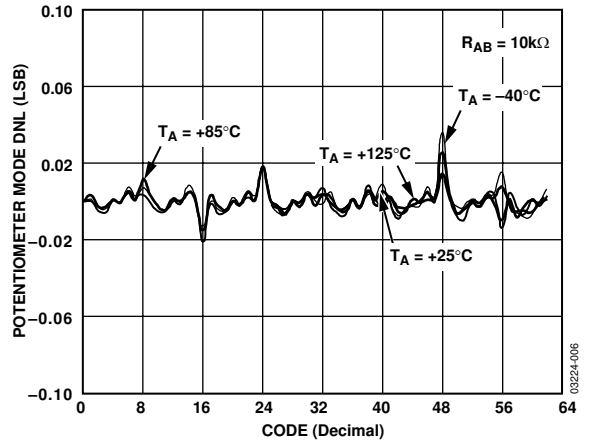Figure 3. R_{INL} vs. Code vs. Supply Voltages

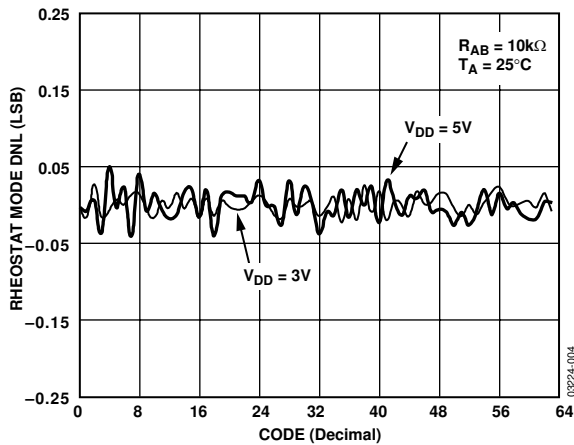Figure 6. DNL vs. Code vs. Temperature

Figure 4. R_{DNL} vs. Code vs. Supply Voltages
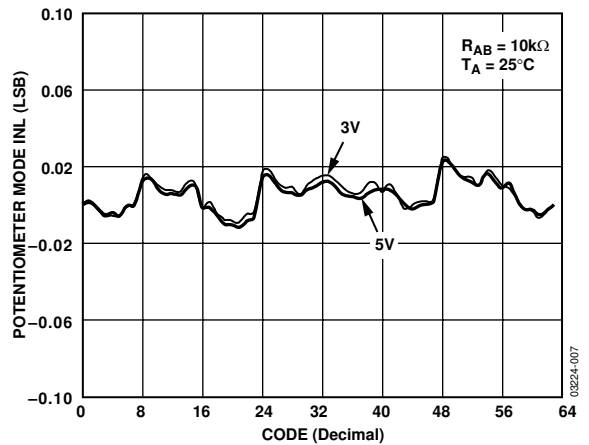

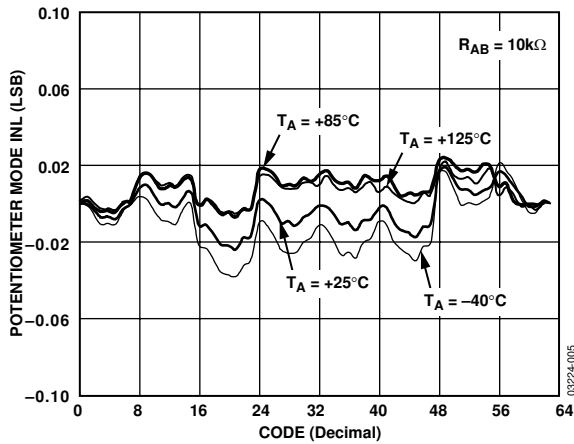Figure 7. INL vs. Code vs. Supply Voltages

Figure 5. INL vs. Code vs. Temperature

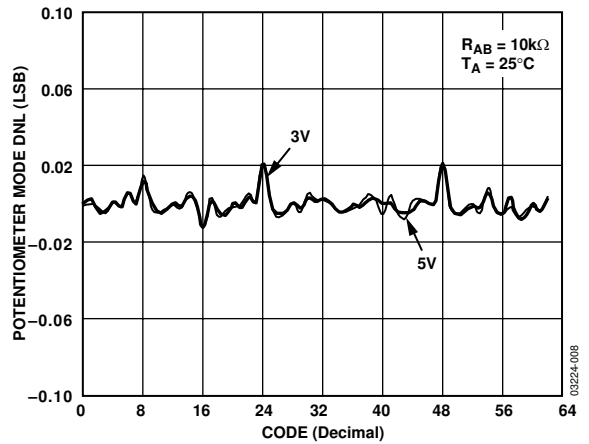Figure 8. DNL vs. Code vs. Supply Voltages

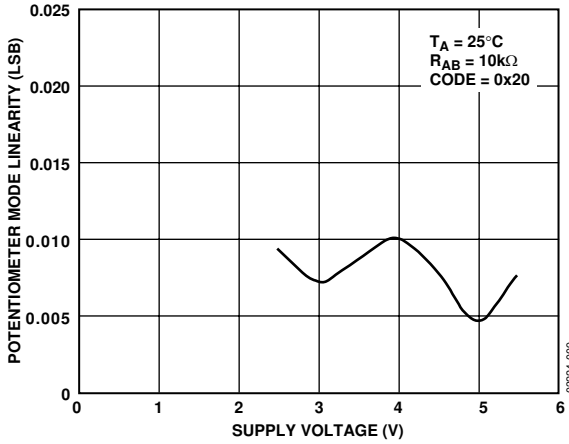Figure 9. INL vs. Supply Voltage

Figure 10. R_INL vs. Supply Voltage

Figure 11. Full-Scale Error

Figure 12. Zero-Scale Error

Figure 13. Supply Current vs. Temperature
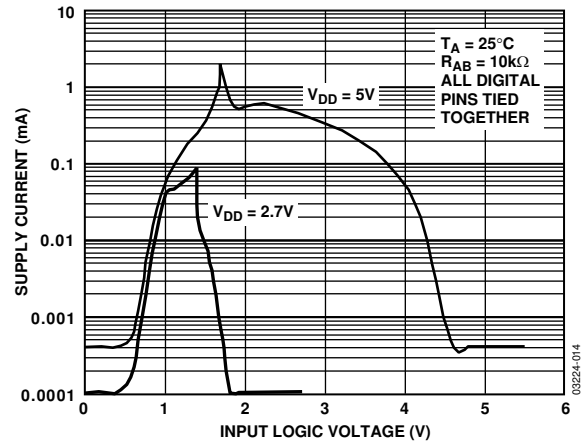
Figure 14. Supply Current vs. Digital Input Voltage
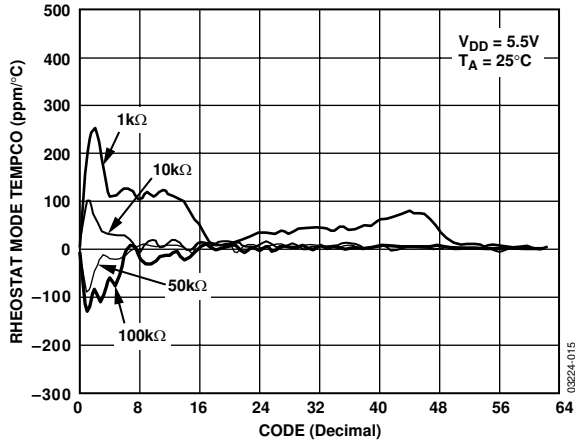
Figure 15. Rheostat Mode Tempco (ΔR_WB/R_WB)/ΔT vs. Code
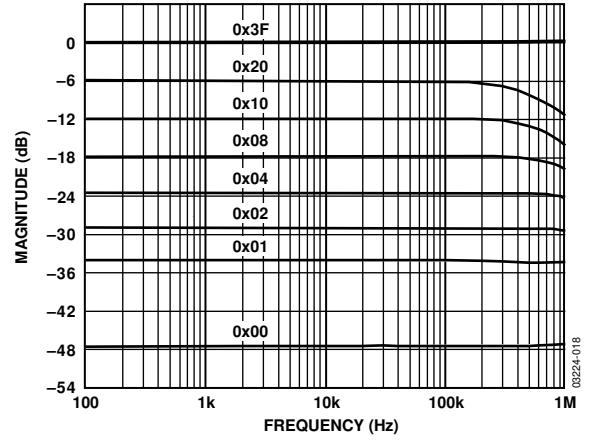
Figure 18. Gain vs. Frequency vs. Code, R_AB = 10 kΩ
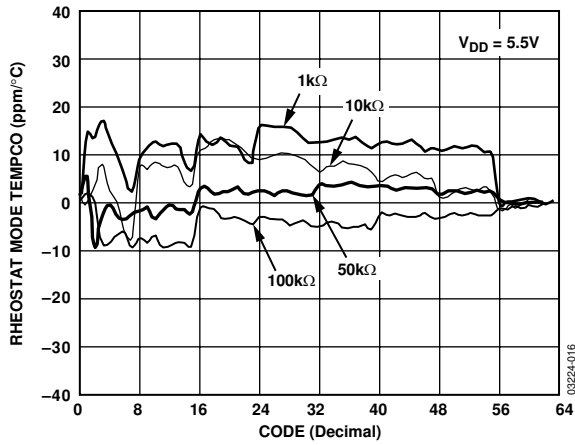
Figure 16. Potentiometer Mode Tempco (ΔV_W/V_W)/ΔT vs. Code
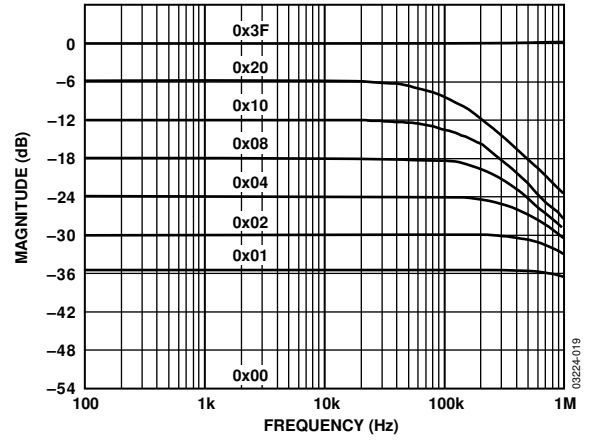
Figure 19. Gain vs. Frequency vs. Code, R_AB = 50 kΩ
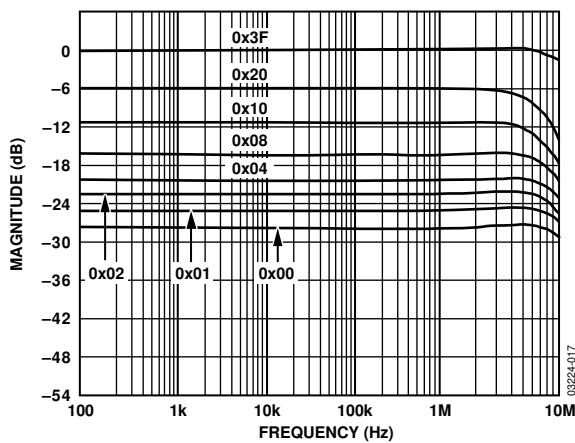
Figure 17. Gain vs. Frequency vs. Code, R_AB = 1 kΩ
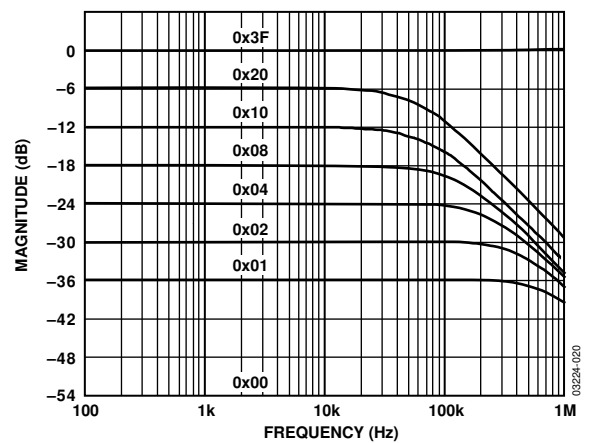
Figure 20. Gain vs. Frequency vs. Code, R_AB = 100 kΩ
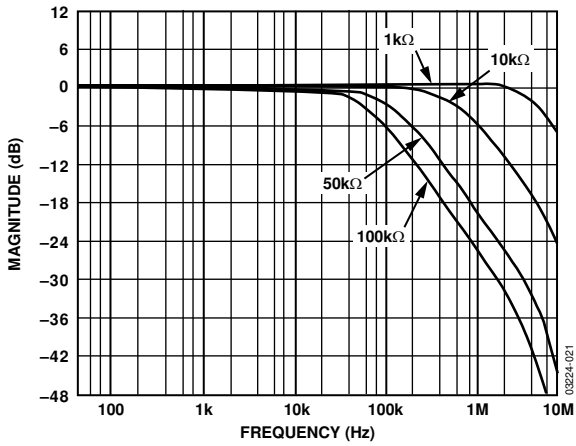
Figure 21. −3 dB Bandwidth

Figure 22. PSRR vs. Frequency

Figure 23. Digital Feedthrough

Figure 24. Large Settling Time

Figure 25. Midscale Glitch Energy
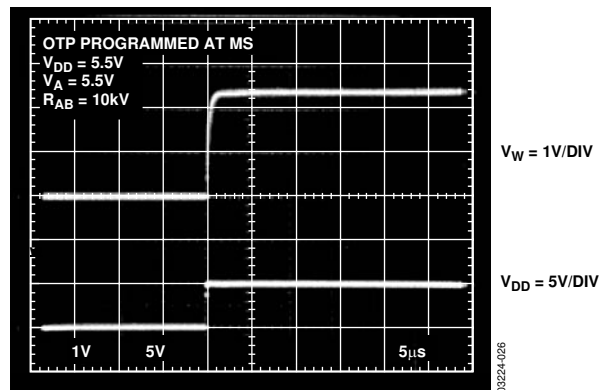
Figure 26. Power-Up Settling Time After Fuses Blown
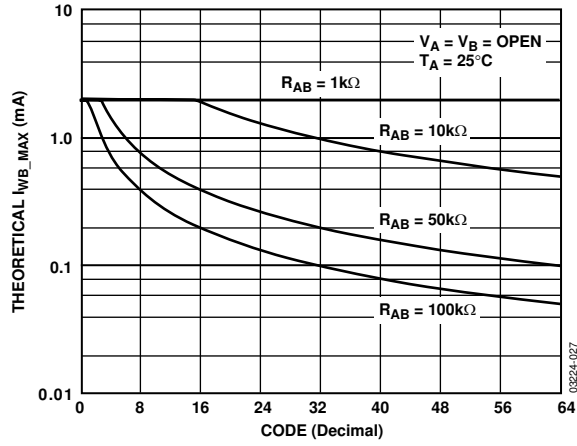
Figure 27. I_{WB_MAX} vs. Code
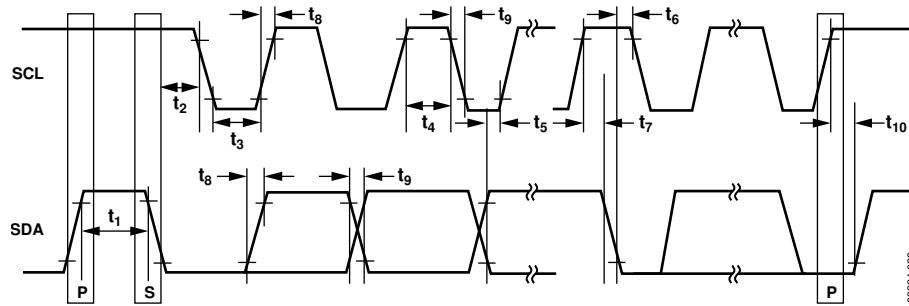
Figure 28. Interface Timing Diagram

THEORY OF OPERATION

The AD5273 is a one-time-programmable (OTP), set-and-forget, 6-bit digital potentiometer. The AD5273 allows unlimited 6-bit adjustments prior to the OTP. OTP technology is a proven cost-effective alternative over EEMEM in one-time memory programming applications. The AD5273 employs fuse link technology to achieve the memory retention of the resistance setting function. It comprises six data fuses, which control the address decoder for programming the RDAC, one user mode test fuse for checking setup error, and one programming lock fuse for disabling any further programming once the data fuses are programmed correctly.

ONE-TIME PROGRAMMING

Prior to OTP activation, the AD5273 presets to midscale during power-on. After the wiper is set to the desired position, the resistance can be permanently set by programming the T bit and the one-time V_{DD_OTP} to high and by coding the part properly (see Table 4). The fuse link technology of the AD5273

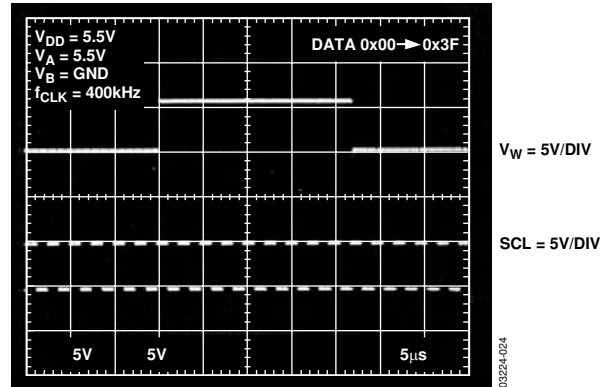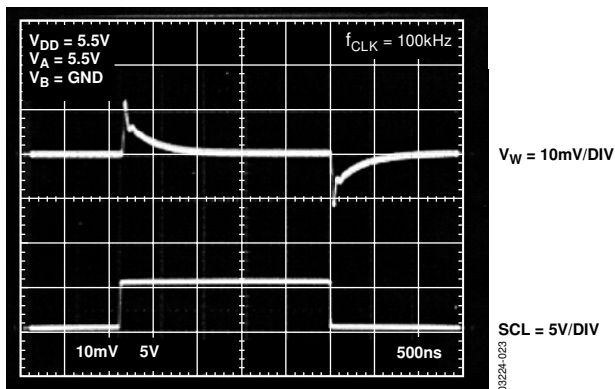requires a V_{DD_OTP} between 5.25 V and 5.5 V to blow the fuses to achieve a given nonvolatile setting. During operation, however, V_{DD} can be 2.7 V to 5.5 V. Therefore, a system supply that is lower than 5.25 V requires an external supply for OTP. The user is allowed only one attempt to blow the fuses. If the user fails to blow the fuses on the first attempt, the fuse structure might change such that they can never be blown, regardless of the energy applied during subsequent events. For details, see the Power Supply Considerations section.

The device control circuit has two validation bits, E1 and E0, that can be read back in the read mode for checking the programming status, as shown in Table 5. Users should always read back the validation bits to ensure that the fuses are properly blown. After the fuses have been blown, all fuse latches are enabled upon subsequent power-on; therefore, the output corresponds to the stored setting. Figure 29 shows a detailed functional block diagram.
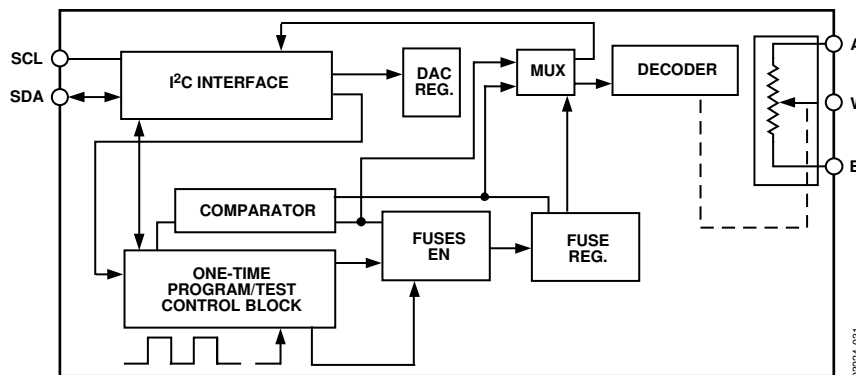
Figure 29. Detailed Functional Block Diagram

Table 4. SDA Write Mode Bit Format

S	0	1	0	1	1	0	AD0	0	A	T	X	X	X	X	X	X	X	A	X	X	D5	D4	D3	D2	D1	D0	A	P
			SLAVE ADDRESS BYTE									INSTRUCTION BYTE											DATA BYTE					

Table 5. SDA Read Mode Bit Format

S	0	1	0	1	1	0	AD0	1	A	E1	E0	D5	D4	D3	D2	D1	D0	A	P
			SLAVE ADDRESS BYTE									DATA BYTE							

SDA Bit Definitions and Descriptions

S = start condition.

P = stop condition.

A = acknowledge.

X = don't care.

T = OTP programming bit. Logic 1 programs wiper position permanently.

D5, D4, D3, D2, D1, D0 = data bits.

E1, E0 = OTP validation bits.

0, 0 = ready to program.

0, 1 = test fuse not blown successfully. (For factory setup checking purpose only. Users should not see these combinations.)

1, 0 = fatal error. Do not retry. Discard the unit.

1, 1 = programmed successfully. No further adjustments possible.

AD0 = I²C device address bit. Allows maximum of two AD5273s to be addressed.

VARIABLE RESISTANCE AND VOLTAGE FOR RHEOSTAT MODE

If only the W-to-B or W-to-A terminals are used as variable resistors, the unused A or B terminal can be opened or shorted with W. This operation is called rheostat mode (see Figure 30).
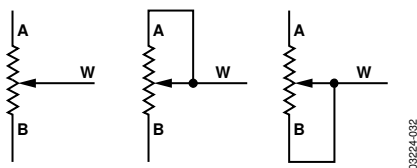
Figure 30. Rheostat Mode Configuration

The nominal resistance, R_{AB}, of the RDAC has 64 contact points accessed by the wiper terminal, plus the B terminal contact if R_{WB} is considered. The 6-bit data in the RDAC latch is decoded to select one of the 64 settings. Assuming that a 10 kΩ part is used, the wiper's first connection starts at Terminal B for Data Register 0x00. This connection yields a minimum of 60 Ω resistance between Terminals W and B because of the 60 Ω wiper contact resistance. The second connection is the first tap point, which corresponds to 219 Ω ($R_W = 1 \times R_{AB}/63 + R_W$) for Data Register 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10060 Ω ($63 \times R_{AB}/63 + R_W$). Figure 31 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining R_{WB} is

$$R_{WB}(D) = \frac{D}{63} \times R_{AB} + R_W \qquad (1)$$

where:
D is the decimal equivalent of the 6-bit binary code.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

Table 6. R_{WB} vs. Codes: R_{AB} = 10 kΩ; Terminal A Opened

D (Dec)	R_{WB} (Ω)	Output State
63	10060	Full scale ($R_{AB} + R_W$)
32	5139	Midscale
1	219	1 LSB
0	60	Zero scale (wiper contact resistance)

Since a finite wiper resistance of 60 Ω is present in the zero-scale condition, care should be taken to limit the current flow between W and B in this state to a maximum pulse current of 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a complementary resistance, R_{WA}. When these terminals are used, Terminal B can be opened or shorted to W. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{63 - D}{63} \times R_{AB} + R_W \qquad (2)$$

Table 7. R_{WA} vs. Codes: R_{AB} =10 kΩ, Terminal B Opened

D (Dec)	R_{WA} (Ω)	Output State
63	60	Full scale
32	4980	Midscale
1	9901	1 LSB
0	10060	Zero scale

The typical distribution of the resistance tolerance from device to device is process-lot dependent, and it is possible to have ±30% tolerance.

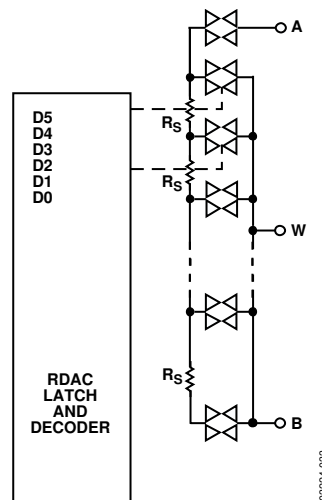*Figure 31. AD5273 Equivalent RDAC Circuit*

AD5273

VARIABLE RESISTANCE AND VOLTAGE FOR POTENTIOMETER MODE

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation (see Figure 32).
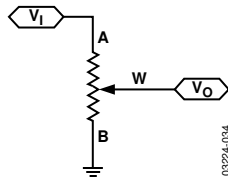

Figure 32. Potentiometer Mode Configuration

Ignoring the effect of the wiper resistance, the transfer function is simply

$$V_W(D) = \frac{D}{63} V_A \qquad (3)$$

A more accurate calculation, which includes the wiper resistance effect, yields

$$V_W(D) = \frac{\dfrac{D}{63} R_{AB} + R_W}{R_{AB} + 2R_W} V_A \qquad (4)$$

Unlike rheostat mode where the absolute tolerance is high, potentiometer mode yields an almost ratiometric function of D/63 with a relatively small error contributed by the R_W terms. Therefore the tolerance effect is almost cancelled. Although the step resistor, R_S, and CMOS switch resistor, R_W, have very different temperature coefficients, the ratiometric adjustment also reduces the overall temperature coefficient effect to 5 ppm/°C, except at low value codes where R_W dominates.

Potentiometer mode includes op amp feedback resistor networks and other voltage scaling applications. Terminals A, W, and B can in fact be input or output terminals, provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed V_{DD} to GND.

ESD PROTECTION

Digital inputs SDA and SCL are protected with a series input resistor and parallel Zener ESD structures (see Figure 33).
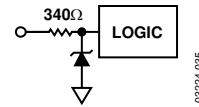
Figure 33. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

There are also ESD protection diodes between V_{DD} and the RDAC terminals. The V_{DD} of AD5273 therefore defines their voltage boundary conditions (see Figure 34). Supply signals present on Terminals A, B, and W that exceed V_{DD} are clamped by the internal forward-biased diodes.
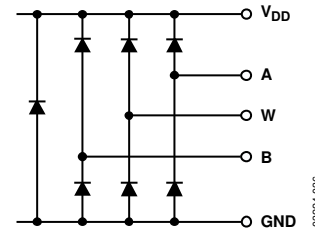
Figure 34. Maximum Terminal Voltages Set by V_{DD}

POWER-UP/POWER-DOWN SEQUENCES

Because of the ESD protection diodes, it is important to power V_{DD} first before applying any voltages to Terminals A, B, and W. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally and can affect the rest of the user's circuits. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}. Similarly, V_{DD} should be powered down last.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both OTP and normal operating voltage supplies are applied to the same V_{DD} terminal of the AD5273. The AD5273 employs fuse link technology that requires 5.25 V to 5.5 V for blowing the internal fuses to achieve a given setting, but normal V_{DD} can be in the range of 2.7 V to 5.5 V after completing the fuse programming process. As a result, dual voltage supplies and isolation are needed if the system V_{DD} is lower than the required V_{DD_OTP}. For successful OTP, the fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 5.25 V to 5.5 V and provide a 100 mA current for 400 ms. Once fuse programming is completed, the V_{DD_OTP} supply must be removed to allow normal operation of 2.7 V to 5.5 V; then the device reduces the current consumption to the μA range. Figure 35 shows the simplest implementation using a jumper. This approach saves one voltage supply, but draws additional current and requires manual configuration.
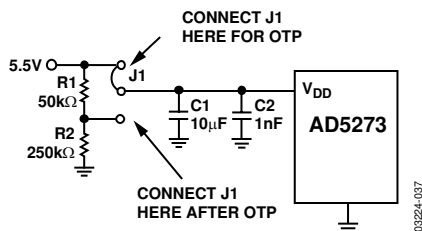

Figure 35. Power Supply Requirement

An alternate approach for 3.5 V to 5.25 V systems is to add a signal diode between the system supply and the OTP supply for isolation, as shown in Figure 36.
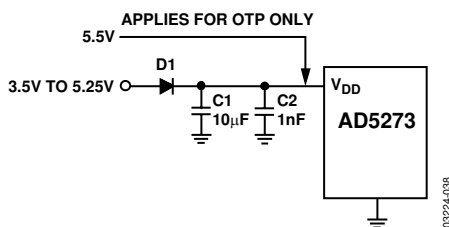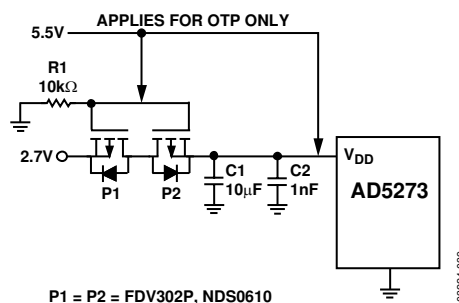

Figure 36. 5.5 V OTP Supply Isolated from the
3.5 V to 5.25 V Normal Operating Supply

When operating systems at 2.7 V, use of the bidirectional low threshold P-Ch MOSFETs is recommended for the supply's isolation. As shown in Figure 37, this assumes that the 2.7 V system voltage is applied first and that the P1 and P2 gates are pulled to ground, thus turning on P1 first and then P2. As a result, V_{DD} of the AD5273 approaches 2.7 V. When the AD5273 setting is found, the factory tester applies the V_{DD_OTP} to both the V_{DD} and the MOSFETs' gates, thus turning off P1 and P2. The OTP command should be executed at this time to program the AD5273 while the 2.7 V source is protected. Once the fuse programming is completed, the tester withdraws the V_{DD_OTP} and the AD5273's setting is fixed permanently.

Figure 37. 5.5 V OTP Supply Isolated From the
2.7 V Normal Operating Supply

AD5273 achieves the OTP function through blowing internal fuses. Users should always apply the 5.25 V to 5.5 V OTP voltage requirement at the first fuse programming attempt. Failure to comply with this requirement can lead to a change in fuse structures, rendering programming inoperable.

Care should be taken when SCL and SDA are driven from a low voltage logic controller. Users must ensure that the logic high level is between $0.7 V \times V_{DD}$ and V_{DD}. Refer to the Level Shift for Different Voltages section.

Poor PCB layout introduces parasitics that can affect fuse programming. Therefore, it is recommended to add a 10 μF tantalum capacitor in parallel with a 1 nF ceramic capacitor as close as possible to the V_{DD} pin. The type and value chosen for both capacitors are important. This combination of capacitor values provides a fast response and larger supply current handling with minimum supply drop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple, while C2 reduces high frequency noise during normal operation.

CONTROLLING THE AD5273

To control the AD5273, users can program the device with either computer software or with external I²C controllers.

SOFTWARE PROGRAMMING

Because of the OTP feature, users can program the AD5273 in the factory before shipping it to end users. Therefore, ADI offers device programming software that can be implemented in the factory on computers running Windows NT, Windows 2000, and Windows XP platforms. The software, which can be downloaded from the AD5273 product folder at http://www.analog.com, is an executable file that does not require any programming languages or user programming skills. Figure 38 shows the software interface.
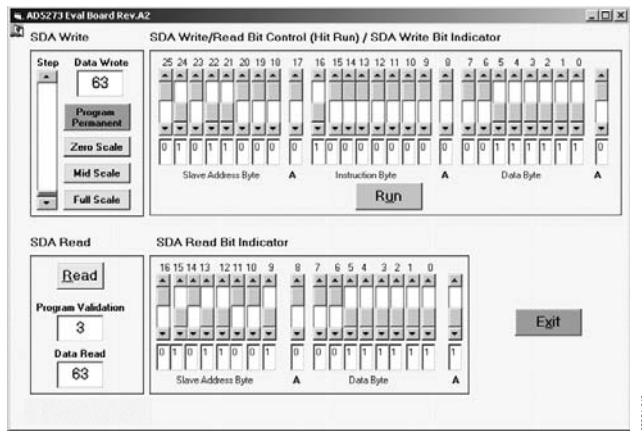

Figure 38. Software Interface

Write

The AD5273 starts at midscale after power-up prior to any OTP programming. To increment or decrement the resistance, move the scrollbar on the left. Once the desired setting is found, click **Program Permanent** to lock the setting permanently. To write any specific values, use the bit pattern control in the upper section and click **Run**. The format of writing data to the device is shown in Table 4. Once the desired setting is found, set the T bit to 1 and click **Run** to program the setting permanently.

Read

To read the validation bits and data from the device, click **Read**. The user can also set the bit pattern in the upper section and click **Run**. The format of reading data from the device is shown in Table 5.

To control the device in both read and write operations, the program generates the I²C digital signals through the parallel port LPT1 Pins 2, 3, 15, and 25 for SDA_write, SCL, SDA_read, and DGND, respectively (see Figure 39).

To apply the device programming software in the factory, lay out the AD5273 SCL and SDA pads on the PCB such that the programming signals can be communicated to and from the parallel port (see Figure 39). Figure 40 shows a recommended AD5273 PCB layout into which pogo pins can be inserted for factory programming. To prevent damaging the PC parallel port, 100 Ω resistors should also be put in series to the SCL and SDA pins. Pull-up resistors on SCL and SDA are also required.
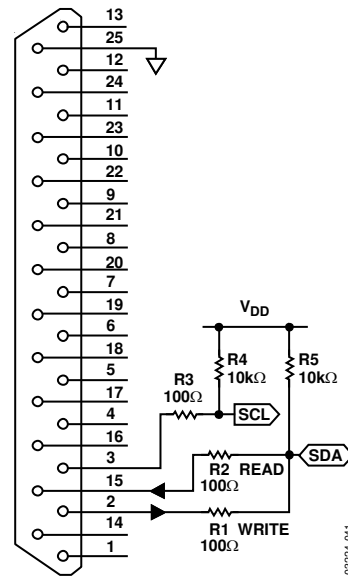

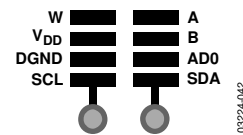*Figure 39. Parallel Port Connection. Pin 2 = SDA_Write, Pin 3 = SCL, Pin 15 = SDA_Read, and Pin 25 = DGND*

Figure 40. Recommended AD5273 PCB Layout

I²C CONTROLLER PROGRAMMING
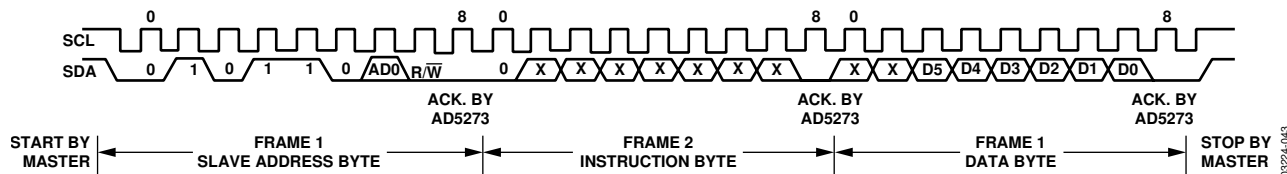
Write Bit Patterns
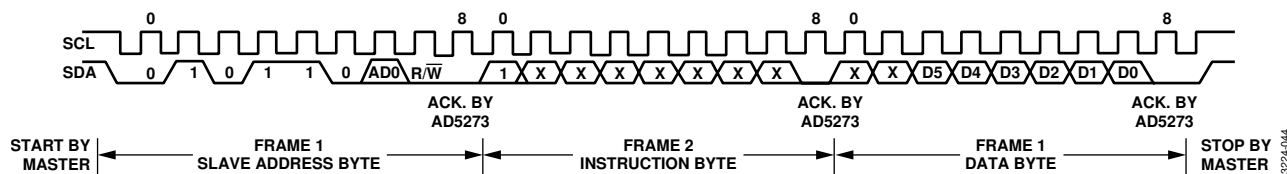

Figure 41. Writing to the RDAC Register

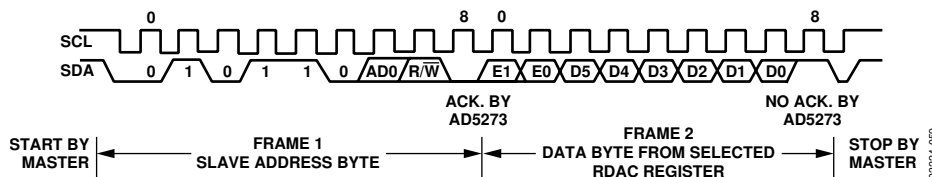Figure 42. Activating One-Time Programming

Read Bit Pattern

Figure 43. Reading Data from the RDAC Register

For users who do not use the software solution, the AD5273 can be controlled via an I²C-compatible serial bus and is connected to this bus as a slave device. Referring to Figure 41, Figure 42, and Figure 43, the 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition. A start condition is defined as a high to low transition on the SDA line while SCL is high, as shown in Figure 41. The byte following the start condition is the slave address byte, which consists of six MSBs defined as 010110. The next bit is AD0; it is an I²C device address bit. Depending on the states of the AD0 bits, two AD5273s can be addressed on the same bus, as shown in Figure 44. The last LSB is the R/$\overline{W}$ bit, which determines whether data is read from or written to the slave device.

   The slave address corresponding to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.

2. A write operation contains one more instruction byte than the read operation. The instruction byte in the write mode follows the slave address byte. The MSB of the instruction byte labeled T is the OTP bit. After acknowledging the instruction byte, the last byte in the write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL, as shown in Figure 41.

3. In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (slight difference from write mode, there are eight data bits followed by a no acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL, as shown in Figure 43.

4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In the write mode, the master pulls the SDA

line high during the 10th clock pulse to establish a stop condition, as shown in Figure 41 and Figure 42. In the read mode, the master issues a no acknowledge for the ninth clock pulse, that is, the SDA line remains high. The master then brings the SDA line low before the 10th clock pulse, which goes high to establish a stop condition, as shown in Figure 43.

A repeated write function gives the user flexibility to update the RDAC output continuously, except after permanent programming, when the part is addressed and receives instructions only once. During the write cycle, each data byte updates the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output updates after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruc-tion, this byte updates the output of the selected slave device. If different instructions are needed, the write mode must be started again with a new slave address, instruction, and data bytes. Similarly, a repeated read function of the RDAC is also allowed.

CONTROLLING TWO DEVICES ON ONE BUS

Figure 44 shows two AD5273 devices on the same serial bus. Each has a different slave address since the state of each AD0 pin is different. This allows each device to operate independently. The master device output bus line drivers are open-drain pull-down in a fully I²C-compatible interface.
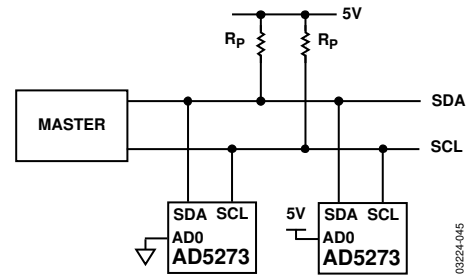

Figure 44. Two AD5273 Devices on One Bus

APPLICATIONS

DAC

It is common to buffer the output of the digital potentiometer as a DAC. The buffer minimizes the load dependence and delivers higher current to the load, if needed.
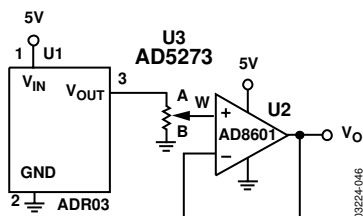

Figure 45. Programmable Voltage Reference (DAC)

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment, such as a laser diode driver or tunable laser, consider a booster voltage source, as shown in Figure 46.
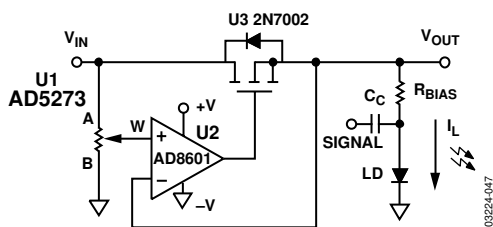

Figure 46. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch FET, N_1. N_1 power handling must be adequate to dissipate $(V_{IN} - V_{OUT}) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference, such as the ADR421, ADR03, or ADR370, can be applied at Terminal A of the digital potentiometer.

PROGRAMMABLE CURRENT SOURCE

A programmable current source can be implemented with the circuit shown in Figure 47. The load current is the voltage across Terminals B-to-W of the AD5273 divided by R_S. At zero scale, Terminal A of the AD5273 is −2.048 V, which makes the wiper voltage clamped at ground potential. Depending on the load, Equation 5 is therefore valid only at certain codes. For example, when the compliance voltage, V_L, equals half of V_{REF}, the current can be programmed from midscale to full scale of the AD5273.
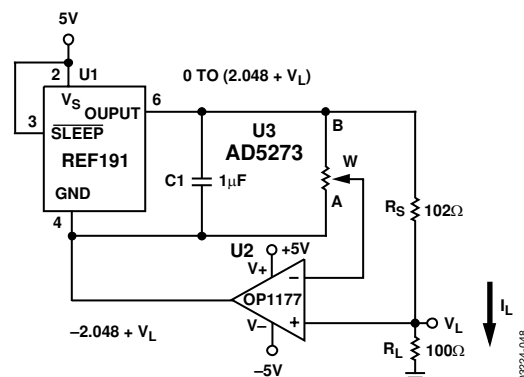

Figure 47. Programmable Current Source

$$I_L = \frac{(V_{REF} \times D)/64}{R_S} \mid 32 \le D \le 63 \qquad (5)$$

GAIN CONTROL COMPENSATION

As shown in Figure 48, the digital potentiometers are commonly used in gain controls or sensor transimpedance amplifier signal conditioning applications.
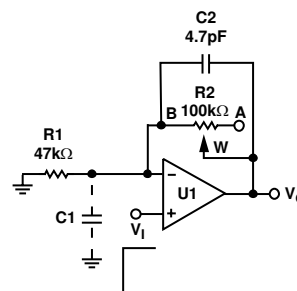

Figure 48. Typical Noninverting Gain Amplifier

In both applications, one of the digital potentiometer terminals is connected to the op amp inverting node with finite terminal capacitance, C1. It introduces a zero for the 1 β_o term with 20 dB/dec, whereas a typical op amp GBP has −20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Therefore, the rate of closure becomes 40 dB/dec and the system has a 0° phase margin at the crossover frequency. The output may ring, or in the worst case, oscillate when the input is a step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input. To reduce the effect of C1, users should also configure Terminal B or Terminal A rather than Terminal W at the inverting node.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor, C2, to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2, but this is not an option because of the variation of R2. As a result, users can use the relationship described and scale C2 as if R2 were at its maximum value. However, doing so may overcompensate by slowing down the settling time when R2 is set to low values. To avoid this problem, C2 should be found empirically for a given application. In general, setting C2 in the range of a few picofarads to no more than a few tenths of a picofarad is usually adequate for compensation.

There is also a Terminal W capacitance connected to the output (not shown); its effect on stability is less significant; therefore. compensation is not necessary unless the op amp is driving a large capacitive load.

PROGRAMMABLE LOW-PASS FILTER

In ADC applications, it is common to include an antialiasing filter to band-limit the sampling signal. To minimize various system redesigns, users can use two 1 kΩ AD5273s to construct a generic second-order Sallen key low-pass filter. Since the AD5273 is a single-supply device, the input must be dc offset when an ac signal is applied to avoid clipping at ground. This is illustrated in Figure 49. The design equations are

$$\frac{V_O}{V_I} = \frac{\omega_O{}^2}{S^2 + \frac{\omega_O}{Q}S + \omega_O{}^2} \tag{6}$$

$$\omega_O = \sqrt{\frac{1}{R1R2C1C2}} \tag{7}$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \tag{8}$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where Q = 0.707, let C1 be twice the size of C2 and let R1 = R2. As a result, R1 and R2 can be adjusted to the same setting to achieve the desired bandwidth.
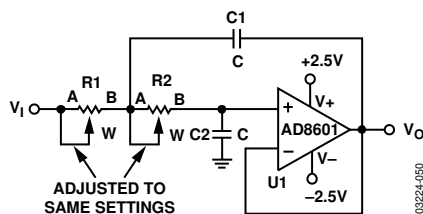

Figure 49. Sallen Key Low-Pass Filter

LEVEL SHIFT FOR DIFFERENT VOLTAGES OPERATION

If the SCL and SDA signals come from a low voltage logic controller and are below the minimum V_{IH} level (0.7 V × V_{DD}), level shift the signals for successful read/write communication between the AD5171 and the controller. Figure 50 shows one of the implementations. For example, when the SDA1 is 2.5 V, M1 turns off, and the SDA2 becomes 5 V. When the SDA1 is 0 V, M1 turns on, and the SDA2 approaches to 0 V. As a result, proper level shifting is established. M1 and M2 should be low threshold N-Ch power MOSFETs, such as FDV301N.
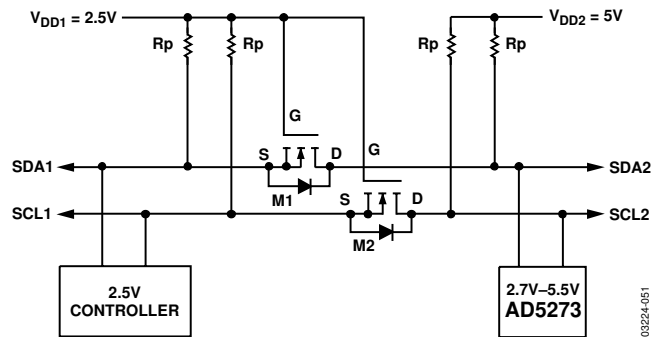

Figure 50. Level Shift for Different Voltages Operation

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the digital potentio-meters. Configured as a potentiometer divider, the −3 dB bandwidth of the AD5273 (1 kΩ resistor) measures 6 MHz at half scale. Figure 17 to Figure 20 provide the large signal BODE plot characteristics of the four available resistor versions 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. Figure 51 shows a parasitic simula-tion model. The code following Figure 51 provides a macro model net list for the 1 kΩ device.
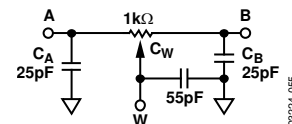

Figure 51. Circuit Simulation Model for RDAC = 1 kΩ

Macro Model Net List for RDAC

```
.PARAM D = 63, RDAC = 1E3
*
.SUBCKT DPOT (A,W,B)
*
CA A 0 25E-12
RWA A W {(1-D/63)*RDAC+60}
CW W 0 55E-12
RWB W B {D/63*RDAC+60}
CB B 0 25E-12
*
.ENDS DPOT
```
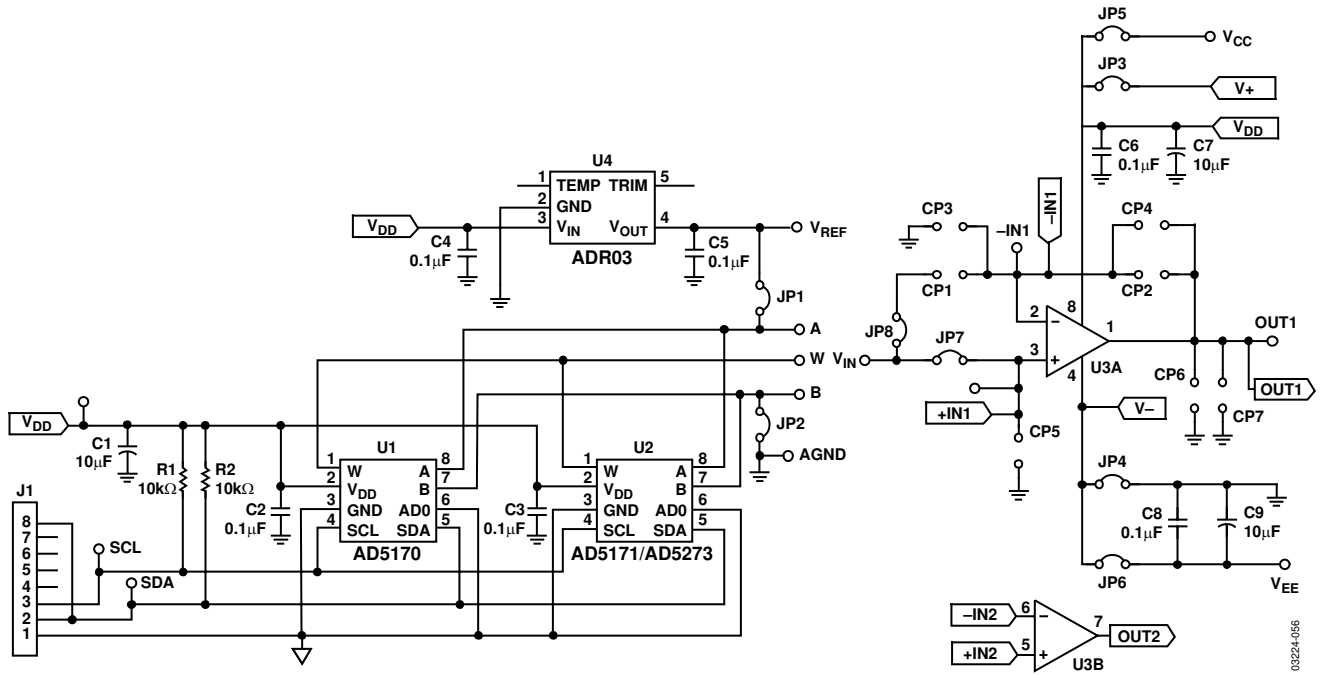
EVALUATION BOARD
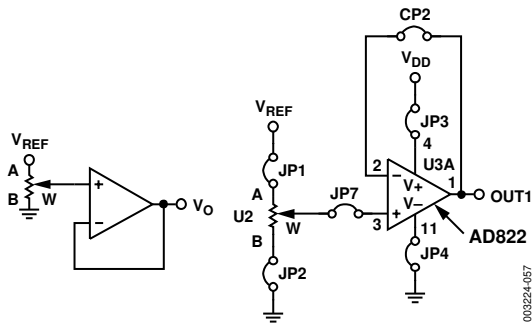

Figure 52. Evaluation Board Schematic

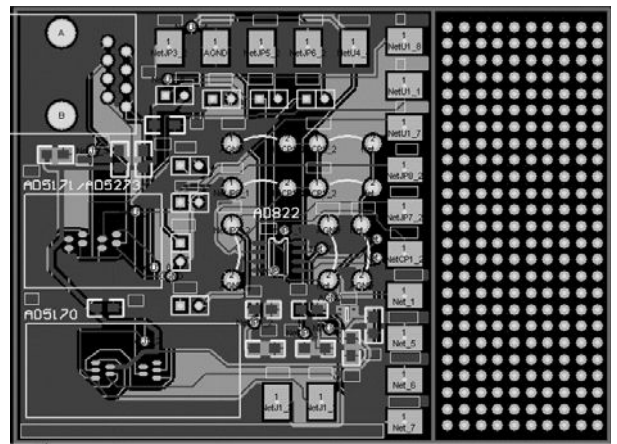*Figure 53. One Possible Configuration: Programmable Voltage Reference*
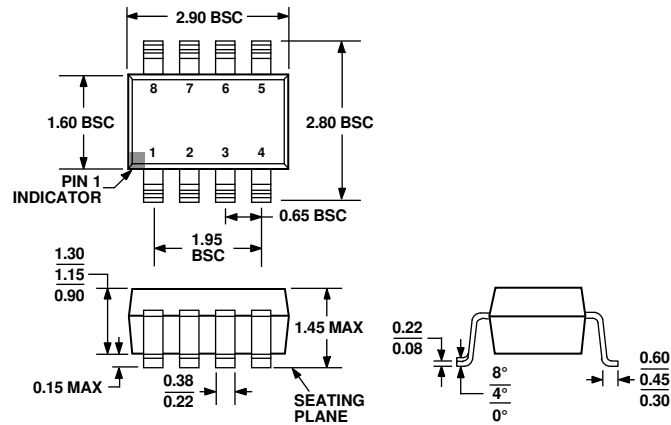

Figure 54. Evaluation Board

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-178BA

Figure 55. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Resistance R_{AB} (kΩ)	Package Option	Package Description	Quantity	Branding
AD5273BRJ1-R2	1	RJ-8	SOT-23	250	DYA
AD5273BRJ1-REEL7	1	RJ-8	SOT-23	3,000	DYA
AD5273BRJ10-R2	10	RJ-8	SOT-23	250	DYB
AD5273BRJ10-REEL7	10	RJ-8	SOT-23	3,000	DYB
AD5273BRJ50-R2	50	RJ-8	SOT-23	250	DYC
AD5273BRJ50-REEL7	50	RJ-8	SOT-23	3,000	DYC
AD5273BRJ100-R2	100	RJ-8	SOT-23	250	DYD
AD5273BRJ100-REEL7	100	RJ-8	SOT-23	3,000	DYD
AD5273EVAL[1]			Evaluation Board		

[1] Users should order samples because the evaluation kit comes with a socket, but does not include the parts.

NOTES

NOTES

ANALOG DEVICES

www.analog.com