Quad, 256 Tap, Low Voltage Digitally Controlled Potentiometer (XDCP™)

ISL23445

The ISL23445 is a volatile, low voltage, low noise, low power, 256 tap, quad digitally controlled potentiometer (DCP) with an SPI Bus™ interface. It integrates four DCP cores, wiper switches and control logic on a monolithic CMOS integrated circuit.

Each digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the SPI bus interface. Each potentiometer has an associated volatile Wiper Register (WRi, i = 0, 1, 2, 3) that can be directly written to and read by the user. The contents of the WRi controls the position of the wiper. When powered on, the wiper of each DCP will always commence at mid-scale (128 tap position).

The low voltage, low power consumption, and small package of the ISL23445 make it an ideal choice for use in battery operated equipment. In addition, the ISL23445 has a V_{LOGIC} pin allowing down to 1.2V bus operation, independent from the V_{CC} value. This allows for low logic levels to be connected directly to the ISL23445 without passing through a voltage level shifter.

The DCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Applications

- Power supply margining
- Trimming sensor circuits
- Gain adjustment in battery powered instruments
- RF power amplifier bias compensation

Features

- Four potentiometers per package
- 256 resistor taps
- 10kΩ, 50kΩ or 100kΩ total resistance
- SPI serial interface
  - No additional level translator for low bus supply
  - Daisy Chaining of multiple DCPs
- Maximum supply current without serial bus activity (standby)
  - 5µA @ V_{CC} and V_{LOGIC} = 5V
  - 2uA @ V_{CC} and V_{LOGIC} = 1.7V
- Shutdown Mode
  - Forces the DCP into an end-to-end open circuit and RWi is connected to RLi internally
  - Reduces power consumption by disconnecting the DCP resistor from the circuit
- Power supply
  - V_{CC} = 1.7V to 5.5V analog power supply
  - V_{LOGIC} = 1.2V to 5.5V SPI bus/logic power supply
- Wiper resistance: 70Ω typical @ V_{CC} = 3.3V
- Power-on preset to mid-scale (128 tap position)
- Extended industrial temperature range: -40°C to +125°C
- 20 Ld TSSOP or 20 Ld QFN packages
- Pb-free (RoHS compliant)

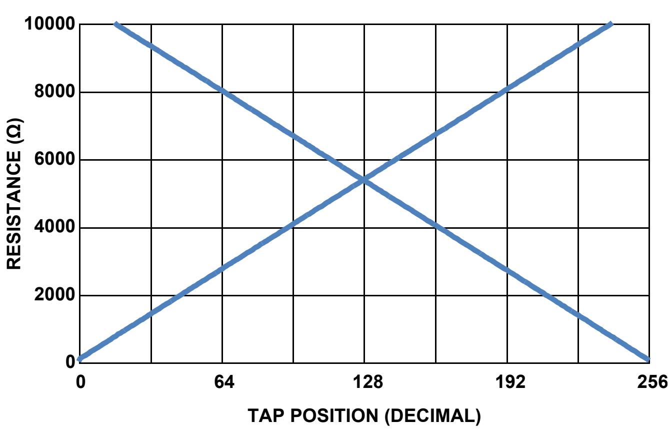


FIGURE 1. FORWARD AND BACKWARD RESISTANCE vs TAP POSITION, 10kΩ DCP

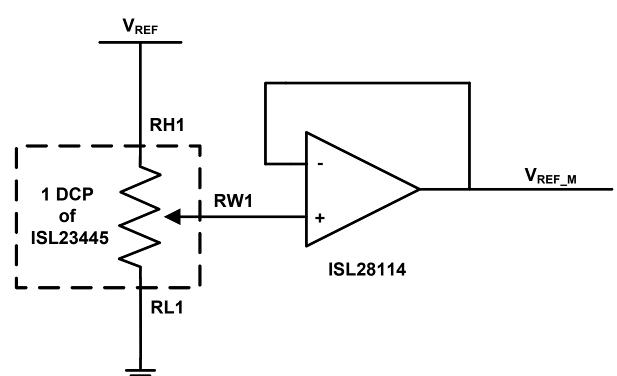
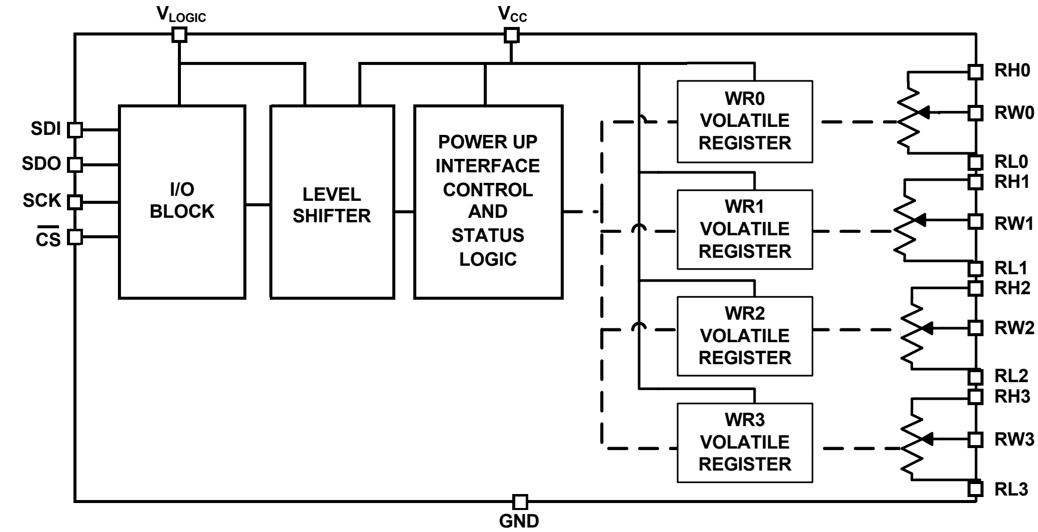


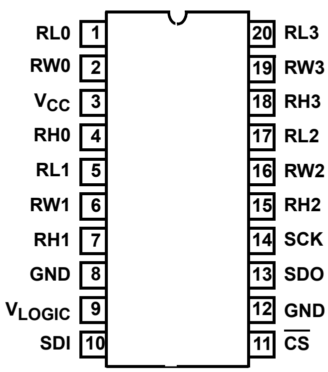
FIGURE 2. V_{REF} ADJUSTMENT

Block Diagram

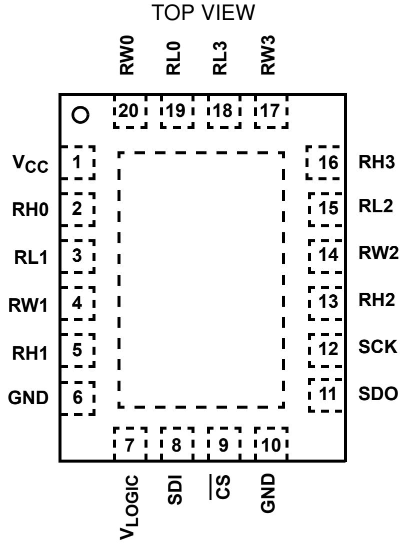


Pin Configurations

ISL23445
(20 LD TSSOP)
TOP VIEW



ISL23445
(20 LD QFN)
TOP VIEW



Pin Descriptions

TSSOP	QFN	SYMBOL	DESCRIPTION
1	19	RL0	DCP0 “low” terminal
2	20	RW0	DCP0 wiper terminal
3	1	V_{CC}	Analog power supply. Range 1.7V to 5.5V
4	2	RH0	DCP0 “high” terminal
5	3	RL1	DCP1 “low” terminal
6	4	RW1	DCP1 wiper terminal
7	5	RH1	DCP1 “high” terminal
8, 12	6, 10	GND	Ground pin
9	7	V_{LOGIC}	SPI bus /logic supply Range 1.2V to 5.5V
10	8	SDI	Logic Pin - Serial bus data input
11	9	$\overline{CS}$	Logic Pin - Active low chip select
13	11	SDO	Logic Pin - Serial bus data output (configurable)
14	12	SCK	Logic Pin - Serial bus clock input
15	13	RH2	DCP2 “high” terminal
16	14	RW2	DCP2 wiper terminal
17	15	RL2	DCP2 “low” terminal
18	16	RH3	DCP3 “high” terminal
19	17	RW3	DCP3 wiper terminal
20	18	RL3	DCP3 “low” terminal

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL23445TFVZ	23445 TFVZ	100	-40 to +125	20 Ld TSSOP	MDP0044
ISL23445UFVZ	23445 UFVZ	50	-40 to +125	20 Ld TSSOP	MDP0044
ISL23445WFVZ	23445 WFVZ	10	-40 to +125	20 Ld TSSOP	MDP0044
ISL23445TFRZ	445T	100	-40 to +125	20 Ld 3x4 QFN	L20.3x4
ISL23445UFRZ	445U	50	-40 to +125	20 Ld 3x4 QFN	L20.3x4
ISL23445WFRZ	445W	10	-40 to +125	20 Ld 3x4 QFN	L20.3x4

NOTES:

1. Add “-TK” suffix for 1k unit or “-T7A” suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL23445. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Supply Voltage Range
V_{CC} . . . . . -0.3V to 6.0V
V_{LOGIC} . . . . . -0.3V to 6.0V
Voltage on Any DCP Terminal Pin . . . . . -0.3V to 6.0V
Voltage on Any Digital Pins . . . . . -0.3V to 6.0V
Wiper Current I_W (10s) . . . . . ±6mA
ESD Rating
Human Body Model (Tested per JESD22-A114E) 6kV
CDM Model (Tested per JESD22-A114E) 1kV
Machine Model (Tested per JESD22-A115-A) 300V
Latch Up (Tested per JESD-78B; Class 2, Level A) . . . . 100mA @ +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld TSSOP Package (Notes 4, 7)	85	33
20 Ld QFN Package (Notes 5, 6)	40	4

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature . . . . . -40°C to +125°C
V_{CC} Supply Voltage . . . . . 1.7V to 5.5V
V_{LOGIC} Supply Voltage . . . . . 1.2V to 5.5V
DCP Terminal Voltage . . . . . 0 to V_{CC}
Max Wiper Current . . . . . ±3mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

Analog Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
R_{TOTAL}	RH to RL Resistance	W option		10		kΩ
		U option		50		kΩ
		T option		100		kΩ
	RH to RL Resistance Tolerance		**-20**	±2	**+20**	%
	End-to-End Temperature Coefficient	W option		125		ppm/°C
		U option		65		ppm/°C
		T option		45		ppm/°C
V_{RH}, V_{RL}	DCP Terminal Voltage	V_{RH} or V_{RL} to GND	**0**		**V_{CC}**	V
R_W	Wiper Resistance	RH - floating, V_{RL} = 0V, force I_W current to the wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$, V_{CC} = 2.7V to 5.5V		70	**200**	Ω
		V_{CC} = 1.7V		580		Ω
$C_H/C_L/C_W$	Terminal Capacitance	See "DCP Macro Model" on page 9		32/32/32		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V_{CC}	**-0.4**	< 0.1	**0.4**	µA
Noise	Resistor Noise Density	Wiper at middle point, W option		16		$nV/\sqrt{Hz}$
		Wiper at middle point, U option		49		$nV/\sqrt{Hz}$
		Wiper at middle point, T option		61		$nV/\sqrt{Hz}$
Feed Thru	Digital Feed-through from Bus to Wiper	Wiper at middle point		-65		dB
PSRR	Power Supply Reject Ratio	Wiper output change if V_{CC} change ±10%; wiper at middle point		-75		dB

Analog Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
VOLTAGE DIVIDER MODE (0V @ RL; V_{CC} @ RH; measured at RW, unloaded)						
INL (Note 13)	Integral Non-linearity, Guaranteed Monotonic	W option	**-1.0**	±0.5	**+1.0**	LSB (Note 9)
		U, T option	**-0.5**	±0.15	**+0.5**	LSB (Note 9)
DNL (Note 12)	Differential Non-linearity, Guaranteed Monotonic	W option	**-1**	±0.4	**+1**	LSB (Note 9)
		U, T option	**-0.4**	±0.1	**+0.4**	LSB (Note 9)
FSerror (Note 11)	Full-scale Error	W option	**-5**	-2	**0**	LSB (Note 9)
		U, T option	**-2**	-0.5	**0**	LSB (Note 9)
ZSerror (Note 10)	Zero-scale Error	W option	**0**	2	**5**	LSB (Note 9)
		U, T option	**0**	0.4	**2**	LSB (Note 9)
Vmatch (Note 22)	DCP to DCP Matching	DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals	**-2**	±0.5	**2**	LSB (Note 9)
TC_V (Note 14)	Ratiometric Temperature Coefficient	W option, Wiper Register set to 80 hex		8		ppm/°C
		U option, Wiper Register set to 80 hex		4		ppm/°C
		T option, Wiper Register set to 80 hex		2.3		ppm/°C
$t_{LS\_Settling}$	Large Signal Wiper Settling Time	From code 0 to FF hex, measured from 0 to 1LSB settling of the wiper		300		ns
f_{cutoff}	-3dB Cutoff Frequency	Wiper at middle point W option		1200		kHz
		Wiper at middle point U option		250		kHz
		Wiper at middle point T option		120		kHz
RHEOSTAT MODE (Measurements between RW and RL pins with RH not connected, or between RW and RH with RL not connected)						
R_{INL} (Note 18)	Integral Non-linearity, Guaranteed Monotonic	W option; V_{CC} = 2.7V to 5.5V	**-2.0**	±1	**+2.0**	MI (Note 15)
		W option; V_{CC} = 1.7V		10.5		MI (Note 15)
		U, T option; V_{CC} = 2.7V to 5.5V	**-1.0**	±0.3	**+1.0**	MI (Note 15)
		U, T option; V_{CC} = 1.7V		2.1		MI (Note 15)
R_{DNL} (Note 17)	Differential Non-linearity, Guaranteed Monotonic	W option; V_{CC} = 2.7V to 5.5V	**-1**	±0.4	**+1**	MI (Note 15)
		W option; V_{CC} = 1.7V		±0.6		MI (Note 15)
		U, T option; V_{CC} = 2.7V to 5.5V	**-0.5**	±0.15	**+0.5**	MI (Note 15)
		U, T option; V_{CC} = 1.7V		±0.35		MI (Note 15)

Analog Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
R_{offset} (Note 16)	Offset, wiper at 0 position	W option; V_{CC} = 2.7V to 5.5V	**0**	3	**5.5**	MI (Note 15)
		W option; V_{CC} = 1.7V		6.3		MI (Note 15)
		U, T option; V_{CC} = 2.7V to 5.5V	**0**	0.5	**2**	MI (Note 15)
		U, T option; V_{CC} = 1.7V		1.1		MI (Note 15)
Rmatch (Note 23)	DCP to DCP Matching	Any two DCPs at the same tap position with the same terminal voltages	**-2**	±0.5	**2**	LSB (Note 9)
TCR (Note 19)	Resistance Temperature Coefficient	W option; Wiper register set between 32 hex and FF hex		170		ppm/°C
		U option; Wiper register set between 32 hex and FF hex		80		ppm/°C
		T option; Wiper register set between 32 hex and FF hex		50		ppm/°C

Operating Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
I_{LOGIC}	V_{LOGIC} Supply Current (Write/Read)	V_{LOGIC} = 5.5V, V_{CC} = 5.5V, f_{SCK} = 5MHz (for SPI active read and write)			**1.5**	mA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, f_{SCK} = 1MHz (for SPI active read and write)			**30**	µA
I_{CC}	V_{CC} Supply Current (Write/Read)	V_{LOGIC} = 5.5V, V_{CC} = 5.5V			**110**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V			**10**	µA
$I_{LOGIC\ SB}$	V_{LOGIC} Standby Current	V_{LOGIC} = V_{CC} = 5.5V, SPI interface in standby			**2**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, SPI interface in standby			**0.5**	µA
$I_{CC\ SB}$	V_{CC} Standby Current	V_{LOGIC} = V_{CC} = 5.5V, SPI interface in standby			**3**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, SPI interface in standby			**1.5**	µA
$I_{LOGIC\ SHDN}$	V_{LOGIC} Shutdown Current	V_{LOGIC} = V_{CC} = 5.5V, SPI interface in standby			**2**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, SPI interface in standby			**0.5**	µA
$I_{CC\ SHDN}$	V_{CC} Shutdown Current	V_{LOGIC} = V_{CC} = 5.5V, SPI interface in standby			**3**	µA
		V_{LOGIC} = 1.2V, V_{CC} = 1.7V, SPI interface in standby			**1.5**	µA
I_{LkgDig}	Leakage Current, at Pins $\overline{CS}$, SDO, SDI, SCK	Voltage at pin from GND to V_{LOGIC}	**-0.4**	<0.1	**0.4**	µA

Operating Specifications

V_{CC} = 2.7V to 5.5V, V_{LOGIC} = 1.2V to 5.5V over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
t_{DCP}	Wiper Response Time	$\overline{CS}$ rising edge to the new position of the wiper (Changes from 10% to 90% FS) W, U, T options specified top to bottom		0.4		µs
				1.5		µs
				3.5		µs
tShdnRec	DCP Recall Time From Shutdown Mode	$\overline{CS}$ rising edge to wiper recalled position and RH connection		1.5		µs
V_{CC}, V_{LOGIC} Ramp	V_{CC} ,V_{LOGIC} Ramp Rate (Note 21)	Ramp monotonic at any level	**0.01**		**50**	V/ms

Serial Interface Specification

For SCK, SDI, SDO, $\overline{CS}$ Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
V_{IL}	Input LOW Voltage		-0.3		0.3 x V_{LOGIC}	V
V_{IH}	Input HIGH Voltage		0.7 x V_{LOGIC}		V_{LOGIC}+ 0.3	V
Hysteresis	SDI and SCK Input Buffer Hysteresis	V_{LOGIC} > 2V	0.05 x V_{LOGIC}			V
		V_{LOGIC} < 2V	0.1 x V_{LOGIC}			
V_{OL}	SDO Output Buffer LOW Voltage	I_{OL} = 3mA, V_{LOGIC} > 2V	0		0.4	V
		I_{OL} = 1.5mA, V_{LOGIC} < 2V			0.2 x V_{LOGIC}	V
R_{pu}	SDO Pull-up Resistor Off-chip	Maximum is determined by t_{RO} and t_{FO} with maximum bus load Cb = 30pF, f_{SCK} = 5MHz			1.5	kΩ
C_{pin}	SCK, SDO, SDI, $\overline{CS}$ Pin Capacitance			10		pF
f_{SCK}	SCK Frequency	V_{LOGIC} = 1.7V to 5.5V			5	MHz
		V_{LOGIC} = 1.2V to 1.6V			1	MHz
t_{CYC}	SPI Clock Cycle Time	V_{LOGIC} ≥ 1.7V	200			ns
t_{WH}	SPI Clock High Time	V_{LOGIC} ≥ 1.7V	100			ns
t_{WL}	SPI Clock Low Time	V_{LOGIC} ≥ 1.7V	100			ns
t_{LEAD}	Lead Time	V_{LOGIC} ≥ 1.7V	250			ns
t_{LAG}	Lag Time	V_{LOGIC} ≥ 1.7V	250			ns
t_{SU}	SDI, SCK and $\overline{CS}$ Input Setup Time	V_{LOGIC} ≥ 1.7V	50			ns
t_H	SDI, SCK and $\overline{CS}$ Input Hold Time	V_{LOGIC} ≥ 1.7V	50			ns
t_{RI}	SDI, SCK and $\overline{CS}$ Input Rise Time	V_{LOGIC} ≥ 1.7V	10			ns
t_{FI}	SDI, SCK and $\overline{CS}$ Input Fall Time	V_{LOGIC} ≥ 1.7V	10		20	ns
t_{DIS}	SDO Output Disable Time	V_{LOGIC} ≥ 1.7V	0		100	ns
t_{SO}	SDO Output Setup Time	V_{LOGIC} ≥ 1.7V	50			ns
t_V	SDO Output Valid Time	V_{LOGIC} ≥ 1.7V	150			ns
t_{HO}	SDO Output Hold Time	V_{LOGIC} ≥ 1.7V	0			ns
t_{RO}	SDO Output Rise Time	R_{pu} = 1.5k, Cbus = 30pF			60	ns
t_{FO}	SDO Output Fall Time	R_{pu} = 1.5k, Cbus = 30pF			60	ns

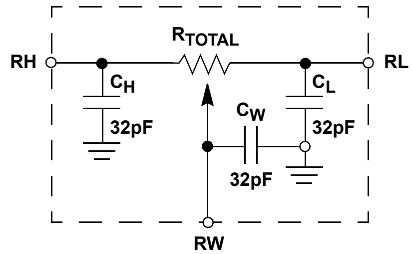
Serial Interface Specification For SCK, SDI, SDO, $\overline{CS}$ Unless Otherwise Noted. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP (Note 8)	MAX (Note 20)	UNITS
t_{CS}	$\overline{CS}$ Deselect Time		2			µs

NOTES:

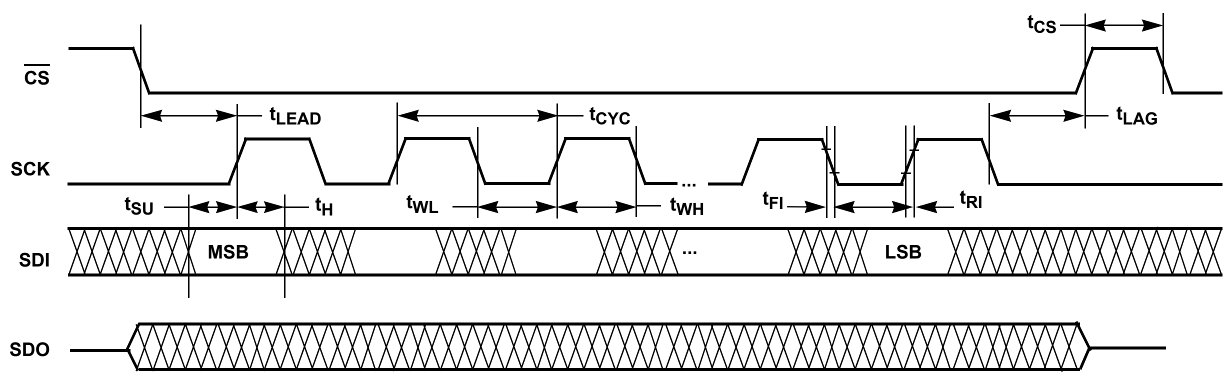
8. Typical values are for T_A = +25°C and 3.3V supply voltages.
9. LSB = $[V(RW)_{255} - V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
10. ZS error = $V(RW)_0/LSB$.
11. FS error = $[V(RW)_{255} - V_{CC}]/LSB$.
12. DNL = $[V(RW)_i - V(RW)_{i-1}]/LSB-1$, for i = 1 to 255. i is the DCP register setting.
13. INL = $[V(RW)_i - i \bullet LSB - V(RW)_0]/LSB$ for i = 1 to 255
14. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{V(RW_i(+25°C))} \times \frac{10^6}{+165°C}$ for i = 16 to 255 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min( ) is the minimum value of the wiper voltage over the temperature range.
15. MI = $|RW_{255} - RW_0|/255$. MI is a minimum increment. RW_{255} and RW_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
16. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{255}/MI, when measuring between RW and RH.
17. RDNL = $(RW_i - RW_{i-1})/MI - 1$, for i = 16 to 255.
18. RINL = $[RW_i - (MI \bullet i) - RW_0]/MI$, for i = 16 to 255.
19. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{Ri(+25°C)} \times \frac{10^6}{+165°C}$ for i = 16 to 255, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min( ) is the minimum value of the resistance over the temperature range.
20. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
21. It is preferable to ramp up both the V_{LOGIC} and the V_{CC} supplies at the same time. If this is not possible, it is recommended to ramp-up the V_{LOGIC} first followed by the V_{CC}.
22. VMATCH = [V(RWx)i - V(RWy)i]/LSB, for i = 1 to 255, x = 0 to 3 and y = 0 to 3.
23. RMATCH = (RWi,x - RWi,y)/MI, for i = 1 to 255 , x = 0 to 3 and y = 0 to 3.

DCP Macro Model

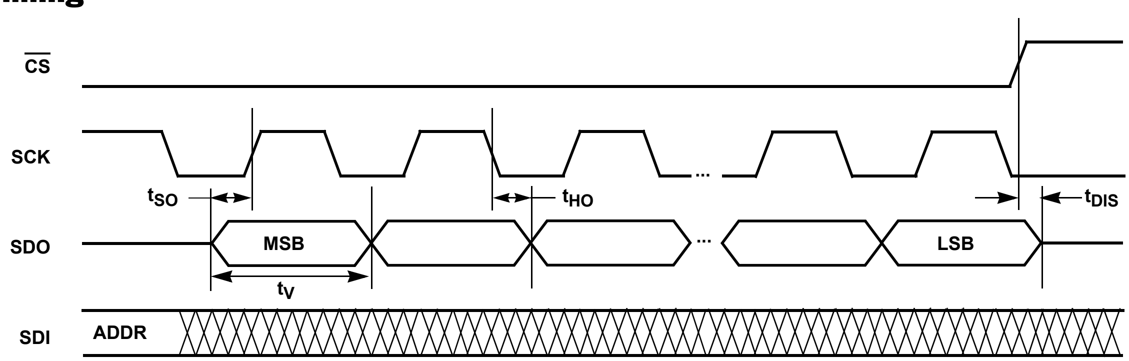


Timing Diagrams

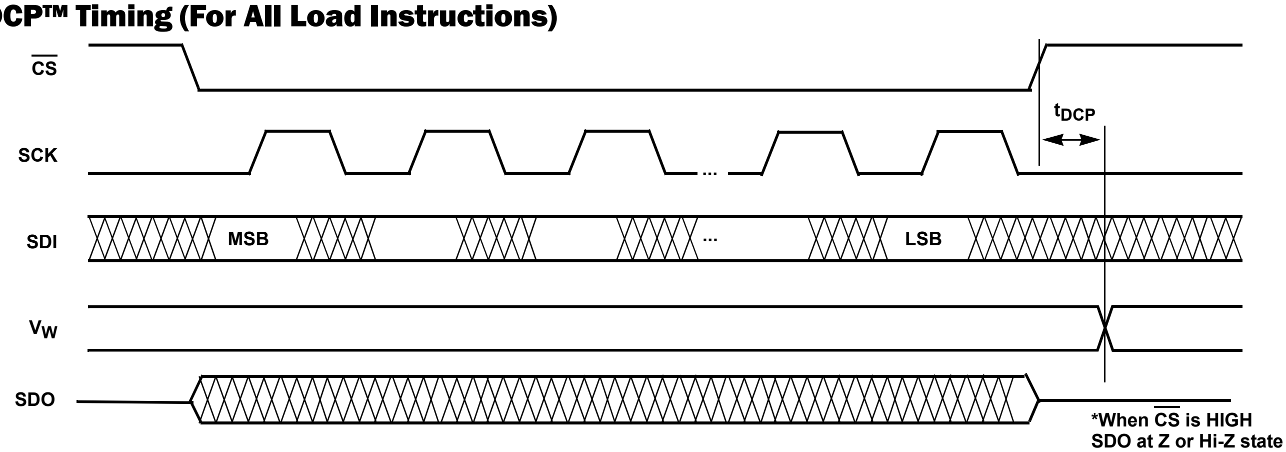
Input Timing



Output Timing



XDCP™ Timing (For All Load Instructions)



Typical Performance Curves

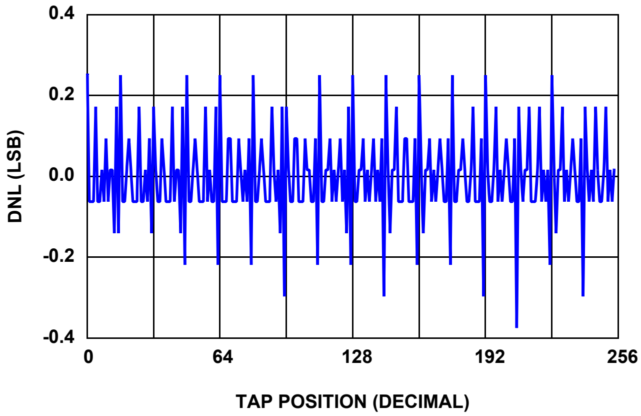


FIGURE 3. 10kΩ DNL vs TAP POSITION, V_{CC} = 3.3V, +25°C

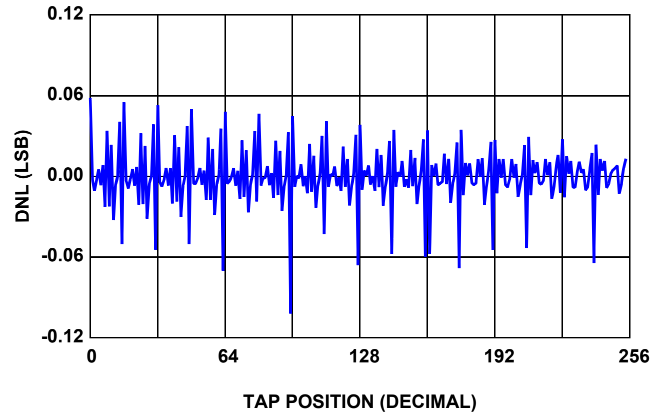


FIGURE 4. 50kΩ DNL vs TAP POSITION, V_{CC} = 3.3V, +25°C

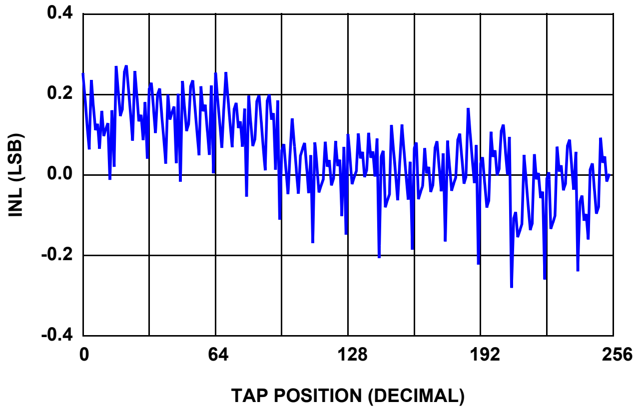


FIGURE 5. 10kΩ INL vs TAP POSITION, V_{CC} = 3.3V, +25°C

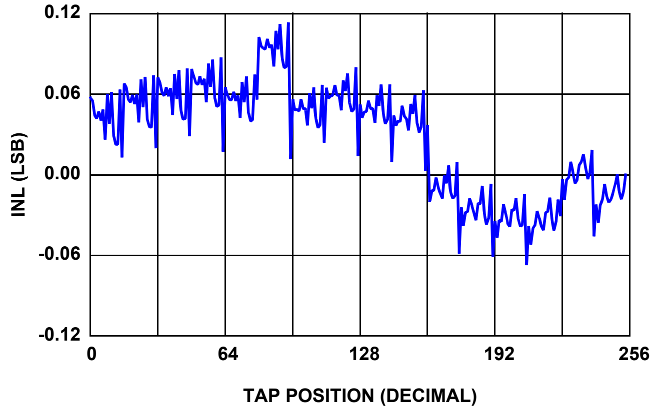


FIGURE 6. 50kΩ INL vs TAP POSITION, V_{CC} = 3.3V, +25°C

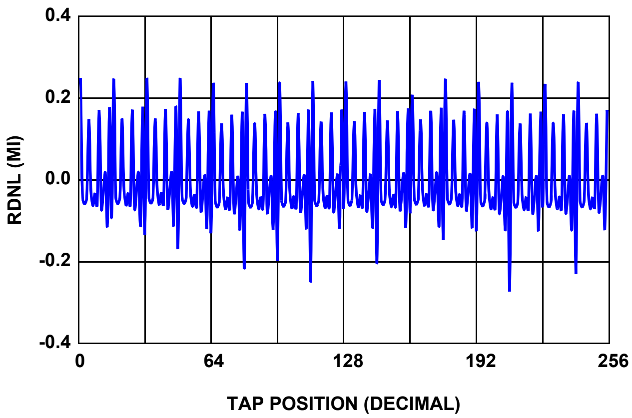


FIGURE 7. 10kΩ RDNL vs TAP POSITION, V_{CC} = 3.3V, +25°C

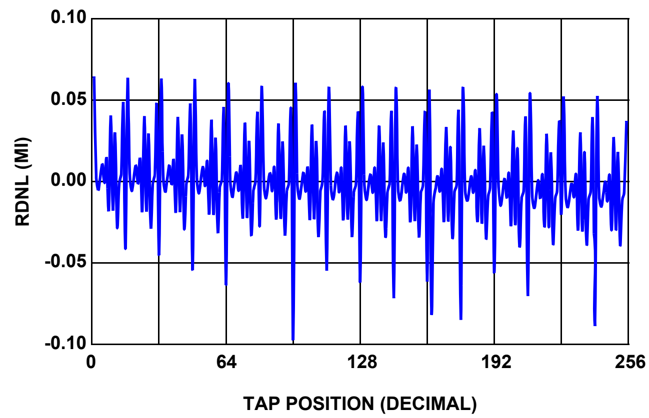


FIGURE 8. 50kΩ RDNL vs TAP POSITION, V_{CC} = 3.3V, +25°C

Typical Performance Curves (Continued)

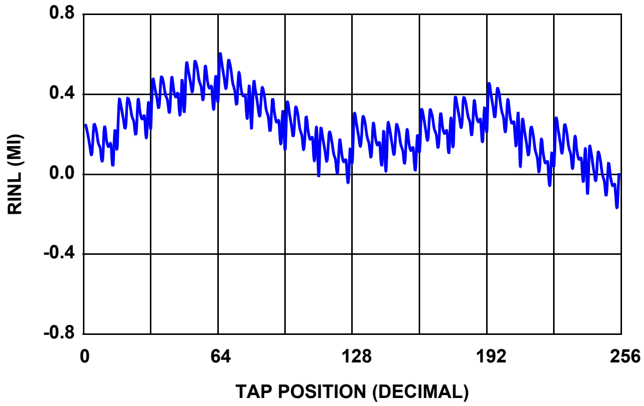


FIGURE 9. 10kΩ RINL vs TAP POSITION, V_{CC} = 3.3V, +25°C

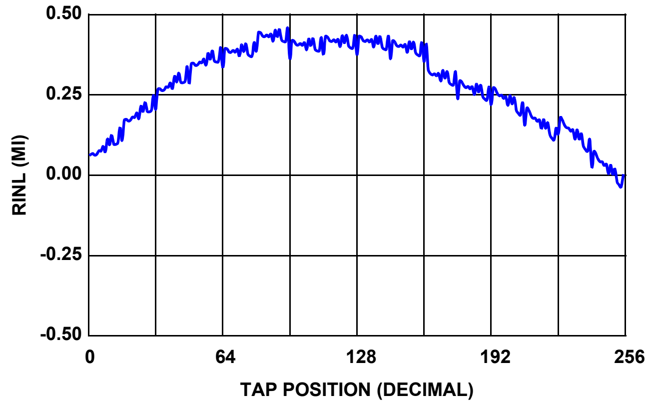


FIGURE 10. 50kΩ RINL vs TAP POSITION, V_{CC} = 3.3V, +25°C

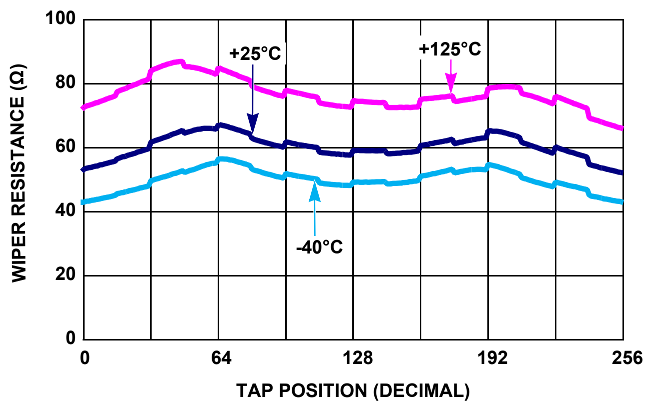


FIGURE 11. 10kΩ WIPER RESISTANCE vs TAP POSITION, V_{CC} = 3.3V

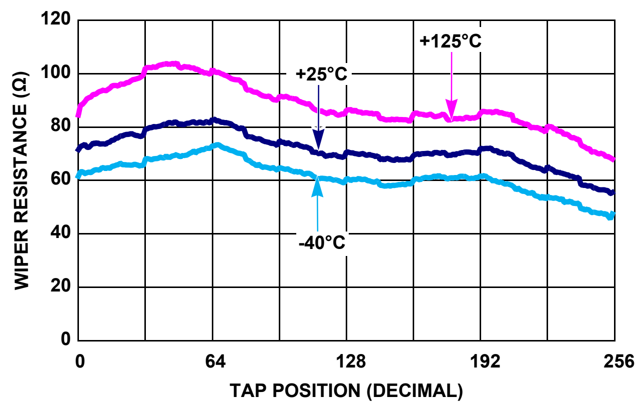


FIGURE 12. 50kΩ WIPER RESISTANCE vs TAP POSITION, V_{CC} = 3.3V

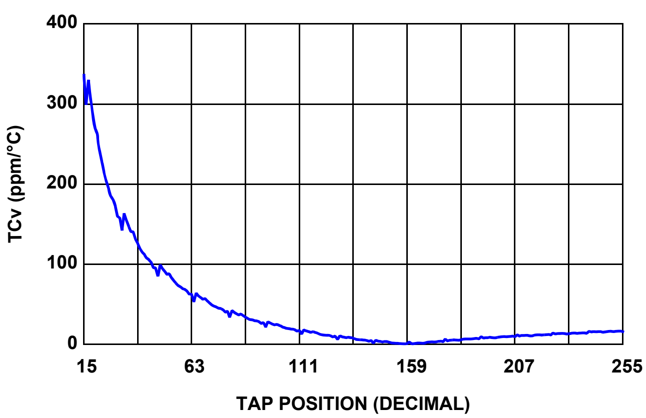


FIGURE 13. 10kΩ TCv vs TAP POSITION, V_{CC} = 3.3V

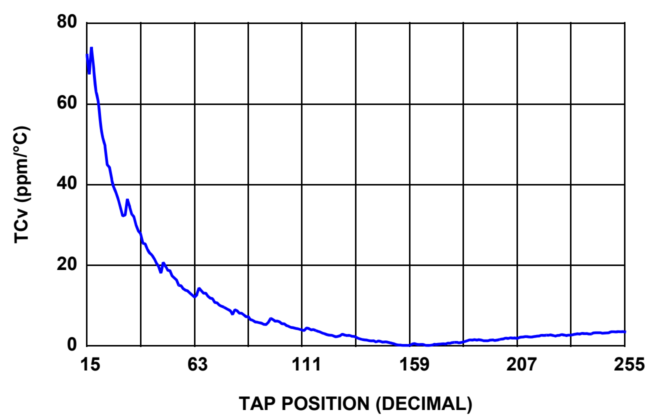


FIGURE 14. 50kΩ TCv vs TAP POSITION, V_{CC} = 3.3V

Typical Performance Curves (Continued)

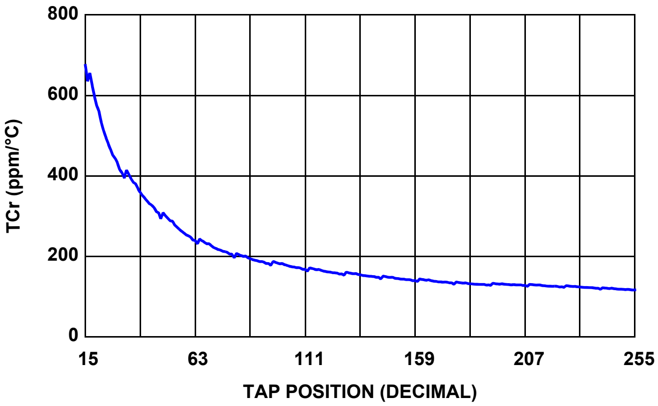


FIGURE 15. 10kΩ TCr vs TAP POSITION

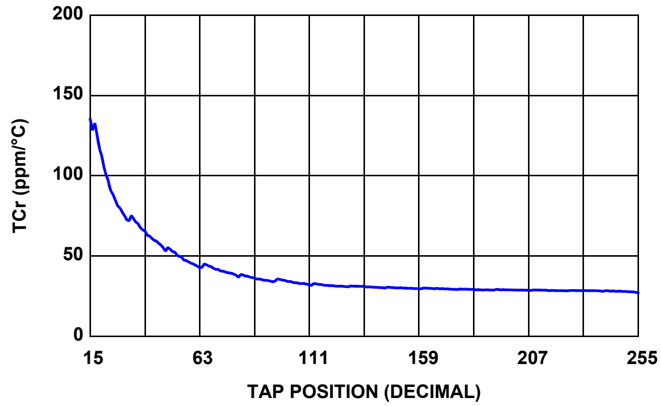


FIGURE 16. 50kΩ TCr vs TAP POSITION, V_{CC} = 3.3V

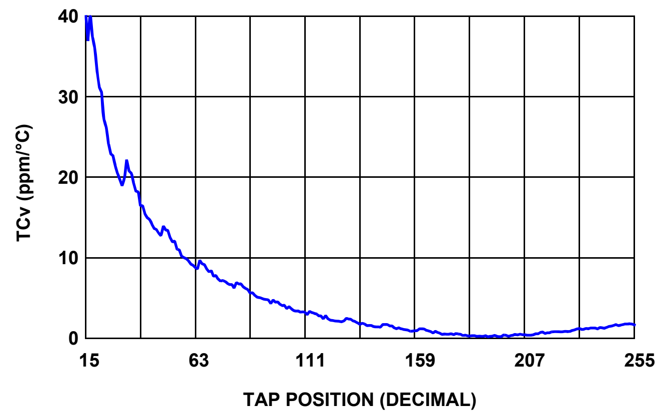


FIGURE 17. 100kΩ TCv vs TAP POSITION, V_{CC} = 3.3V

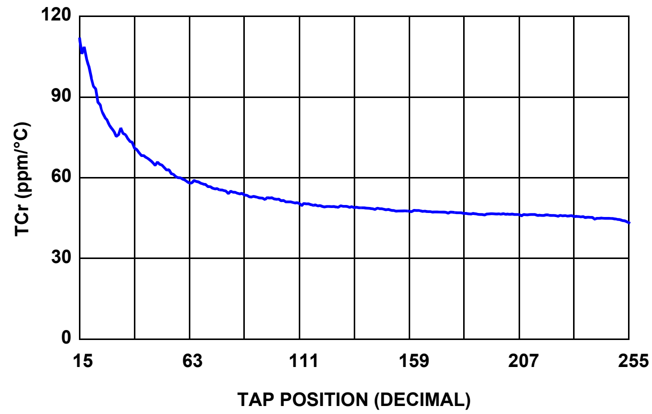


FIGURE 18. 100kΩ TCr vs TAP POSITION, V_{CC} = 3.3V

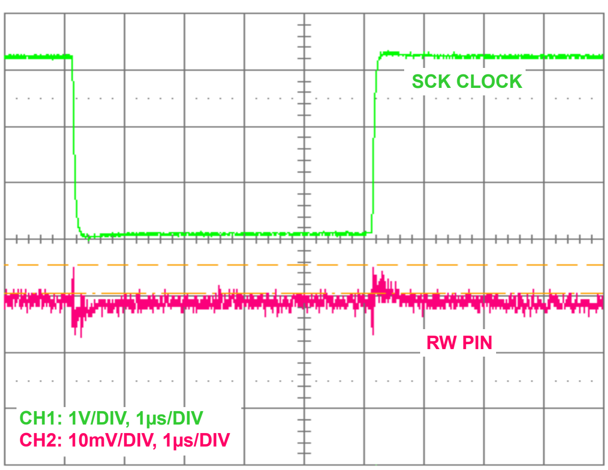


FIGURE 19. WIPER DIGITAL FEED-THROUGH

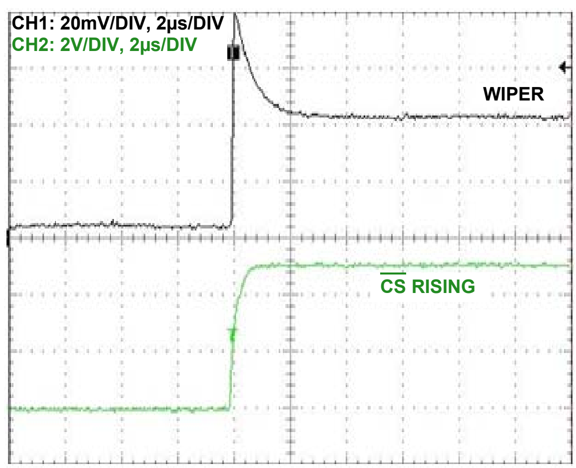


FIGURE 20. WIPER TRANSITION GLITCH

Typical Performance Curves (Continued)

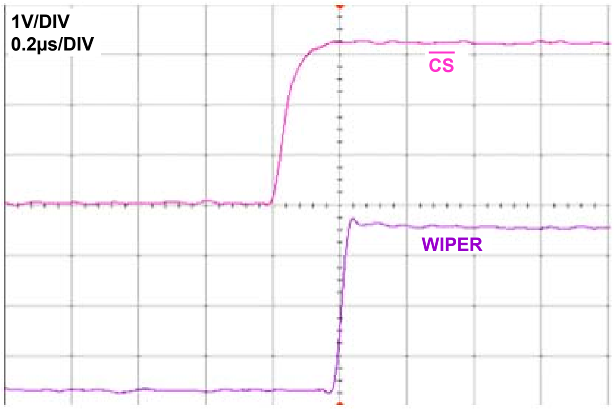


FIGURE 21. WIPER LARGE SIGNAL SETTLING TIME

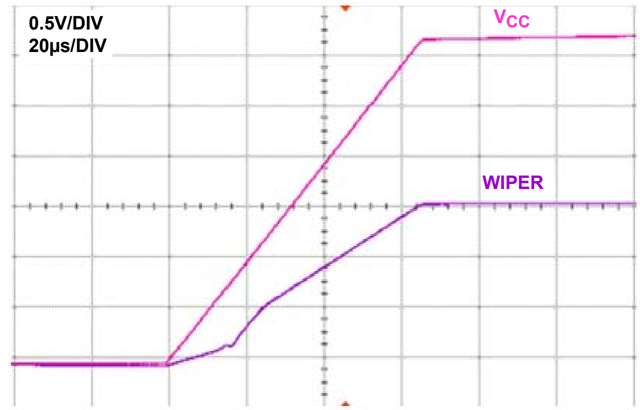


FIGURE 22. POWER-ON START-UP IN VOLTAGE DIVIDER MODE

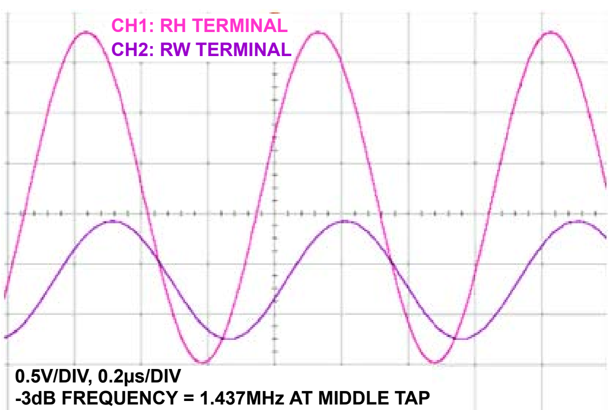


FIGURE 23. 10kΩ -3dB CUT OFF FREQUENCY

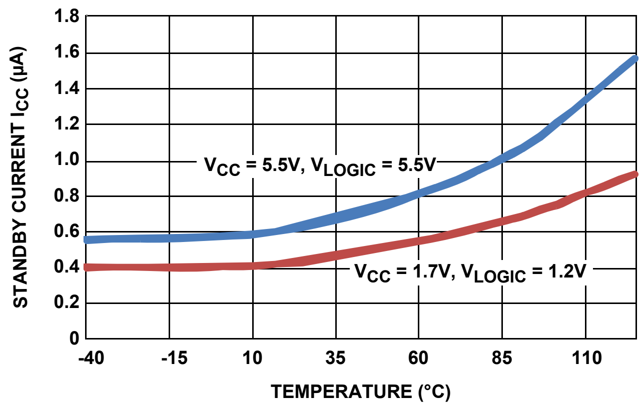


FIGURE 24. STANDBY CURRENT vs TEMPERATURE

Functional Pin Descriptions

Potentiometers Pins

RHi AND RLi

The high (RHi, i = 0, 1, 2, 3) and low (RLi, i = 0, 1, 2, 3) terminals of the ISL23445 are equivalent to the fixed terminals of a mechanical potentiometer. RHi and RLi are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WRi set to 255 decimal, the wiper will be closest to RHi, and with the WRi set to 0, the wiper is closest to RLi.

RWi

RWi (i = 0, 1, 2, 3) is the wiper terminal, and it is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

Power Pins

V_{CC}

Power terminal for the potentiometer section analog power source. Can be any value needed to support the voltage range of the DCP pins, from 1.7V to 5.5V, independent of the V_{LOGIC} voltage.

Bus Interface Pins

SERIAL CLOCK (SCK)

This input is the serial clock of the SPI serial interface.

SERIAL DATA INPUT (SDI)

The SDI is a serial data input pin for SPI interface. It receives operation code, wiper address and data from the SPI remote host device. The data bits are shifted in at the rising edge of the serial clock SCK, while the $\overline{CS}$ input is low.

SERIAL DATA OUTPUT (SDO)

The SDO is a serial data output pin. During a read cycle, the data bits are shifted out on the falling edge of the serial clock SCK and will be available to the master on the following rising edge of SCK.

The output type is configured through ACR[1] bit for Push-Pull or Open Drain operation. The default setting for this pin is Push-Pull. An external pull-up resistor is required for Open Drain output operation. When $\overline{CS}$ is HIGH, the SDO pin is in tri-state (Z) or high-tri-state (Hi-Z) depending on the selected configuration.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ LOW enables the ISL23445, placing it in the active power mode. A HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation after power-up. When $\overline{CS}$ is HIGH, the ISL23445 is deselected and the SDO pin is at high impedance, and the device will be in the standby state.

V_{LOGIC}

Digital power source for the logic control section. It supplies an internal level translator for 1.2V to 5.5V serial bus operation. Use the same supply as the I^2C logic source.

Principles of Operation

The ISL23445 is an integrated circuit incorporating four DCPs with its associated registers and an SPI serial interface providing direct communication between a host and the potentiometer. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make-before-break” mode when the wiper changes tap positions.

Voltage at any of the DCP pins, RHi, RLi or RWi, should not exceed V_{CC} level at any conditions during power-up and normal operation.

The V_{LOGIC} pin is the terminal for the logic control digital power source. It should use the same supply as the SPI logic source, which allows reliable communication with a wide range of microcontrollers and is independent from the V_{CC} level. This is extremely important in systems where the master supply has lower levels than the DCP analog supply.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RHi and RLi pins). The RWi pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WRi). When the WR of a DCP contains all zeroes (WRi[7:0] = 00h), its wiper terminal (RWi) is closest to its “Low” terminal (RLi). When the WRi register of a DCP contains all ones (WRi[7:0] = FFh), its wiper terminal (RWi) is closest to its “High” terminal (RHi). As the value of the WRi increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to RLi to the position closest to RHi. At the same time, the resistance between RWi and RLi increases monotonically, while the resistance between RHi and RWi decreases monotonically.

While the ISL23445 is being powered up, both WRi are reset to 80h (128 decimal), which positions RWi at the center between RLi and RHi.

The WRi can be read or written to directly using the SPI serial interface as described in the following sections.

Memory Description

The ISL23445 contains five volatile 8-bit registers: Wiper Register WR0, Wiper Register WR1, Wiper Register WR2, Wiper Register WR3 and Access Control Register (ACR). The memory map of ISL23445 is shown in Table 1. The Wiper Register WRi at address i, contains current wiper position of DCPi (i = 0, 1, 2, 3). The Access Control Register (ACR) at address 10h contains information and control bits described in Table 2.

TABLE 1. MEMORY MAP

ADDRESS (hex)	VOLATILE REGISTER NAME	DEFAULT SETTING (hex)
10	ACR	40
3	WR3	80
2	WR2	80
1	WR1	80
0	WR0	80

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
NAME/ VALUE	0	$\overline{SHDN}$	0	0	0	0	SDO	0

The SDO bit (ACR[1]) configures the type of SDO output pin. The default value of SDO bit is 0 for Push-Pull output. The SDO pin can be configured as Open Drain output for some applications. In this case, an external pull-up resistor is required. Reference the “Serial Interface Specification” on page 7.

Shutdown Function

The $\overline{SHDN}$ bit (ACR[6]) disables or enables shutdown mode for all DCP channels simultaneously. When this bit is 0, i.e. each DCP is forced to end-to-end open circuit and each RW shorted to RL through a 2kΩ serial resistor, as shown in Figure 25. The default value of the $\overline{SHDN}$ bit is 1.

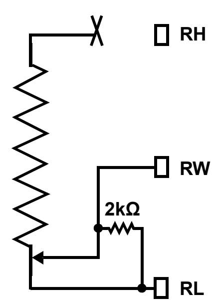


FIGURE 25. DCP CONNECTION IN SHUTDOWN MODE

When the device enters shutdown, all current DCP WR settings are maintained. When the device exits shutdown, the wipers will return to the previous WR settings after a short settling time (see Figure 26).

In shutdown mode, if there is a glitch on the power supply which causes it to drop below 1.3V for more than 0.2 to 0.4µs the wipers will be RESET to their mid position. This is done to avoid an undefined state at the wiper outputs.

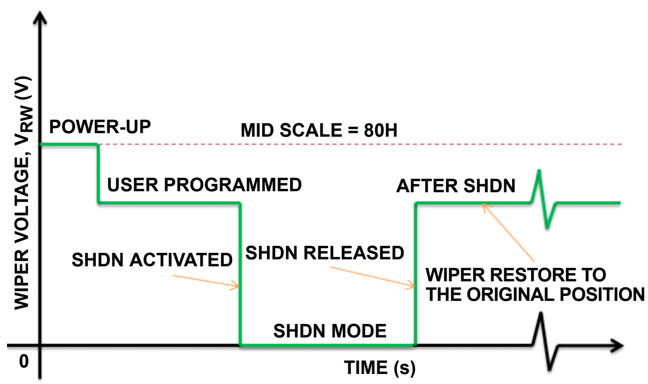


FIGURE 26. SHUTDOWN MODE WIPER RESPONSE

SPI Serial Interface

The ISL23445 supports an SPI serial protocol, mode 0. The device is accessed via the SDI input and SDO output with data clocked in on the rising edge of SCK, and clocked out on the falling edge of SCK. $\overline{CS}$ must be LOW during communication with the ISL23445. The SCK and $\overline{CS}$ lines are controlled by the host or master. The ISL23445 operates only as a slave device.

All communication over the SPI interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

The SPI protocol contains Instruction Byte followed by one or more Data Bytes. A valid Instruction Byte contains instruction as the three MSBs, with the following five register address bits (see Table 3).

The next byte sent to the ISL23445 is the Data Byte.

TABLE 3. INSTRUCTION BYTE FORMAT

BIT #	7	6	5	4	3	2	1	0
	I2	I1	I0	R4	R3	R2	R1	R0

Table 4 contains a valid instruction set for ISL23445.

If the [R4:R0] bits are zero, one, two or three then the read or write is to the WRi register. If the [R4:R0] are 10000, then the operation is to the ACR.

Write Operation

A write operation to the ISL23445 is a two or more bytes operation. First, it requires that the $\overline{CS}$ transition from HIGH-to-LOW. Then, the host sends a valid Instruction Byte, followed by one or more Data Bytes to the SDI pin. The host terminates the write operation by pulling the $\overline{CS}$ pin from LOW-to-HIGH. Instruction is executed on the rising edge of $\overline{CS}$ (see Figure 27).

Read Operation

A Read operation to the ISL23445 is a four byte operation. First, it requires that the $\overline{CS}$ transition from HIGH-to-LOW. Then, the host sends a valid Instruction Byte, followed by a “dummy” Data Byte, NOP Instruction Byte and another “dummy” Data Byte to the SDI pin. The SPI host receives the Instruction Byte (instruction code + register address) and requested Data Byte from the SDO pin on the rising edge of SCK during the third and fourth bytes, respectively. The host terminates the read by pulling the $\overline{CS}$ pin from LOW-to-HIGH (see Figure 28).

TABLE 4. INSTRUCTION SET

INSTRUCTION SET								OPERATION
I2	I1	I0	R4	R3	R2	R1	R0	
0	0	0	X	X	X	X	X	NOP
0	0	1	X	X	X	X	X	ACR READ
0	1	1	X	X	X	X	X	ACR WRTE
1	0	0	R4	R3	R2	R1	R0	WRi or ACR READ
1	1	0	R4	R3	R2	R1	R0	WRi or ACR WRTE

where X means “do not care”.

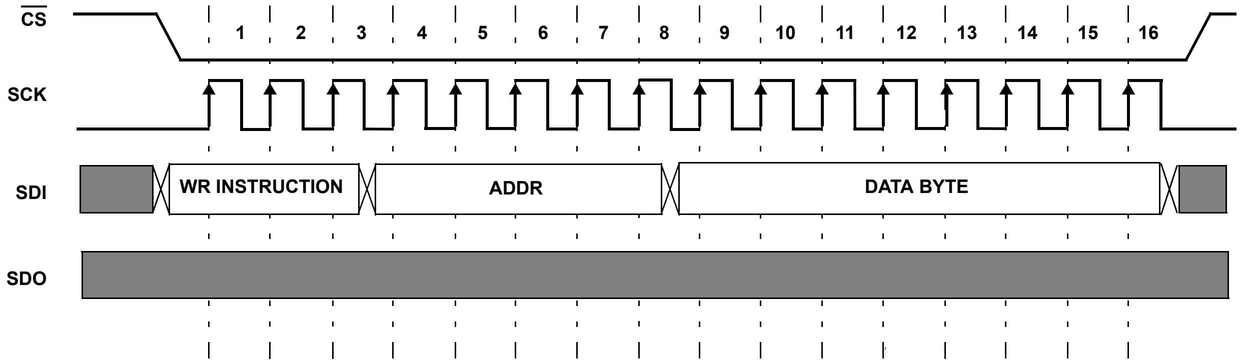


FIGURE 27. TWO BYTE WRITE SEQUENCE

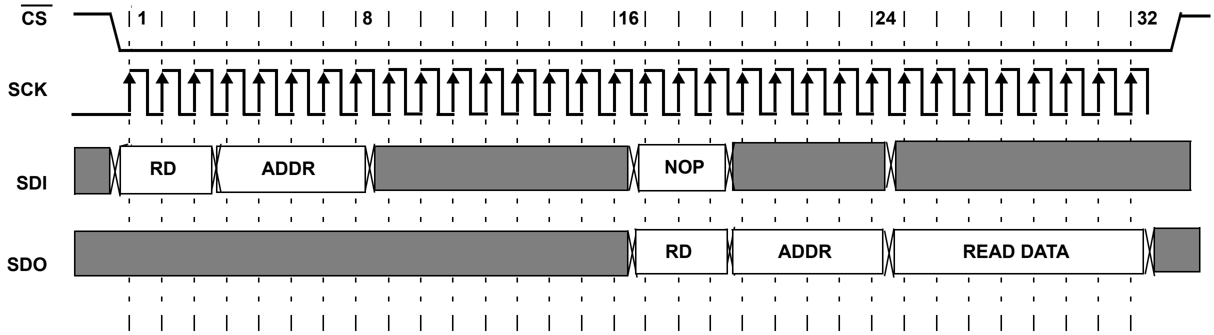


FIGURE 28. FOUR BYTE READ SEQUENCE

Applications Information

Communicating with ISL23445

Communication with ISL23445 proceeds using SPI interface through the ACR (address 10000b), WR0 (addresses 00000b), WR1 (addresses 00001b), WR2 (addresses 00010b), WR3 (addresses 00011b) registers.

The wiper of the potentiometer is controlled by the WRi register. Writes and reads can be made directly to these registers to control and monitor the wiper position.

Daisy Chain Configuration

When an application needs more than one ISL23445, it can communicate with all of them without additional $\overline{CS}$ lines by daisy chaining the DCPs, as shown in Figure 29. In Daisy Chain configuration, the SDO pin of the previous chip is connected to the SDI pin of the following chip, and each $\overline{CS}$ and SCK pins are connected to the corresponding microcontroller pins in parallel, like regular SPI interface implementation. The Daisy Chain configuration can also be used for simultaneous setting of multiple DCPs. Note, the number of daisy chained DCPs is limited only by the driving capabilities of SCK and $\overline{CS}$ pins of microcontroller; for larger number of SPI devices, buffering of SCK and $\overline{CS}$ lines is required.

Daisy Chain Write Operation

The write operation starts by a HIGH-to-LOW transition on the $\overline{CS}$ line, followed by N number of two bytes write instructions on the SDI line with reversed chain access sequence: the instruction byte + data byte for the last DCP in chain is going first, as shown in Figure 30, where N is a number of DCPs in chain. The serial data is going through DCPs from DCP0 to DCP(N-1) as follows: DCP0 –> DCP1 –> DCP2 –> ... –> DCP(N-1). The write instruction is executed on the rising edge of $\overline{CS}$ for all N DCPs simultaneously.

Daisy Chain Read Operation

The read operation consists of two parts: first, send the read instructions (N two bytes operation) with valid address; second, read the requested data while sending NOP instructions (N two bytes operation), as shown in Figures 31 and 32.

The first part starts by a HIGH-to-LOW transition on the $\overline{CS}$ line, followed by N two bytes read instruction on the SDI line with reversed chain access sequence: the instruction byte + dummy data byte for the last DCP in chain is going first, followed by a LOW-to-HIGH transition on the $\overline{CS}$ line. The read instructions are executed during the second part of the read sequence. It also starts by a HIGH-to-LOW transition on the $\overline{CS}$ line, followed by N number of two bytes NOP instructions on the SDI line and LOW-to-HIGH transition of $\overline{CS}$. The data is read on every even byte during the second part of the read sequence while every odd byte contains code 111b followed by the address from which the data is being read.

Wiper Transition

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients, or overshoot/undershoot, resulting from the sudden transition from a very low impedance "make" to a much higher impedance "break" within a short period of time (<1µs). There are several code transitions such as 0Fh to 10h, 1Fh to 20h,..., EFh to FFh, which have higher transient glitch. Note, that all switching transients will settle well within the settling time as stated in the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients, but that will also reduce the useful bandwidth of the circuit, thus, this may not be a good solution for some applications. It may be a good idea, in this case, to use fast amplifiers in a signal chain for fast recovery.

V_{LOGIC} Requirements

It is recommended to keep V_{LOGIC} powered all the time during normal operation. In a case where turning V_{LOGIC} OFF is necessary, it is recommended to ground the V_{LOGIC} pin of the ISL23445. Grounding the V_{LOGIC} pin or both V_{LOGIC} and V_{CC} does not affect other devices on the same bus. It is good practice to put a 1µF capacitor in parallel with 0.1µF decoupling capacitor close to the V_{LOGIC} pin.

V_{CC} Requirements and Placement

It is recommended to put a 1µF capacitor in parallel with 0.1µF decoupling capacitor close to the V_{CC} pin.

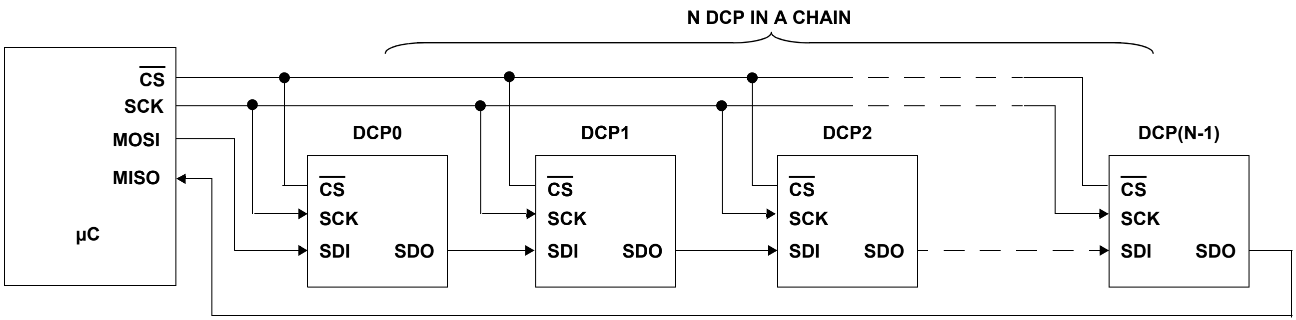


FIGURE 29. DAISY CHAIN CONFIGURATION

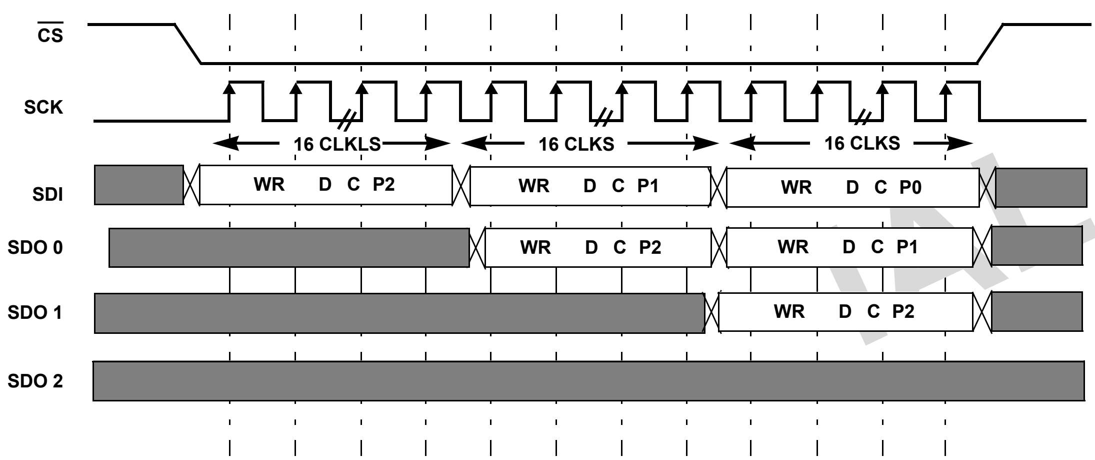


FIGURE 30. DAISY CHAIN WRITE SEQUENCE OF N = 3 DCP

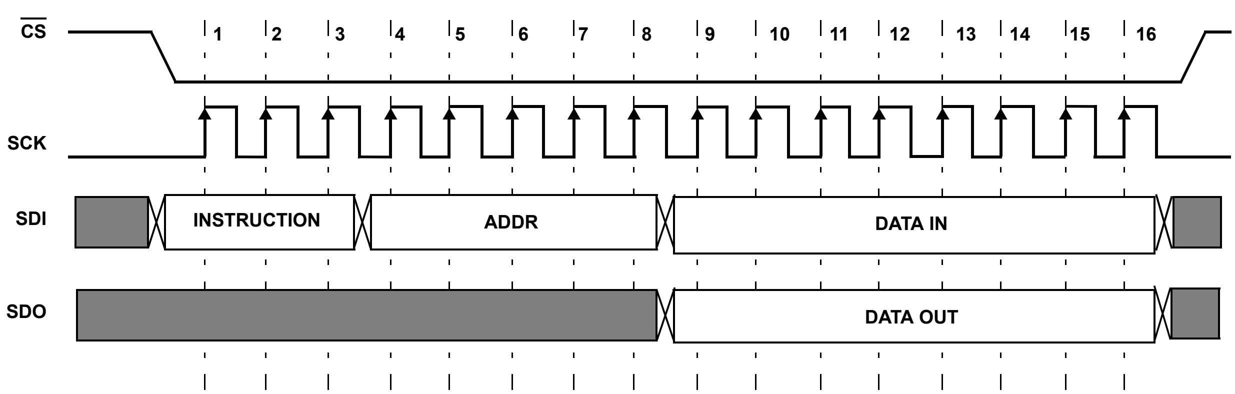


FIGURE 31. TWO BYTE READ INSTRUCTION

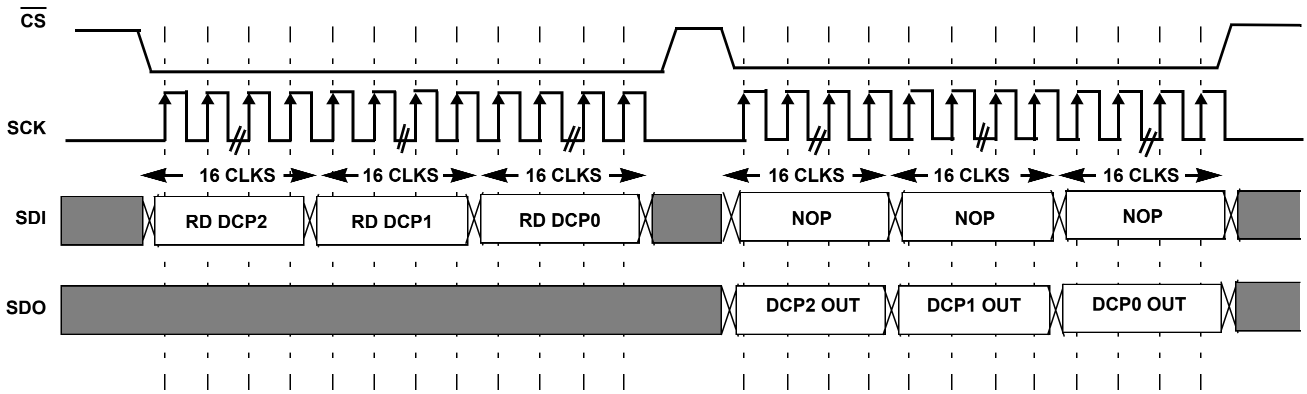


FIGURE 32. DAISY CHAIN READ SEQUENCE OF N = 3 DCP

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
June 21, 2011	FN7874.0	Initial release.

Products

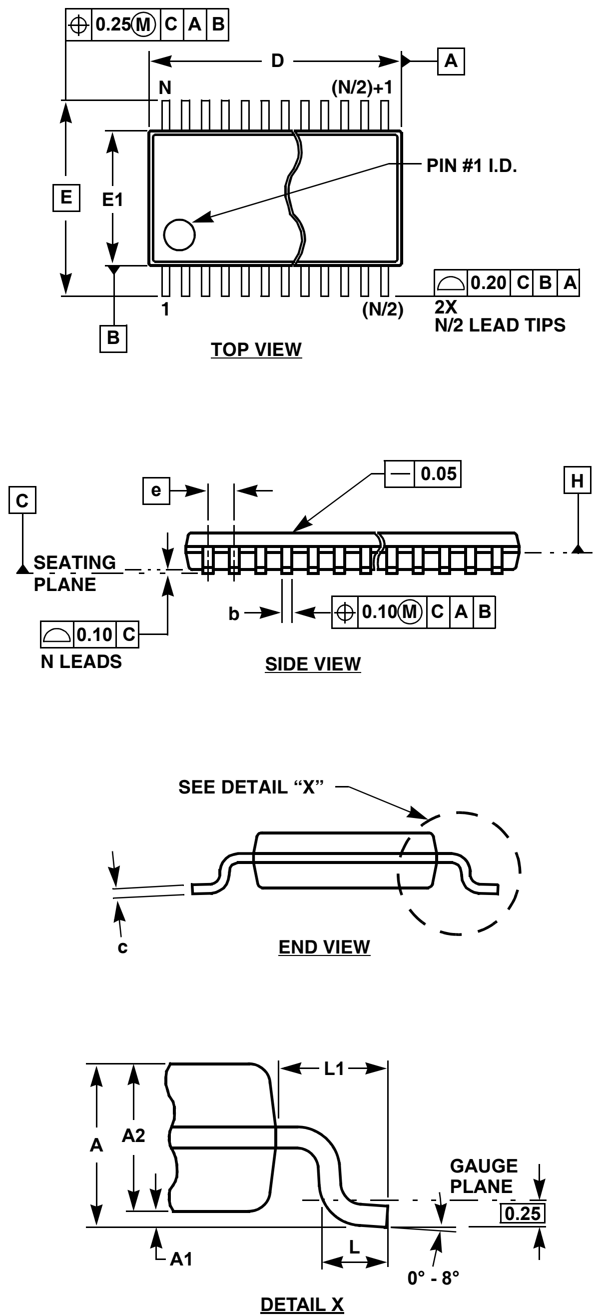
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL23445

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

Thin Shrink Small Outline Package Family (TSSOP)



MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

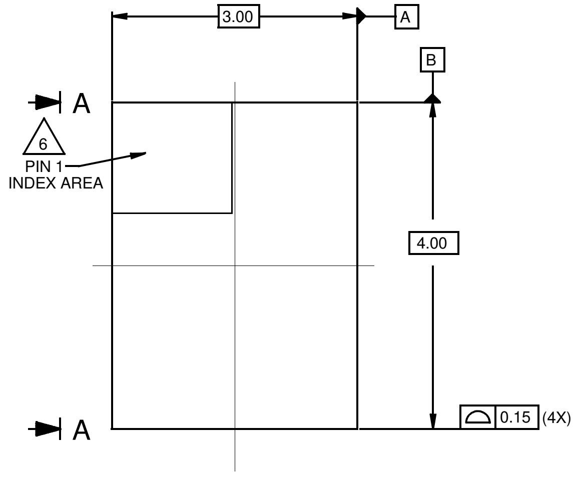
NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

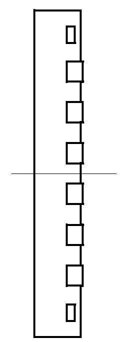
Package Outline Drawing

L20.3x4

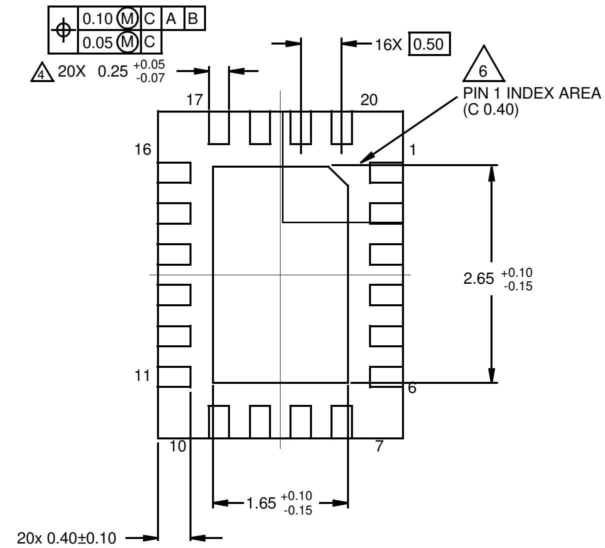
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 3/10



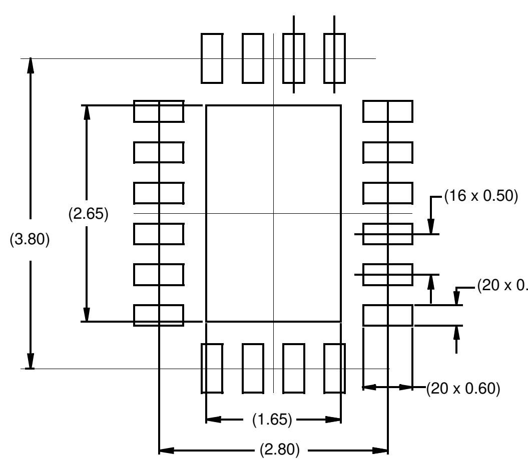
TOP VIEW



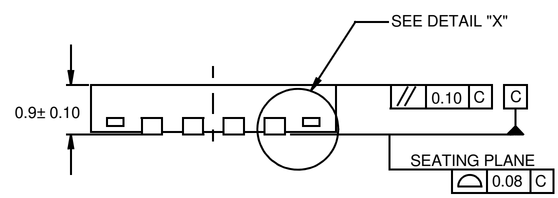
VIEW "A-A"



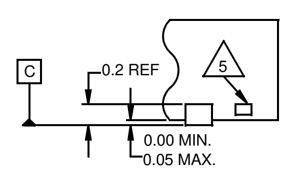
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.