OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
ISL22424

Dual Digitally-Controlled (XDCP™) Potentiometers

FEATURES

- **Dual–Two Separate Potentiometers**
- **256 Resistor Taps/pot–0.4% Resolution**
- **SPI Serial Interface for Write, Read, and Transfer Operations of the Potentiometer Single Supply Device**
- **Wiper Resistance, 100Ω typical @ V_{CC} = 5V**
- **4 Nonvolatile Data Registers for Each Potentiometer**
- **Nonvolatile Storage of Multiple Wiper Positions**
- **Power-on Recall Loads Saved Wiper Position on Power-up.**
- **Standby Current < 5µA Max**
- **50kΩ, 100kΩ Versions of End to End Resistance**
- **100 yr. Data Retention**
- **Endurance: 100,000 Data Changes per Bit per Register**
- **24 Ld SOIC, 24 Ld TSSOP**
- **Low Power CMOS**
- **Power Supply V_{CC} = 5V ±10%**
- **Pb-Free Plus Anneal Available (RoHS Compliant)**

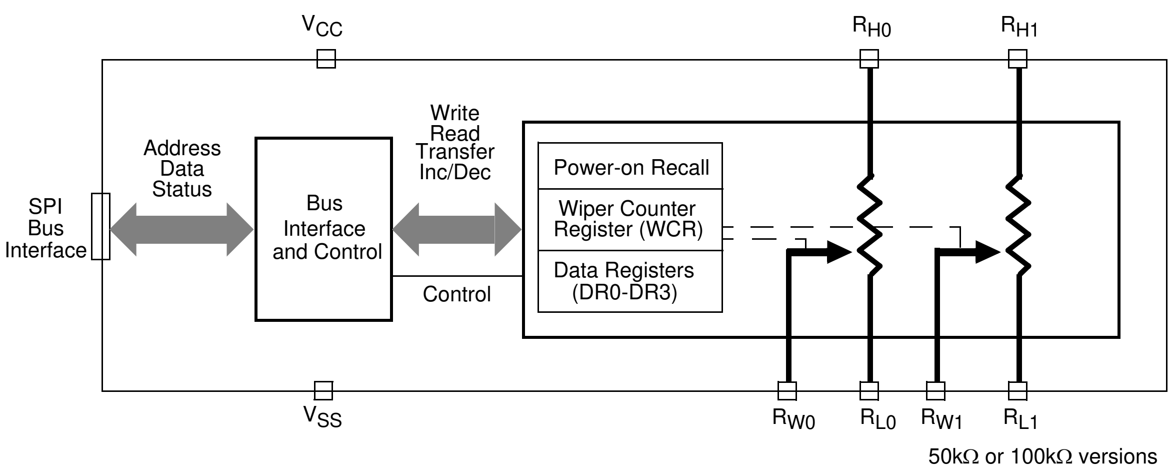
DESCRIPTION

The X9261 integrates 2 digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

The digital controlled potentiometer is implemented using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Powerup recalls the contents of the default Data Register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

FUNCTIONAL DIAGRAM

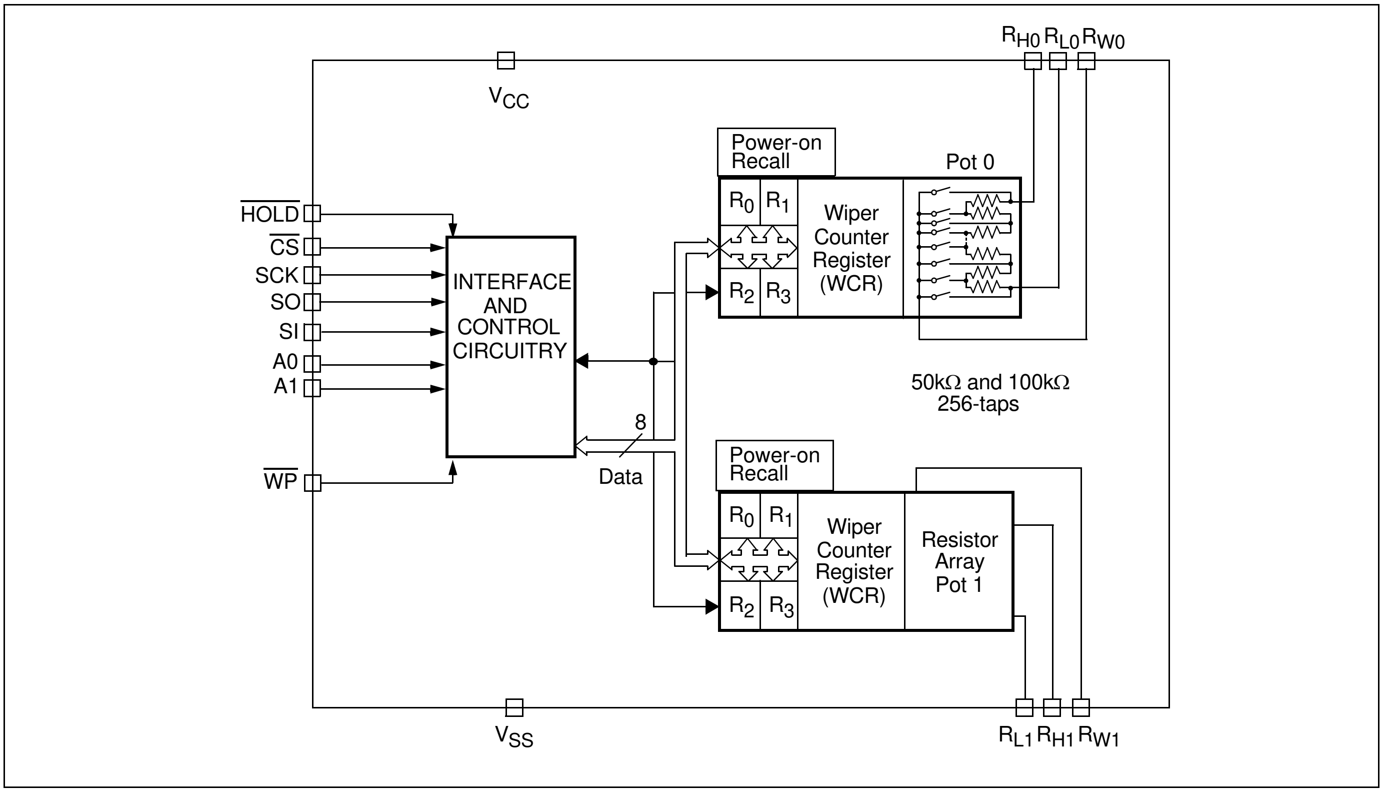


Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
X9261US24	X9261US	5 ±10%	50	0 to 70	24 Ld SOIC (300 mil)	M24.3
X9261US24Z (Note)	X9261US Z			0 to 70	24 Ld SOIC (300 mil) (Pb-free)	M24.3
X9261UV24	X9261UV			0 to 70	24 Ld TSSOP (4.4mm)	MDP0044
X9261UV24Z (Note)	X9261UV Z			0 to 70	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

DETAILED FUNCTIONAL DIAGRAM



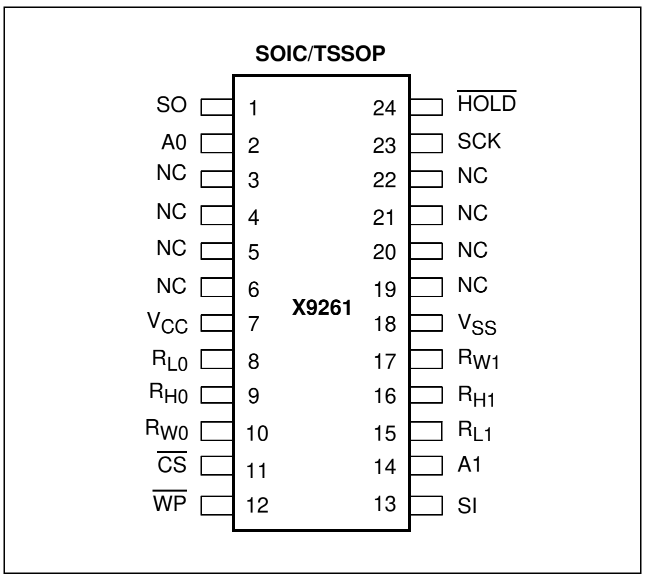
CIRCUIT LEVEL APPLICATIONS

- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

SYSTEM LEVEL APPLICATIONS

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

PIN CONFIGURATION



PIN ASSIGNMENTS

Pin (SOIC/ TSSOP)	Symbol	Function
1	SO	Serial Data Output for SPI bus
2	A0	Device Address for SPI bus.
3	NC	No Connect.
4	NC	No Connect.
5	NC	No Connect.
6	NC	No Connect.
7	V_{CC}	System Supply Voltage
8	R_{L0}	Low Terminal for Potentiometer 0.
9	R_{H0}	High Terminal for Potentiometer 0.
10	R_{W0}	Wiper Terminal for Potentiometer 0.
11	$\overline{CS}$	Device Address for SPI bus.
12	$\overline{WP}$	Hardware Write Protect
13	SI	Serial Data Input for SPI bus
14	A1	Device Address for SPI bus.
15	R_{L1}	Low Terminal for Potentiometer 1.
16	R_{H1}	High Terminal for Potentiometer 1.
17	R_{W1}	Wiper Terminal for Potentiometer 1.
18	V_{SS}	System Ground
19	NC	No Connect
20	NC	No Connect
21	NC	No Connect
22	NC	No Connect
23	SCK	Serial Clock for SPI bus
24	$\overline{HOLD}$	Device select. Pause the SPI serial bus.

PIN DESCRIPTIONS

Bus Interface Pins

SERIAL OUTPUT (SO)

SO is a serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

SERIAL INPUT

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

SERIAL CLOCK (SCK)

The SCK input is used to clock data into and out of the X9261.

HOLD (HOLD)

HOLD is used in conjunction with the CS pin to select the device. Once the part is selected and a serial sequence is underway, HOLD may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, HOLD must be brought LOW while SCK is LOW. To resume communication, HOLD is brought HIGH, again while SCK is LOW. If the pause feature is not used, HOLD should be held HIGH at all times.

DEVICE ADDRESS (A1 - A0)

The address inputs are used to set the 4-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9261.

CHIP SELECT (CS)

When CS is HIGH, the X9261 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. CS LOW enables the X9261, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on CS is required prior to the start of any operation.

Potentiometer Pins

R_H, R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer. Since there are 2 potentiometers, there are 2 sets of R_H and R_L such that R_{H0} and R_{L0} are the terminals of POT 0 and so on.

R_W

The wiper pin are equivalent to the wiper terminal of a mechanical potentiometer. Since there are 2 potentiometers, there are 2 sets of R_W such that R_{W0} is the terminals of POT 0 and so on.

Supply Pins

SYSTEM SUPPLY VOLTAGE (V_{CC}) AND SUPPLY GROUND (V_{SS})

The V_{CC} pin is the system supply voltage. The V_{SS} pin is the system ground.

Other Pins

NO CONNECT

No connect pins should be left floating. This pins are used for Intersil manufacturing and testing purposes.

HARDWARE WRITE PROTECT INPUT (WP)

The WP pin when LOW prevents nonvolatile writes to the Data Registers.

PRINCIPLES OF OPERATION

Serial Interface

The X9261 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK. CS must be LOW and the HOLD and WP pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

Array Description

The X9261 is comprised of a resistor array (See Figure 1). The array contains the equivalent of 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L inputs).

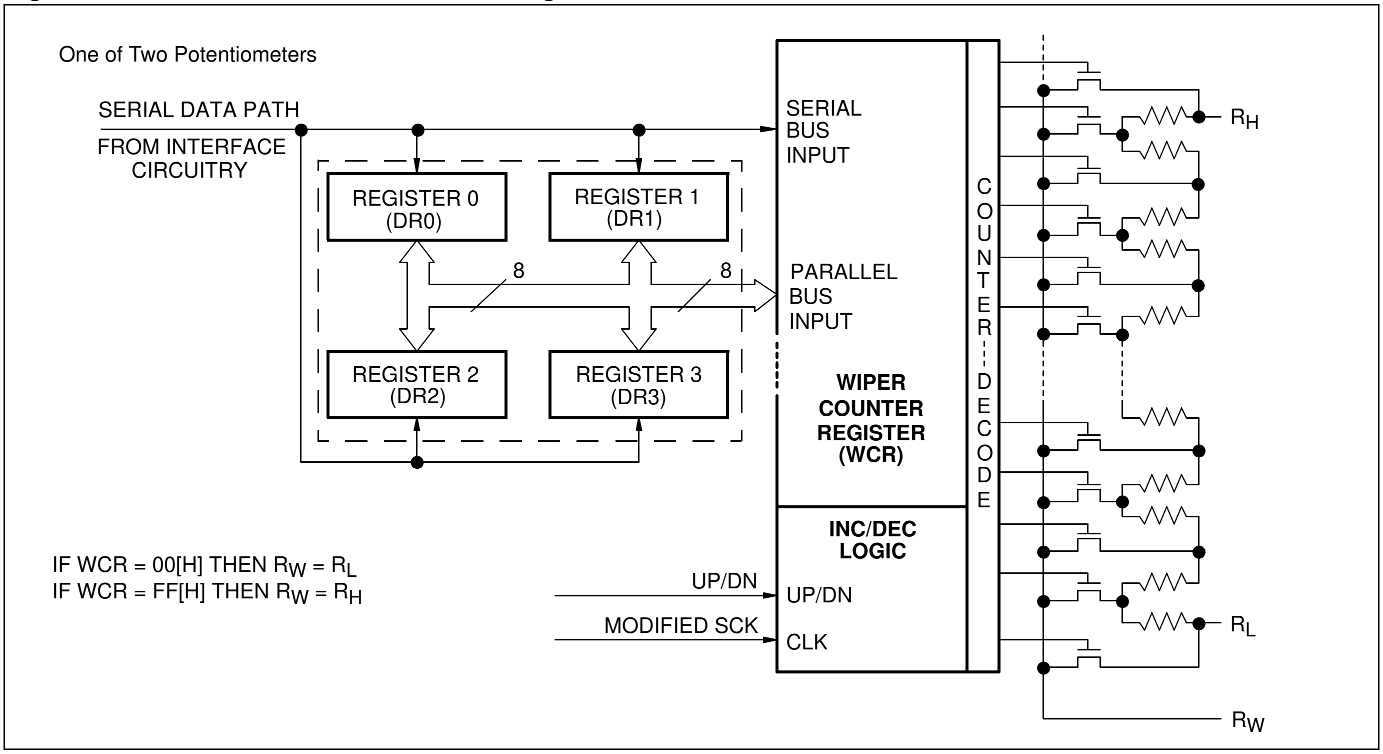
At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R_W) output. Within each individual array only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The 8-bits of the WCR (WCR[7:0]) are decoded to select, and enable, one of 256 switches (See Table 1).

Power-up and Down Requirements.

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., V_{CC}, V_H, V_L, V_W. The V_{CC} ramp rate specification is always in effect.

Figure 1. Detailed Potentiometer Block Diagram



DEVICE DESCRIPTION

Wiper Counter Register (WCR)

The X9261 contains two Wiper Counter Registers, one for each DCP potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (See Instruction section for more details). Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9261 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR.

Data Registers (DR)

Each potentiometer has four 8-bit nonvolatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bits [7:0] are used to store one of the 256 wiper positions or data (0~255).

Status Register (SR)

This 1-bit Status Register is used to store the system status.

WIP: Write In Progress status bit, read only.

– When WIP=1, indicates that high-voltage write cycle is in progress.
– When WIP=0, indicates that no high-voltage write cycle is in progress.

Table 1. Wiper Counter Register, WCR (8-bit), WCR[7:0]: Used to store the current wiper position (Volatile, V).

WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V
(MSB)							(LSB)

Table 2. Data Register, DR (8-bit), Bit [7:0]: Used to store wiper positions or data (Nonvolatile, NV).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NV	NV	NV	NV	NV	NV	NV	NV
MSB							LSB

DEVICE DESCRIPTION

Instructions

IDENTIFICATION BYTE (ID AND A)

The first byte sent to the X9261 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification Byte. The most significant four bits of the slave address are a device type identifier. The ID[3:0] bits is the device id for the X9261; this is fixed as 0101[B] (refer to Table 3).

The AD[3:0] bits in the ID byte is the internal slave address. The physical device address is defined by the state of the A3 - A0 input pins. The slave address is externally specified by the user. The X9261 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9261 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A3-A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

INSTRUCTION BYTE (I[3:0])

The next byte sent to the X9261 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode (I[3:0]). The RB and RA bits point to one of the four Data Registers of each associated XDCP. The least significant bit points to one of two Wiper Counter Registers or Pots.The format is shown below in Table 4.

Table 3. Identification Byte Format

Device Type Identifier				Slave Address			
ID3	ID2	ID1	ID0	A3	A2	A1	A0
0	1	0	1				
(MSB)							(LSB)

Table 4. Instruction Byte Format

Instruction Opcode				Data Register Selection			Pot Selection (WCR Selection)
I3	I2	I1	I0	RB	RA	0	P0
(MSB)							(LSB)

Register Selection

Register Selected	RB	RA
DR0	0	0
DR1	0	1
DR2	1	0
DR3	1	1

DEVICE DESCRIPTION

Instructions

Four of the ten instructions are three bytes in length. These instructions are:

– **Read Wiper Counter Register** – read the current wiper position of the selected potentiometer,

– **Write Wiper Counter Register** – change current wiper position of the selected potentiometer,

– **Read Data Register** – read the contents of the selected Data Register;

– **Write Data Register** – write a new value to the selected Data Register.

– **Read Status** - This command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The basic sequence of the three byte instructions is illustrated in Figure 3. These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the two potentiometers and one of its associated registers; or it may occur globally, where the transfer occurs between all potentiometers and one associated register. The Read Status Register instruction is the only unique format (See Figure 5).

Four instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9261; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

– **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.

– **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.

– **Global XFR Data Register to Wiper Counter Register** – This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.

– **Global XFR Wiper Counter Register to Data Register** – This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

INCREMENT/DECREMENT COMMAND

The final command is Increment/Decrement (See Figures 6 and 7). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9261 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCL clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the R_L terminal. A detailed illustration of the sequence and timing for this operation are shown. See Instruction format for more details.

Figure 2. Two-Byte Instruction Sequence

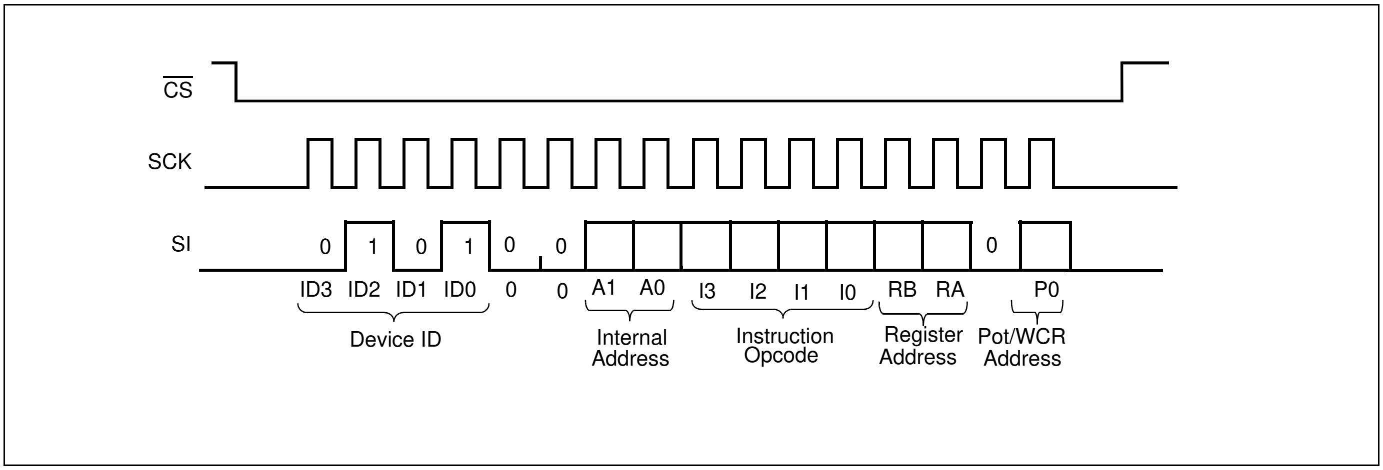


Figure 3. Three-Byte Instruction Sequence (Write)

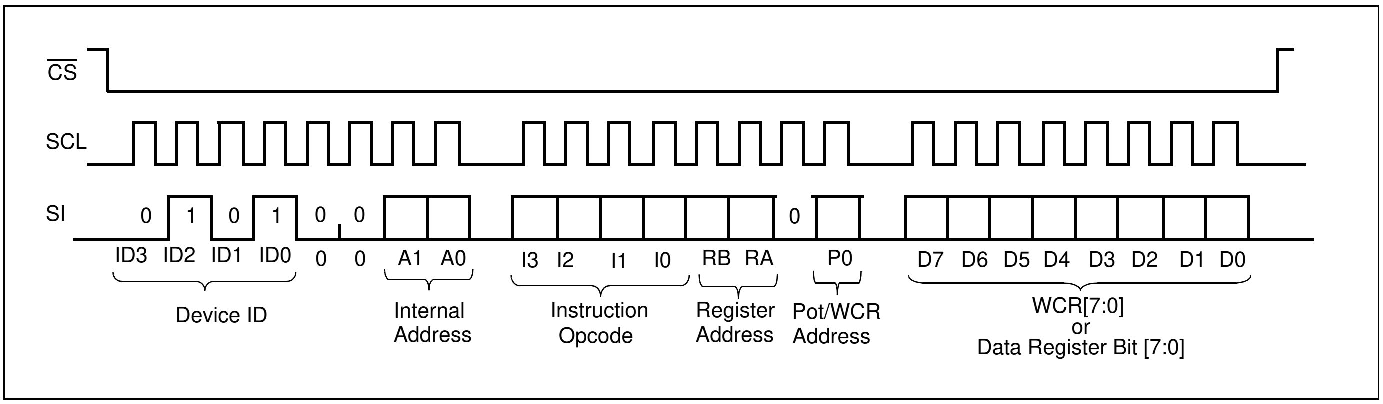


Figure 4. Three-Byte Instruction Sequence (Read)

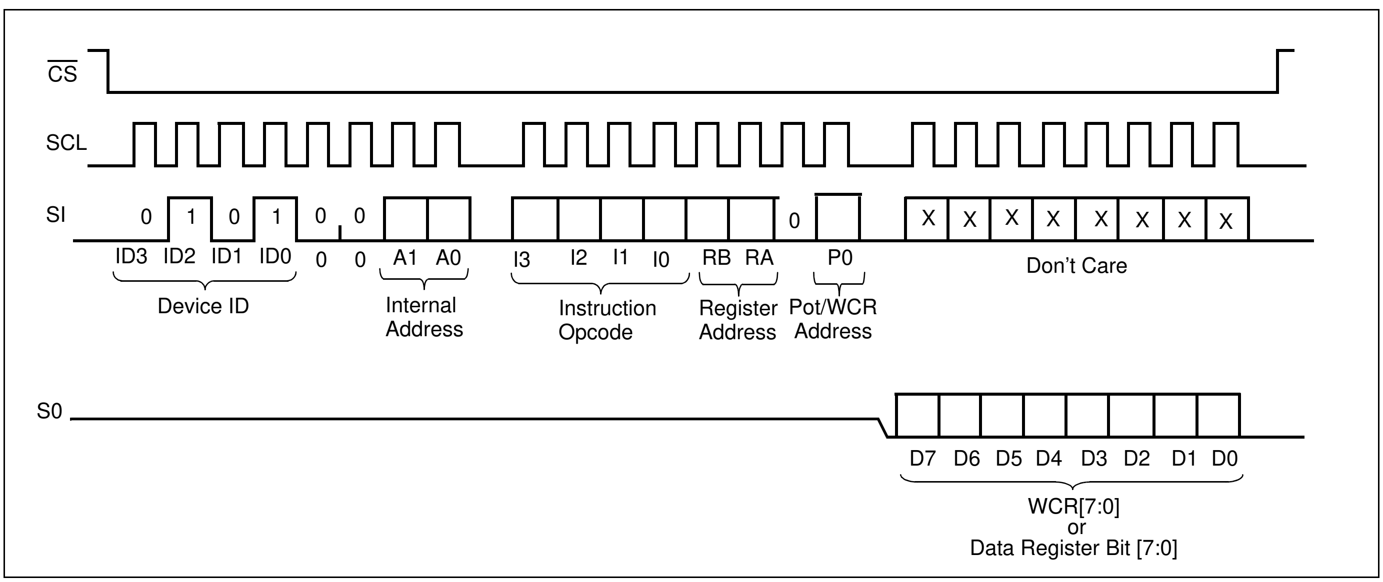


Figure 5. Three-Byte Instruction Sequence (Read Status Register)

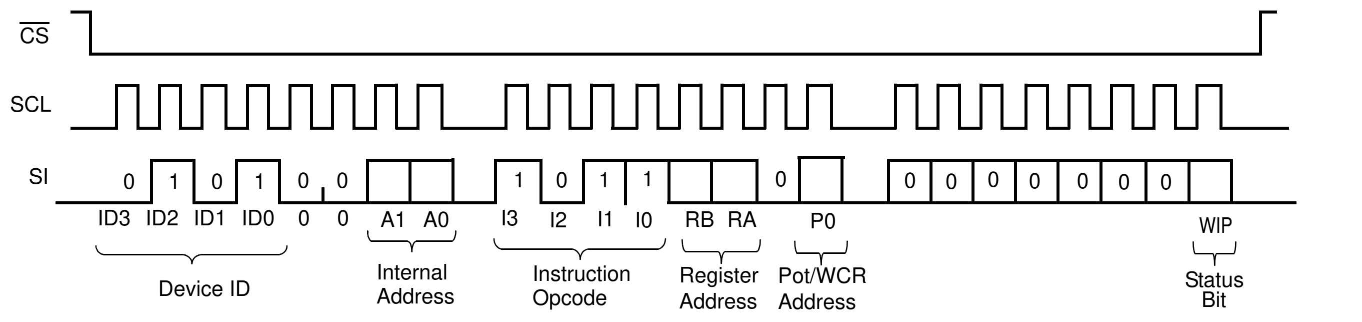


Figure 6. Increment/Decrement Instruction Sequence

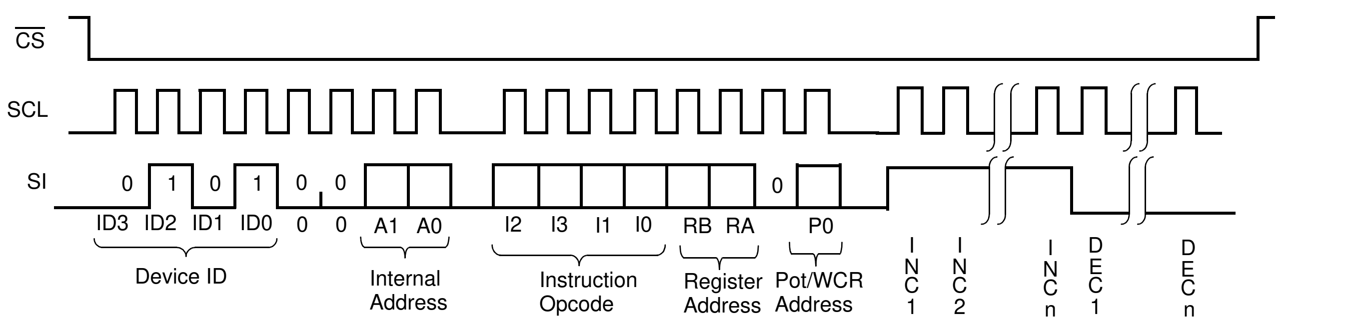


Figure 7. Increment/Decrement Timing Limits

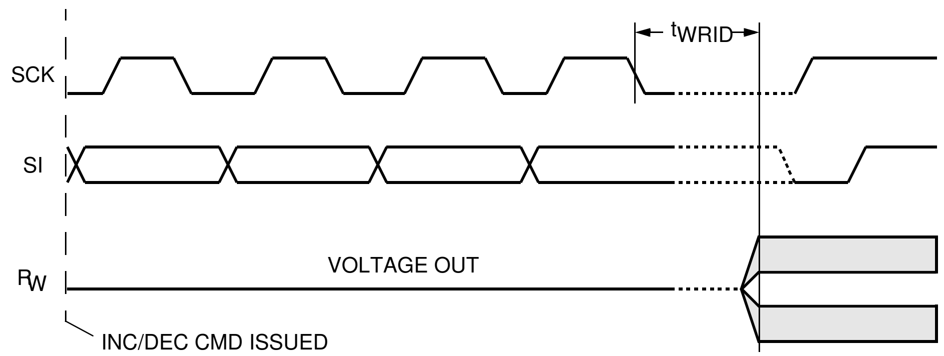


Table 5. Instruction Set

Instruction	Instruction Set								Operation
	I3	I2	I1	I0	RB	RA	0	P0	
Read Wiper Counter Register	1	0	0	1	0	0	0	1/0	Read the contents of the Wiper Counter Register pointed to by P0
Write Wiper Counter Register	1	0	1	0	0	0	0	1/0	Write new value to the Wiper Counter Register pointed to by P0
Read Data Register	1	0	1	1	1/0	1/0	0	1/0	Read the contents of the Data Register pointed to by P0 and RB - RA
Write Data Register	1	1	0	0	1/0	1/0	0	1/0	Write new value to the Data Register pointed to by P0 and RB - RA
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	0	1/0	Transfer the contents of the Data Register pointed to by P0 and RB - RA to its associated Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	0	1/0	Transfer the contents of the Wiper Counter Register pointed to by P0 to the Data Register pointed to by RB - RA
Global XFR Data Registers to Wiper Counter Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by RB - RA of all four pots to their respective Wiper Counter Registers
Global XFR Wiper Counter Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Counter Registers to their respective data Registers pointed to by RB - RA of all four pots
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	0	1/0	Enable Increment/decrement of the Control Latch pointed to by P0

Note: 1/0 = data is one or zero

INSTRUCTION FORMAT

Read Wiper Counter Register (WCR)

	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Wiper Position (Sent by X9261 on SO)								
$\overline{CS}$ Falling Edge	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	0	P0	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	$\overline{CS}$ Rising Edge

Write Wiper Counter Register (WCR)

	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Data Byte (Sent by Host on SI)								
$\overline{CS}$ Falling Edge	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	0	P0	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	$\overline{CS}$ Rising Edge

Read Data Register (DR)

	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				Data Byte (Sent by X9271 on SO)								
$\overline{CS}$ Falling Edge	0	1	0	1	0	0	A1	A0	1	0	1	1	RB	RA	0	P0	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{CS}$ Rising Edge

Write Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				Data Byte (Sent by Host on SI)								$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	0	0	RB	RA	0	P0	D7	D6	D5	D4	D3	D2	D1	D0		

Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR Addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	0	1	RB	RA	0	0	

Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR Addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	0	0	0	RB	RA	0	0		

Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	1	0	RB	RA	0	P0		

Transfer Data Register (DR) to Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	1	0	1	RB	RA	0	P0	

Increment/Decrement Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Increment/Decrement (Sent by Master on SDA)				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	1	0	X	X	0	P0	I/D	I/D	. . . .	I/D	I/D	

Read Status Register (SR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Data Byte (Sent by X9261 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	WIP	

Notes: (1) "A1 ~ A0": stands for the device addresses sent by the master.
(2) WPx refers to wiper position data in the Counter Register
(2) "I": stands for the increment operation, SI held HIGH during active SCK phase (high).
(3) "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

ABSOLUTE MAXIMUM RATINGS

Temperature under bias .... -65°C to +135°C
Storage temperature.......................... -65°C to +150°C
Voltage on SCK any address input
with respect to V_{SS} .... -1V to +7V
$\Delta V = |(V_H - VL)|$...5.5V
Lead temperature (soldering, 10s) .... 300°C
I_W (10s) ....±6mA

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

Device	Supply Voltage (V_{CC})$^{(4)}$ Limits
X9261	5V ± 10%

POTENTIOMETER CHARACTERISTICS (Over recommended industrial operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
R_{TOTAL}	End to End Resistance		100		kΩ	T version
R_{TOTAL}	End to End Resistance		50		kΩ	U version
	End to End Resistance Tolerance			±20	%	
	Power Rating			50	mW	25°C, each pot
I_W	Wiper Current			±3	mA	
R_W	Wiper Resistance			300	Ω	I_W = ±3mA @ V+ = 3V
R_W	Wiper Resistance			150	Ω	I_W = ±3mA @ V+ = 5V
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS}		V_{CC}	V	V_{SS} = 0V
	Noise		-120		dBV	Ref: 1V
	Resolution		0.4		%	
	Absolute Linearity (1)			±1	MI(3)	$R_{w(n)(actual)} - R_{w(n)(expected)}$ (5)
	Relative Linearity (2)			±0.6	MI(3)	$R_{w(n+1)} - [R_{w(n)} + MI]$ (5)
	Temperature Coefficient of R_{TOTAL}		±300		ppm/°C	
	Ratiometric Temp. Coefficient			20	ppm/°C	
$C_H/C_L/C_W$	Potentiometer Capacitances		10/10/25		pF	See Macro model
I_{al}	R_W, R_H, R_L Leakage		0.1	10.0	µA	Device in stand by. Vin = V_{SS} to V_{CC}

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT / 255 or (R_H - R_L) / 255, single pot
(4) During power-up $V_{CC} > V_H$, V_L, and V_W.
(5) n = 0, 1, 2, …,255; m = 0, 1, 2, …, 254.

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
I_{CC1}	V_{CC} supply current (active)			400	µA	f_{SCK} = 2.5 MHz, SO = Open, V_{CC} = 6V Other Inputs = V_{SS}
I_{CC2}	V_{CC} supply current (nonvolatile write)		1	5	mA	f_{SCK} = 2.5MHz, SO = Open, V_{CC} = 6V Other Inputs = V_{SS}
I_{SB}	V_{CC} current (standby)			5	µA	SCK = SI = V_{SS}, Addr. = V_{SS}, $\overline{CS}$ = V_{CC} = 6V
I_{LI}	Input leakage current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH voltage	V_{CC} x 0.7		V_{CC} + 1	V	
V_{IL}	Input LOW voltage	-1		V_{CC} x 0.3	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 3mA
V_{OH}	Output HIGH voltage	V_{CC} - 0.8			V	I_{OH} = -1mA, $V_{CC} \geq$ +3V
V_{OH}	Output HIGH voltage	V_{CC} - 0.4			V	I_{OH} = -0.4mA, $V_{CC} \leq$ +3V

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	years

CAPACITANCE

Symbol	Test	Max.	Units	Test Conditions
C_{OUT}(6)	Output capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(6)	Input capacitance (A0, A1, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$, and SCK)	6	pF	V_{IN} = 0V

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_r V_{CC}(6)	V_{CC} Power-up rate	0.2	50	V/ms
t_{PUR}(7)	Power-up to initiation of read operation		1	ms

POWER-UP AND DOWN REQUIREMENTS

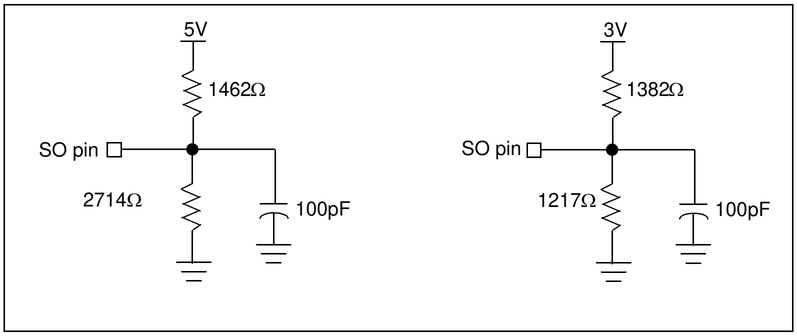
The are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., $V_{CC} \geq V_H$, V_L, V_W. The V_{CC} power-up timing spec is always in effect.

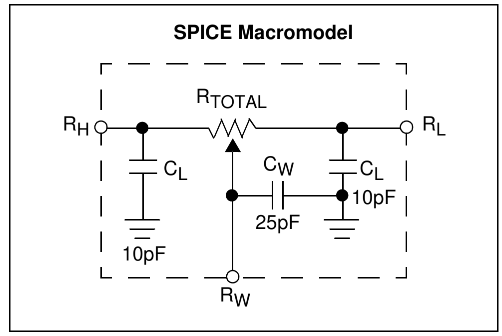
A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

Notes: (6) This parameter is not 100% tested
(7) t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT





AC TIMING

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	SSI/SPI clock frequency		2	MHz
t_{CYC}	SSI/SPI clock cycle rime	500		ns
t_{WH}	SSI/SPI clock high rime	200		ns
t_{WL}	SSI/SPI clock low time	200		ns
t_{LEAD}	Lead time	250		ns
t_{LAG}	Lag time	250		ns
t_{SU}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input setup time	50		ns
t_H	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input hold time	50		ns
t_{RI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input rise time		2	µs
t_{FI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input fall time		2	µs
t_{DIS}	SO output disable time	0	250	ns
t_V	SO output valid time		200	ns
t_{HO}	SO output hold time	0		ns
t_{RO}	SO output rise time		100	ns
t_{FO}	SO output fall time		100	ns
t_{HOLD}	$\overline{HOLD}$ time	400		ns
t_{HSU}	$\overline{HOLD}$ setup time	100		ns
t_{HH}	$\overline{HOLD}$ hold time	100		ns
t_{HZ}	$\overline{HOLD}$ low to output in high Z		100	ns
t_{LZ}	$\overline{HOLD}$ high to output in low Z		100	ns
T_I	Noise suppression time constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs		10	ns
t_{CS}	$\overline{CS}$ deselect time	2		µs
t_{WPASU}	$\overline{WP}$, A0, A1 setup time	0		ns
t_{WPAH}	$\overline{WP}$, A0, A1 hold time	0		ns

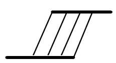
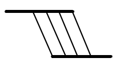
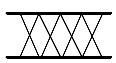
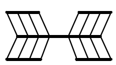
HIGH-VOLTAGE WRITE CYCLE TIMING

Symbol	Parameter	Typ.	Max.	Units
t_{WR}	High-voltage write cycle time (store instructions)	5	10	ms

XDCP TIMING

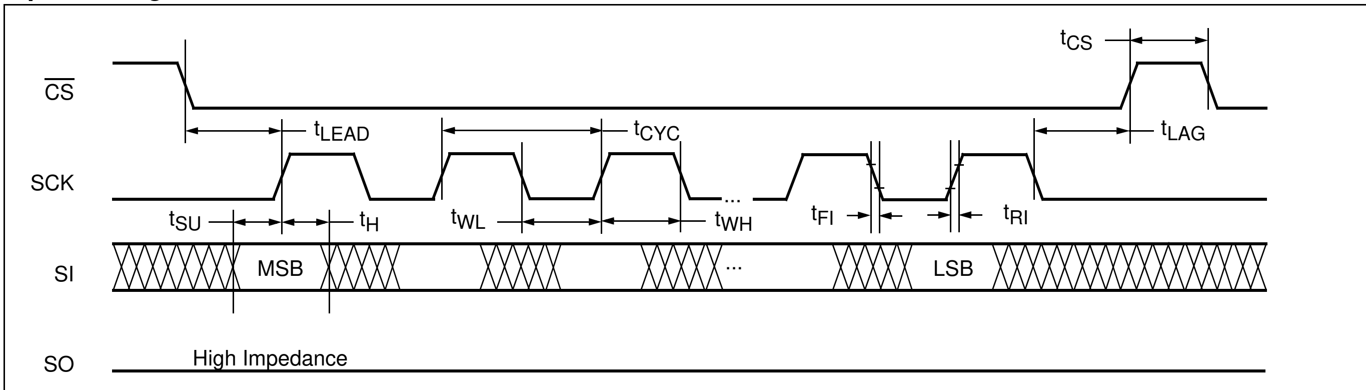
Symbol	Parameter	Min.	Max.	Units
t_{WRPO}	Wiper response time after the third (last) power supply is stable	5	10	µs
t_{WRL}	Wiper response time after instruction issued (all load instructions)	5	10	µs

SYMBOL TABLE

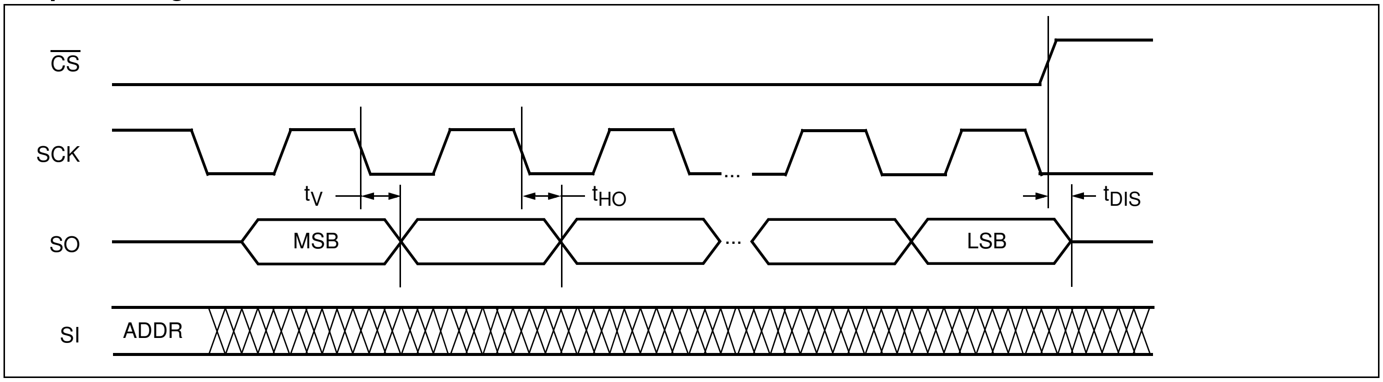
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

TIMING DIAGRAMS

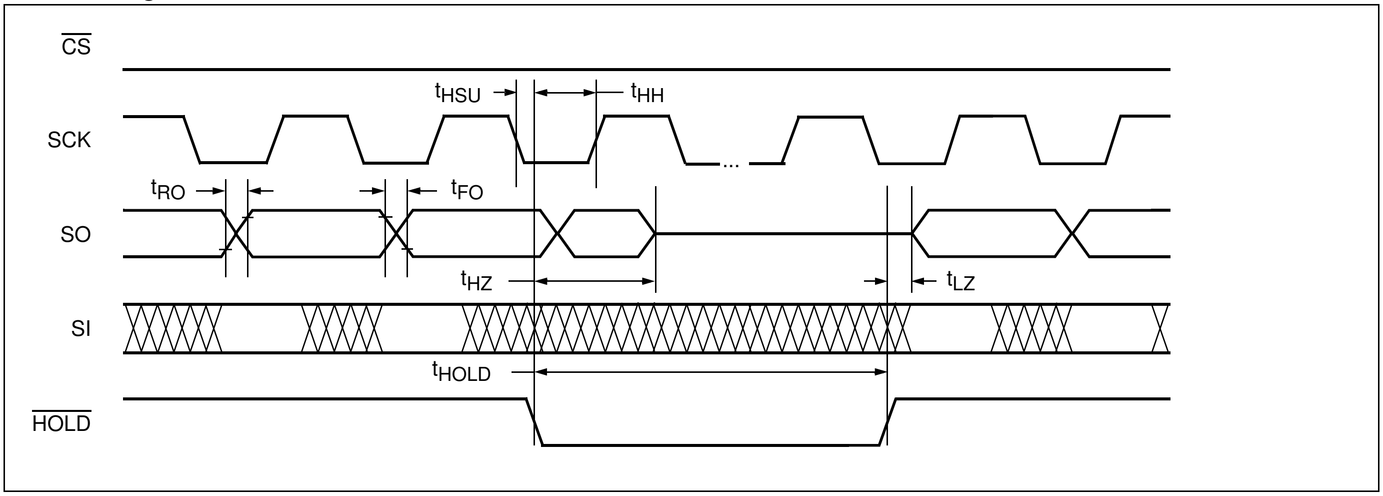
Input Timing



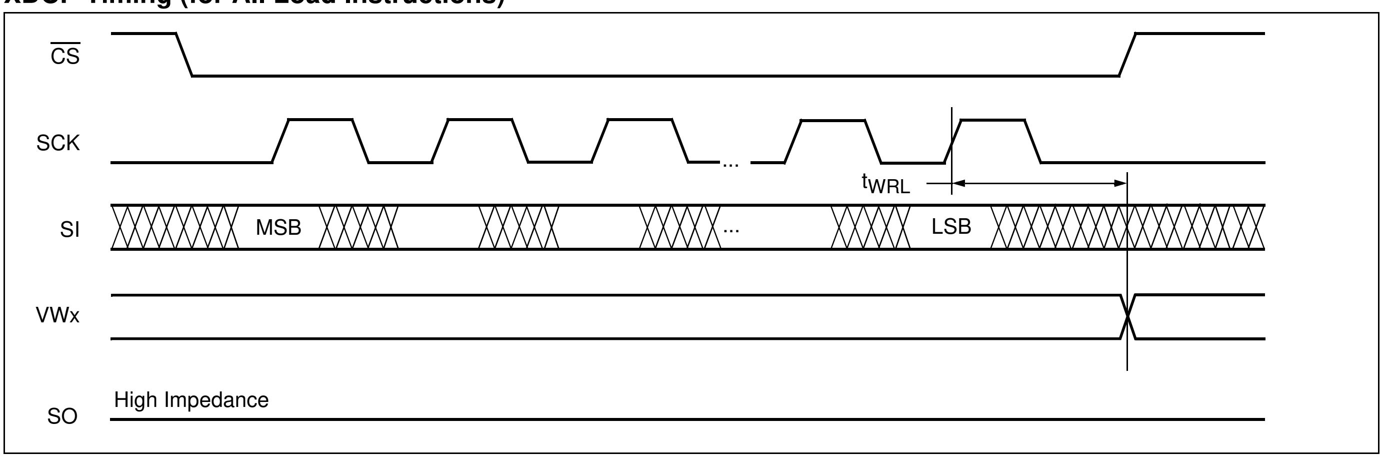
Output Timing



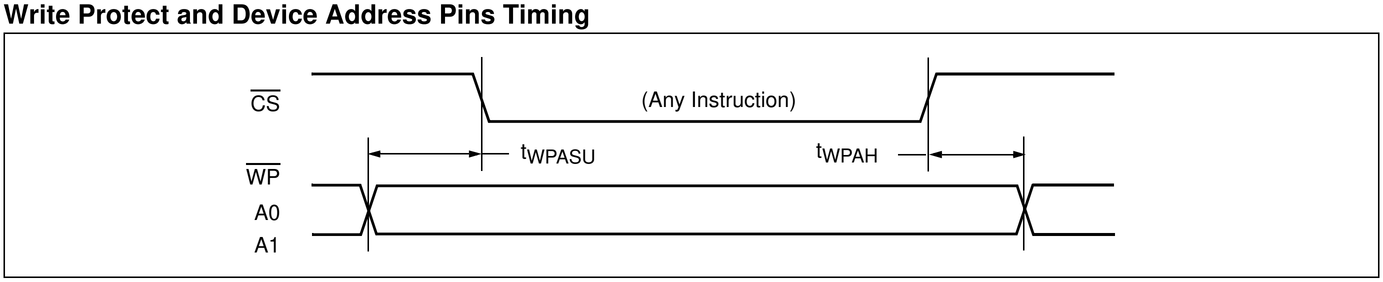
Hold Timing



XDCP Timing (for All Load Instructions)

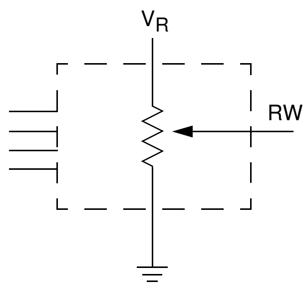


Write Protect and Device Address Pins Timing

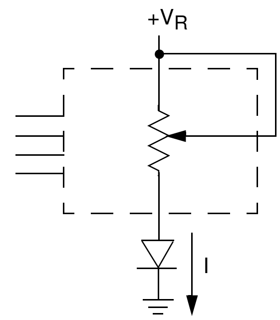


APPLICATIONS INFORMATION

Basic Configurations of Electronic Potentiometers



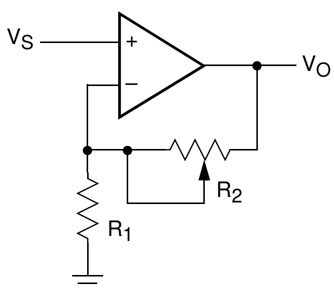
Three terminal Potentiometer;
Variable voltage divider



Two terminal Variable Resistor;
Variable current

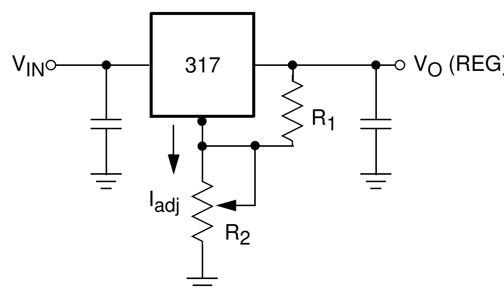
Application Circuits

Noninverting Amplifier



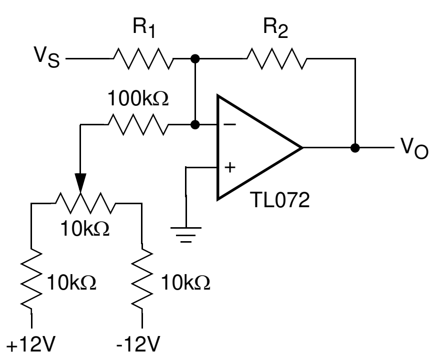
$V_O = (1+R_2/R_1)V_S$

Voltage Regulator

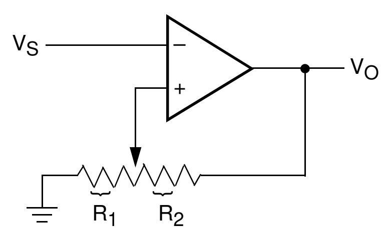


$V_O\ (REG) = 1.25V\ (1+R_2/R_1)+I_{adj}\ R_2$

Offset Voltage Adjustment



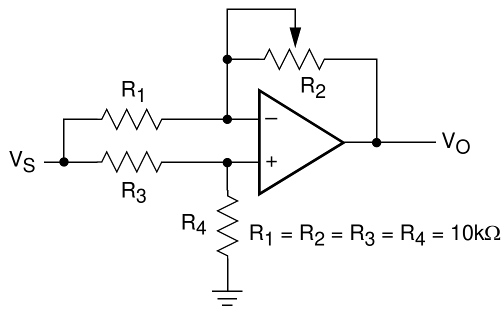
Comparator with Hysterisis



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

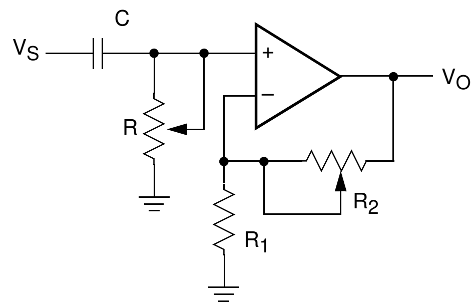
Application Circuits (continued)

Attenuator



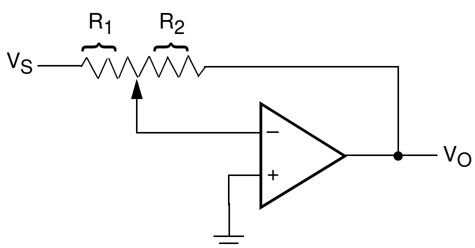
$V_O = G\ V_S$
$-1/2 \le G \le +1/2$

Filter



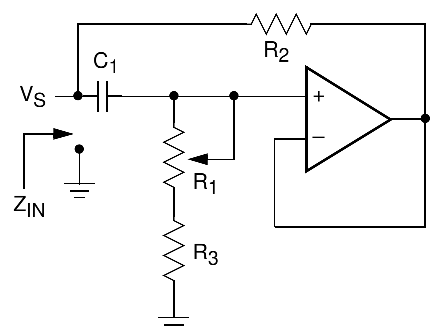
$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

Inverting Amplifier



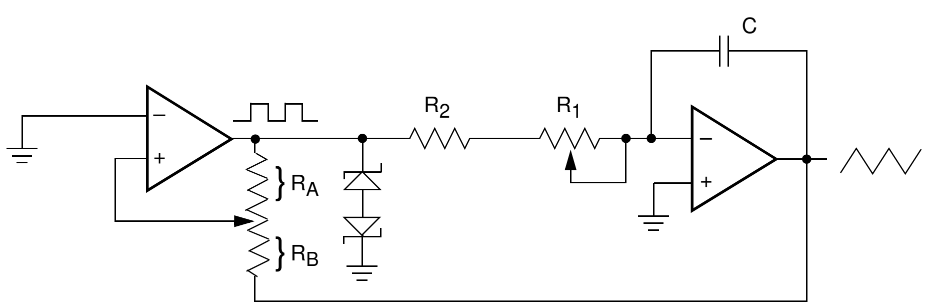
$V_O = G\ V_S$
$G = -\ R_2/R_1$

Equivalent L-R Circuit



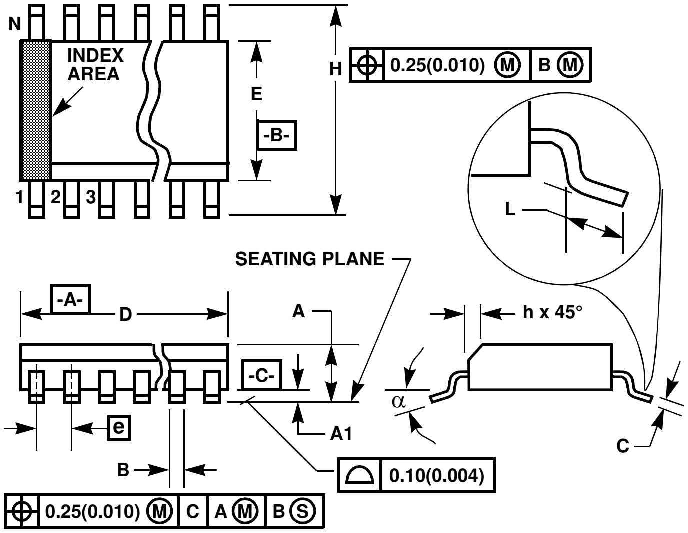
$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

Function Generator



frequency $\propto R_1, R_2, C$
amplitude $\propto R_A, R_B$

Small Outline Plastic Packages (SOIC)



NOTES:

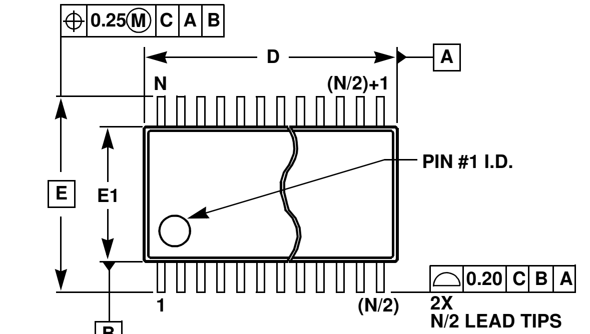
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

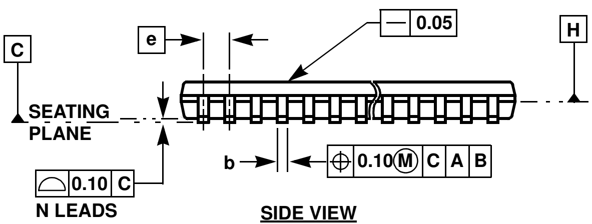
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 1 4/06

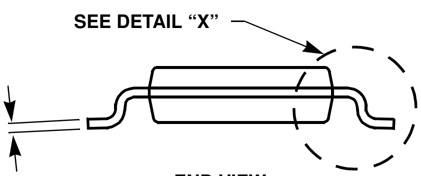
Thin Shrink Small Outline Package Family (TSSOP)



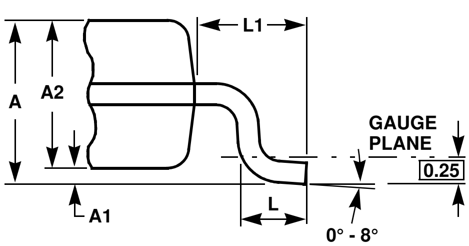
TOP VIEW



SIDE VIEW



END VIEW



DETAIL X

MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	14 LD	16 LD	20 LD	24 LD	28 LD	TOLERANCE
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. E 12/02

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.