

**Digitally Controlled Potentiometer (XDCP™)**

The Intersil X9315 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the CS, U/D, and INC inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

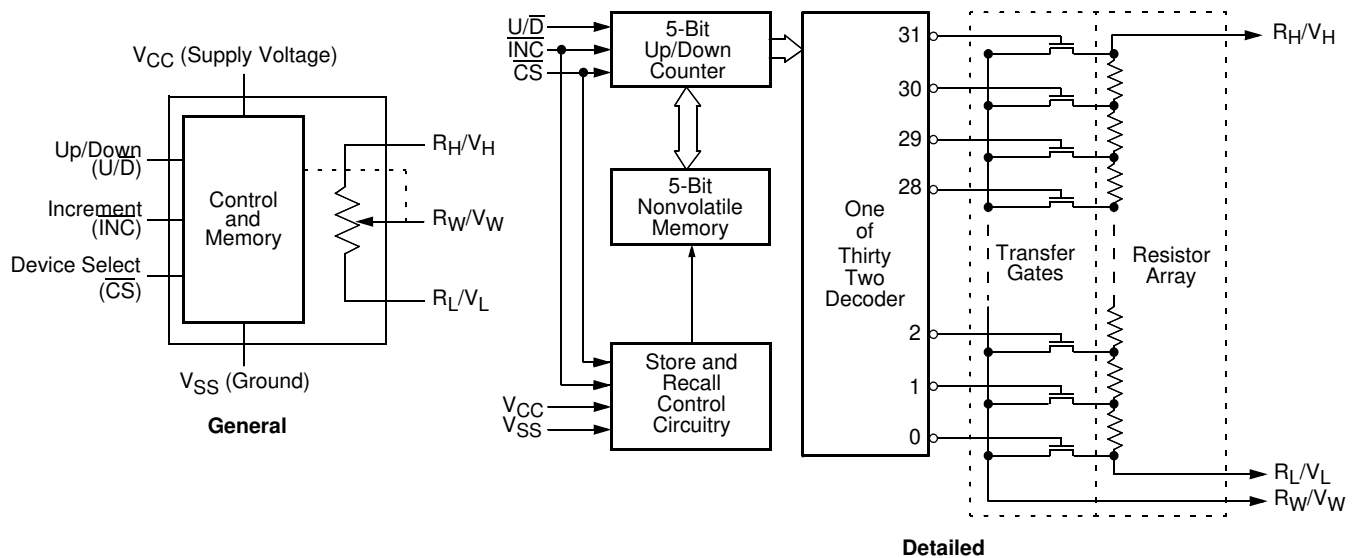
The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Control
- Parameter Adjustments
- Signal Processing

**Features**

- Solid-state potentiometer
- 3-wire serial interface
- 32 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements
  - Temperature compensated
  - End to end resistance range  $\pm 20\%$
  - Terminal voltage, 0 to  $V_{CC}$
- Low power CMOS
  - $V_{CC} = 2.7V$  or  $5V$
  - Active current,  $50/400\mu A$  max.
  - Standby current,  $1\mu A$  max.
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- $R_{TOTAL}$  values =  $10k\Omega$ ,  $50k\Omega$ ,  $100k\Omega$
- Packages
  - 8 Ld SOIC, MSOP and PDIP
- Pb-free plus anneal available (RoHS compliant)

**Block Diagram**



# X9315

## Ordering Information

PART NUMBER	PART MARKING	V <sub>CC</sub> LIMITS (V)	R <sub>TOTAL</sub> (kΩ)	TEMP RANGE (°C)	PACKAGE
X9315WM*	AAW	5 ±10%	10	0 to 70	8 Ld MSOP
X9315WMZ* (Note)	DDT			0 to 70	8 Ld MSOP (Pb-free)
X9315WMI*	AAX			-40 to 85	8 Ld MSOP
X9315WMIZ* (Note)	AKW			-40 to 85	8 Ld MSOP (Pb-free)
X9315WP	X9315WP			0 to 70	8 Ld PDIP
X9315WPI	X9315WP I			-40 to 85	8 Ld PDIP
X9315WS*	X9315W			0 to 70	8 Ld SOIC
X9315WSZ* (Note)	X9315W Z			0 to 70	8 Ld SOIC (Pb-free)
X9315WSI*	X9315W I			-40 to 85	8 Ld SOIC
X9315WSIZ* (Note)	X9315W Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9315UM*			50	0 to 70	8 Ld MSOP
X9315UMZ* (Note)	DDS			0 to 70	8 Ld MSOP (Pb-free)
X9315UMI*	AEB			-40 to 85	8 Ld MSOP
X9315UMIZ* (Note)	DDR			-40 to 85	8 Ld MSOP (Pb-free)
X9315UP	X9315UP			0 to 70	8 Ld PDIP
X9315UPI	X9315UP I			-40 to 85	8 Ld PDIP
X9315US*	X9315U			0 to 70	8 Ld SOIC
X9315USZ* (Note)	X9315U Z			0 to 70	8 Ld SOIC (Pb-free)
X9315USI*	X9315U I			-40 to 85	8 Ld SOIC
X9315USIZ* (Note)	X9315U Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9315TM*	AEJ	100	0 to 70	8 Ld MSOP	
X9315TMZ* (Note)	DDN		0 to 70	8 Ld MSOP (Pb-free)	
X9315TMI*	ADZ		-40 to 85	8 Ld MSOP	
X9315TMIZ* (Note)	DDL		-40 to 85	8 Ld MSOP (Pb-free)	
X9315TP	X9315TP		0 to 70	8 Ld PDIP	
X9315TPI	X9315TP I		-40 to 85	8 Ld PDIP	
X9315TS*	X9315T		0 to 70	8 Ld SOIC	
X9315TSZ* (Note)	X9315T Z		0 to 70	8 Ld SOIC (Pb-free)	
X9315TSI*	X9315T I		-40 to 85	8 Ld SOIC	
X9315TSIZ* (Note)	X9315T Z I		-40 to 85	8 Ld SOIC (Pb-free)	

# X9315

## Ordering Information (Continued)

PART NUMBER	PART MARKING	V <sub>CC</sub> LIMITS (V)	R <sub>TOTAL</sub> (kΩ)	TEMP RANGE (°C)	PACKAGE	
X9315TP-2.7	X9315TP F	2.7-5.5	10	0 to 70	8 Ld PDIP	
X9315TPI-2.7	X9315TP G			-40 to 85	8 Ld PDIP	
X9315WM-2.7*	AAU			0 to 70	8 Ld MSOP	
X9315WMZ-2.7* (Note)	AOI			0 to 70	8 Ld MSOP (Pb-free)	
X9315WMI-2.7*	AAV			-40 to 85	8 Ld MSOP	
X9315WMIZ-2.7* (Note)				-40 to 85	8 Ld MSOP (Pb-free)	
X9315WP-2.7	X9315WP F			0 to 70	8 Ld PDIP	
X9315WPI-2.7	X9315WP G			-40 to 85	8 Ld PDIP	
X9315WS-2.7*	X9315W F			0 to 70	8 Ld SOIC	
X9315WSZ-2.7* (Note)	X9315W Z F			0 to 70	8 Ld SOIC (Pb-free)	
X9315WSI-2.7*	X9315W G			-40 to 85	8 Ld SOIC	
X9315WSIZ-2.7* (Note)	X9315W Z G			-40 to 85	8 Ld SOIC (Pb-free)	
X9315UM-2.7*	AEK		50	0 to 70	8 Ld MSOP	
X9315UMZ-2.7* (Note)	AKU			0 to 70	8 Ld MSOP (Pb-free)	
X9315UMI-2.7*	AEA			-40 to 85	8 Ld MSOP	
X9315UMIZ-2.7* (Note)	AJG			-40 to 85	8 Ld MSOP (Pb-free)	
X9315UP-2.7				0 to 70	8 Ld PDIP	
X9315UPI-2.7				-40 to 85	8 Ld PDIP	
X9315US-2.7*	X9315U F			0 to 70	8 Ld SOIC	
X9315USZ-2.7* (Note)	X9315U Z F			0 to 70	8 Ld SOIC (Pb-free)	
X9315USI-2.7*	X9315U G			-40 to 85	8 Ld SOIC	
X9315USIZ-2.7* (Note)	X9315U Z G			-40 to 85	8 Ld SOIC (Pb-free)	
X9315TM-2.7*	AEI			100	0 to 70	8 Ld MSOP
X9315TMZ-2.7* (Note)	DDP				0 to 70	8 Ld MSOP (Pb-free)
X9315TMI-2.7*	ADY	-40 to 85	8 Ld MSOP			
X9315TMIZ-2.7* (Note)	DDM	-40 to 85	8 Ld MSOP (Pb-free)			
X9315TS-2.7*	X9315T F	0 to 70	8 Ld SOIC			
X9315TSZ-2.7* (Note)	X9315T Z F	0 to 70	8 Ld SOIC (Pb-free)			
X9315TSI-2.7*	X9315T G	-40 to 85	8 Ld SOIC			
X9315TSIZ-2.7* (Note)	X9315T Z G	-40 to 85	8 Ld SOIC (Pb-free)			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

\*Add "T1" suffix for tape and reel.

**Pin Descriptions**

**$R_H/V_H$  and  $R_L/V_L$**

The high ( $R_H/V_H$ ) and low ( $R_L/V_L$ ) terminals of the X9315 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is  $V_{SS}$  and the maximum is  $V_{CC}$ . The terminology of  $R_L/V_L$  and  $R_H/V_H$  references the relative position of the terminal in relation to wiper movement direction selected by the  $U/\bar{D}$  input, and not the voltage potential on the terminal.

**$R_W/V_W$**

$R_W/V_W$  is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically  $200\Omega$  at  $V_{CC} = 5V$ .

**Up/Down ( $U/\bar{D}$ )**

The  $U/\bar{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

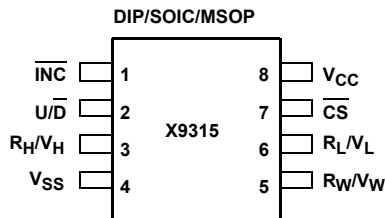
**Increment ( $\bar{INC}$ )**

The  $\bar{INC}$  input is negative-edge triggered. Toggling  $\bar{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\bar{D}$  input.

**Chip Select ( $\bar{CS}$ )**

The device is selected when the  $\bar{CS}$  input is LOW. The current counter value is stored in nonvolatile memory when  $\bar{CS}$  is returned HIGH while the  $\bar{INC}$  input is also HIGH. After the store operation is complete the X9315 will be placed in the low power standby mode until the device is selected once again.

**Pin Configuration**



**Pin Names**

SYMBOL	DESCRIPTION
$R_H/V_H$	High terminal
$R_W/V_W$	Wiper terminal
$R_L/V_L$	Low terminal
$V_{SS}$	Ground
$V_{CC}$	Supply voltage
$U/\bar{D}$	Up/Down control input

**Pin Names**

SYMBOL	DESCRIPTION
INC	Increment control input
CS	Chip Select control input

**Principles of Operation**

There are three sections of the X9315: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for  $t_{1W}$  ( $INC$  to  $V_W$  change). The  $R_{TOTAL}$  value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

**Instructions and Programming**

The  $\bar{INC}$ ,  $U/\bar{D}$  and  $\bar{CS}$  inputs control the movement of the wiper along the resistor array. With  $\bar{CS}$  set LOW the device is selected and enabled to respond to the  $U/\bar{D}$  and  $\bar{INC}$  inputs. HIGH to LOW transitions on  $\bar{INC}$  will increment or decrement (depending on the state of the  $U/\bar{D}$  input) a five bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever  $\bar{CS}$  transitions HIGH while the  $\bar{INC}$  input is also HIGH.





The system may select the X9315, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep  $\bar{INC}$  LOW while taking  $\bar{CS}$  HIGH. The new wiper position will be maintained until

changed by the system or until a power-up/down cycle recalled the previously stored data.

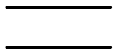
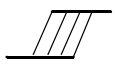
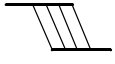

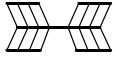
This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc...

The state of  $U/\bar{D}$  may be changed while  $\bar{CS}$  remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

**Mode Selection**

CS	INC	U/ $\bar{D}$	MODE
L		H	Wiper Up
L		L	Wiper Down
	H	X	Store Wiper Position
H	X	X	Standby Current
	L	X	No Store, Return to Standby

**Symbol Table**

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**Absolute Maximum Ratings**

Temperature under bias . . . . .	-65°C to +135°C
Storage temperature . . . . .	-65°C to +150°C
Voltage on CS, INC, U/D, V <sub>H</sub> , V <sub>L</sub> and V <sub>CC</sub> with respect to V <sub>SS</sub> . . . . .	-1V to +7V
$\Delta V =  V_H - V_L $ . . . . .	.5V
Lead temperature (soldering 10 seconds) . . . . .	300°C
I <sub>W</sub> (10 seconds) . . . . .	±7.5mA

**Recommended Operating Conditions**

Temperature (Commercial) . . . . .	0°C to +70°C
Temperature (Industrial) . . . . .	-40°C to +85°C
Supply Voltage (V <sub>CC</sub> ) (Note 4) Limits	
X9315 . . . . .	5V ± 10%
X9315-2.7 . . . . .	2.7V to 5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Potentiometer Characteristics** (Over recommended operating conditions unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	LIMITS			
			MIN	TYP	MAX.	UNIT
	End to end resistance tolerance				±20	%
V <sub>VH</sub>	V <sub>H</sub> terminal voltage		0		V <sub>CC</sub>	V
V <sub>VL</sub>	V <sub>L</sub> terminal voltage		0		V <sub>CC</sub>	V
	Power rating	R <sub>TOTAL</sub> ≥ 10kΩ			10	mW
R <sub>W</sub>	Wiper resistance	I <sub>W</sub> = 1mA, V <sub>CC</sub> = 5V		200	400	Ω
R <sub>W</sub>	Wiper resistance	I <sub>W</sub> = 1mA, V <sub>CC</sub> = 2.7V		400	1000	Ω
I <sub>W</sub>	Wiper current				±3.75	mA
	Noise	Ref: 1kHz		-120		dBV
	Resolution			3		%
	Absolute linearity <sup>(1)</sup>	V <sub>w(n)(actual)</sub> - V <sub>w(n)(expected)</sub>			±1	MI <sup>(3)</sup>
	Relative linearity <sup>(2)</sup>	V <sub>w(n+1)</sub> - [V <sub>w(n)</sub> + MI]			±0.2	MI <sup>(3)</sup>
	R <sub>TOTAL</sub> temperature coefficient			±300		ppm/°C
	Ratiometric temperature coefficient				±20	ppm/°C
C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub>	Potentiometer capacitances	See circuit #3		10/10/25		pF

- Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = (V<sub>w(n)(actual)</sub> - V<sub>w(n)(expected)</sub>) = ±1 MI Maximum.  
 (2) Relative linearity is a measure of the error in step size between taps = R<sub>w(n+1)</sub> - [R<sub>w(n)</sub> + MI] = ±0.2 MI.  
 (3) 1 MI = Minimum Increment = R<sub>TOT</sub>/31.  
 (4) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
 (5) This parameter is periodically sampled and not 100% tested

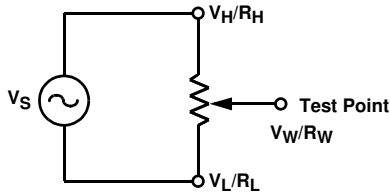
**DC Electrical Specifications** (Over recommended operating conditions unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP <sup>(4)</sup>	MAX	
I <sub>CC1</sub>	V <sub>CC</sub> active current (Increment)	$\overline{CS} = V_{IL}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = 0.4V$ @ max. t <sub>CYC</sub>			50	μA
I <sub>CC2</sub>	V <sub>CC</sub> active current (Store) (EEPROM Store)	$\overline{CS} = V_{IH}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = V_{IH}$ @ max. t <sub>WR</sub>			400	μA
I <sub>SB</sub>	Standby supply current	$\overline{CS} = V_{CC} - 0.3V$ , $U/\overline{D}$ and $\overline{INC} = V_{SS}$ or $V_{CC} - 0.3V$			1	μA
I <sub>LI</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ input leakage current	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>			±10	μA
V <sub>IH</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ input HIGH voltage		V <sub>CC</sub> x 0.7		V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ input LOW voltage		-0.5		V <sub>CC</sub> x 0.1	V
C <sub>IN</sub> <sup>(5)</sup>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ input capacitance	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>SS</sub> , T <sub>A</sub> = 25°C, f = 1MHz			10	pF

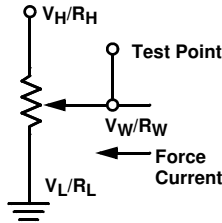
**Endurance and Data Retention**

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

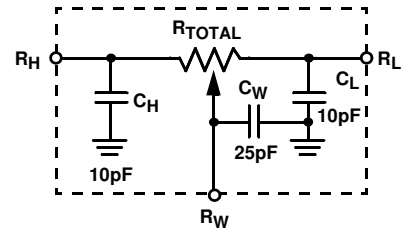
**Test Circuit #1**



**Test Circuit #2**



**Circuit #3 SPICE Macro Model**



**AC Conditions of Test**

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

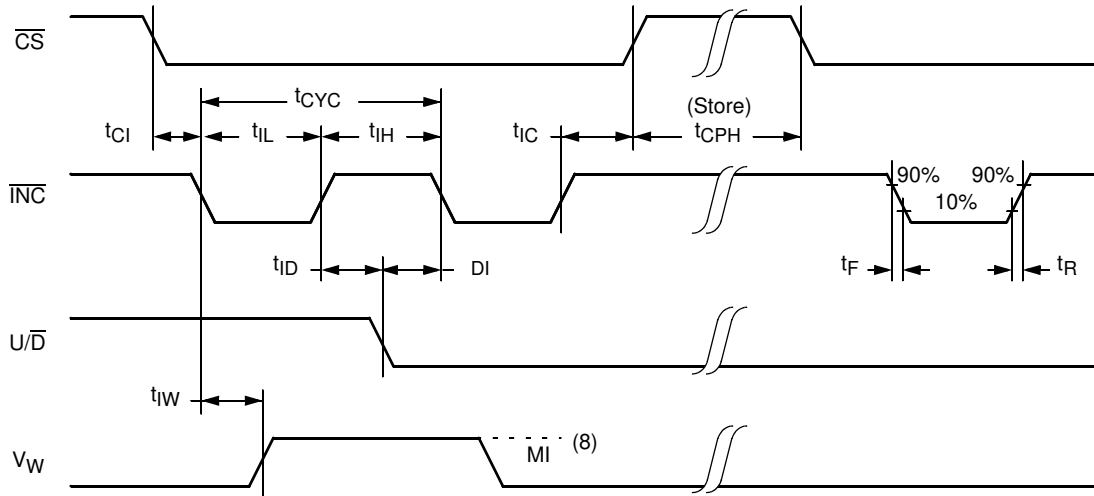
**AC Electrical Specifications** (Over recommended operating conditions unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP(6)	MAX	
$t_{CI}$	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
$t_{D}$	$\overline{INC}$ HIGH to $U/\overline{D}$ change	100			ns
$t_{DI}$	$U/\overline{D}$ to $\overline{INC}$ setup	2.9			$\mu$ s
$t_{iL}$	$\overline{INC}$ LOW period	1			$\mu$ s
$t_{iH}$	$\overline{INC}$ HIGH period	1			$\mu$ s
$t_{iC}$	$\overline{INC}$ Inactive to $\overline{CS}$ inactive	1			$\mu$ s
$t_{CPH}$	$\overline{CS}$ Deselect time (NO STORE)	100			ns
$t_{CPH}$	$\overline{CS}$ Deselect time (STORE)	10			ms
$t_{iW}$	$\overline{INC}$ to $V_w$ change		1	5	$\mu$ s
$t_{CYC}$	$\overline{INC}$ cycle time	4			$\mu$ s
$t_R, t_F^{(7)}$	$\overline{INC}$ input rise and fall time			500	$\mu$ s
$t_{PU}^{(7)}$	Power-up to wiper stable			5	$\mu$ s
$t_R V_{CC}^{(7)}$	$V_{CC}$ power-up rate	0.2		50	V/ms
$t_{WR}$	Store cycle		5	10	ms

### Power-up and Down Requirements

There are no restrictions on the power-up or power-down conditions of  $V_{CC}$  and the voltages applied to the potentiometer pins provided that  $V_{CC}$  is always more positive than or equal to  $V_H$ ,  $V_L$ , and  $V_W$ , i.e.,  $V_{CC} \geq V_H, V_L, V_W$ . The  $V_{CC}$  ramp rate spec is always in effect.

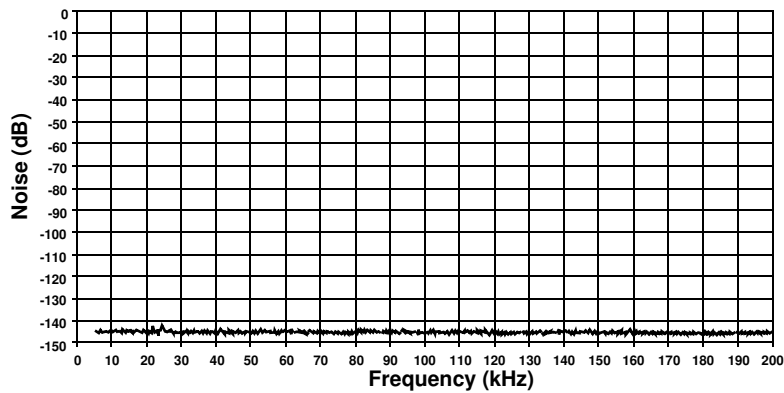
### AC Timing



- Notes: (6) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.
- (7) This parameter is not 100% tested.
- (8) MI in the A.C. timing diagram refers to the minimum incremental change in the  $V_W$  output due to a change in the wiper position.

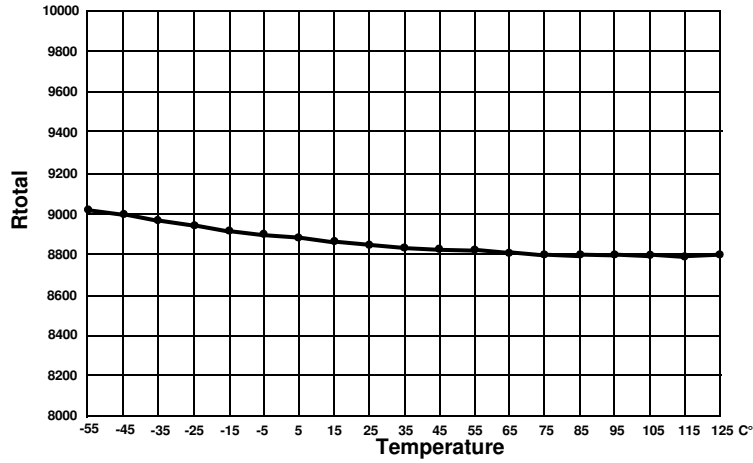
### Performance Characteristics (Typical)

#### Typical Noise

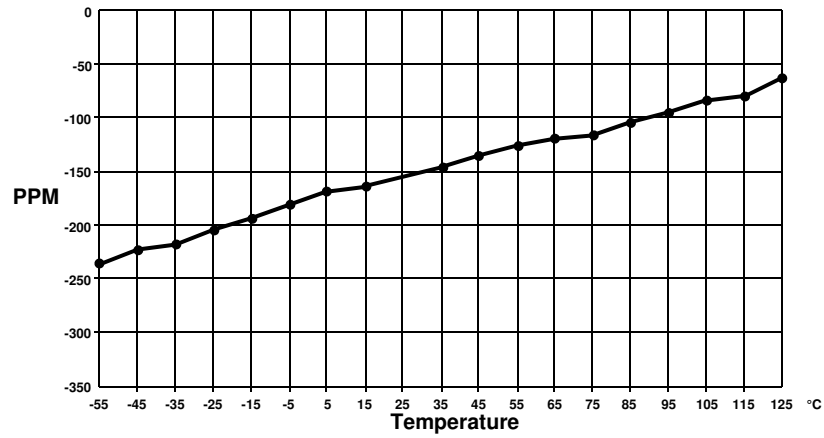




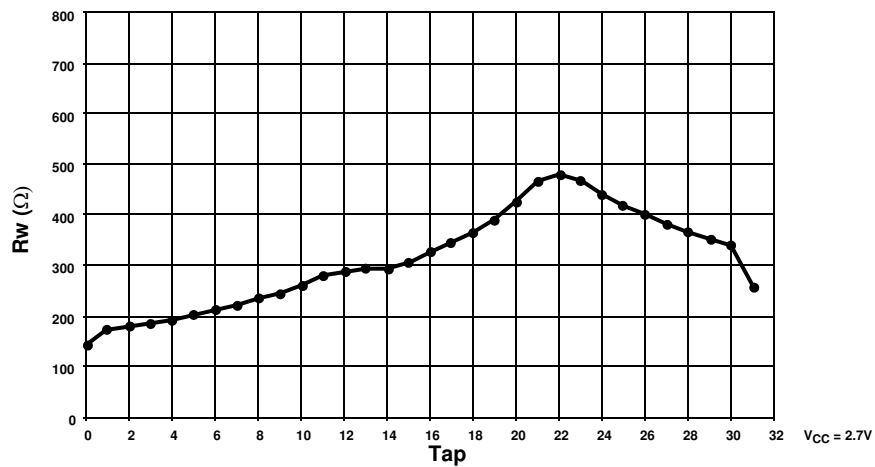
**Typical  $R_{total}$  vs. Temperature**



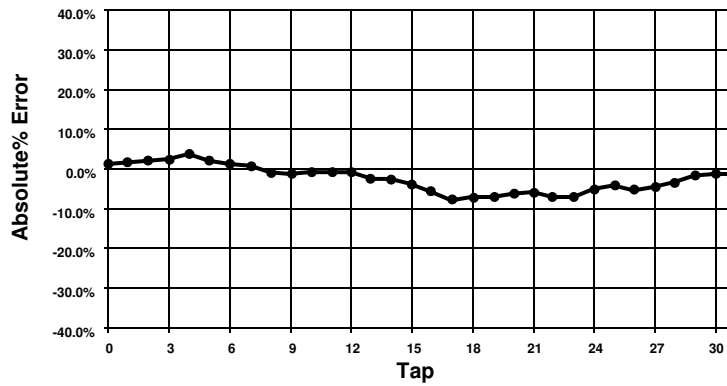
**Typical Total Resistance Temperature Coefficient**



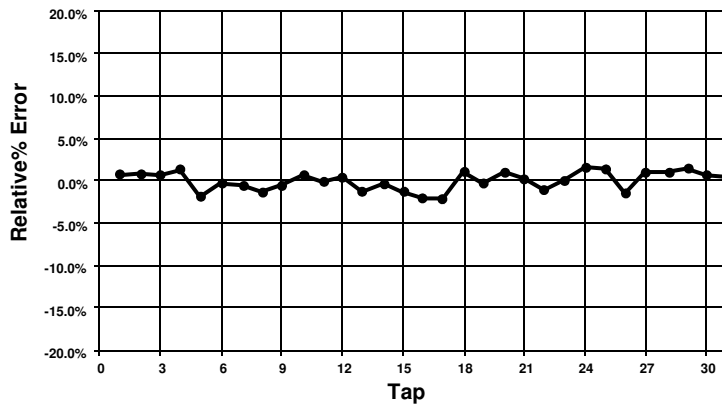
**Typical Wiper Resistance**



**Typical Absolute% Error per Tap Position**



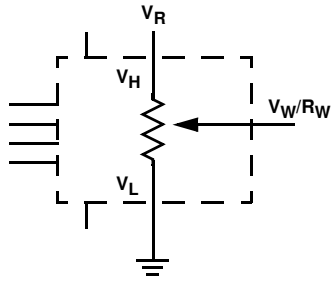
**Typical Relative% Error per Tap Position**



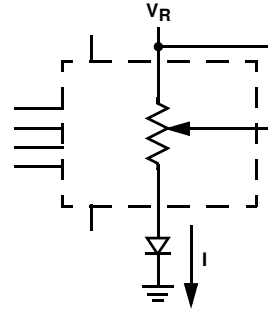
**Applications Information**

Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

**Basic Configurations of Electronic Potentiometers**



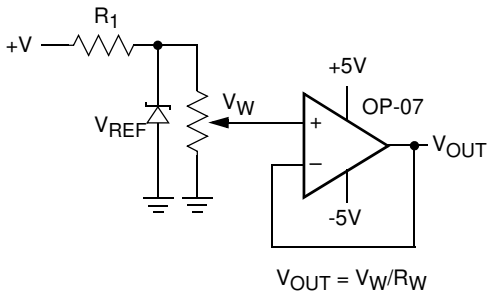
Three terminal potentiometer;  
variable voltage divider



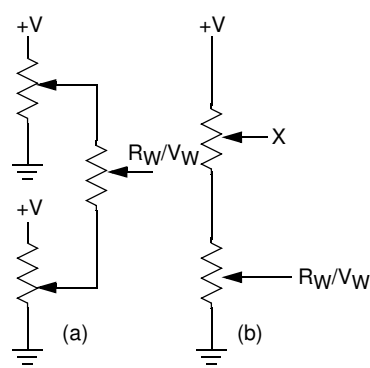
Two terminal variable resistor;  
variable current

**Basic Circuits**

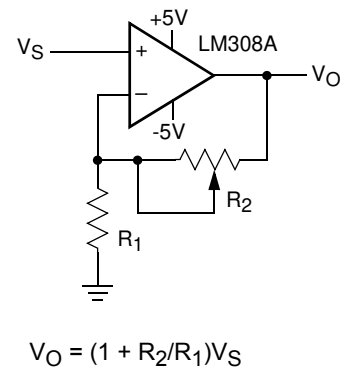
**Buffered Reference Voltage**



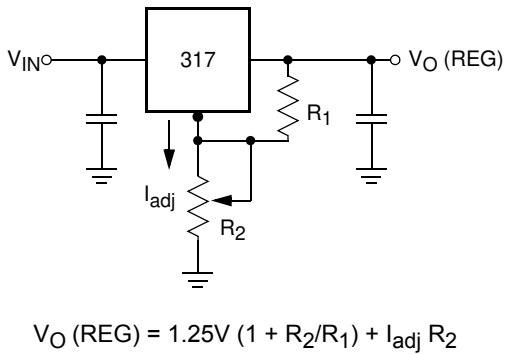
**Cascading Techniques**



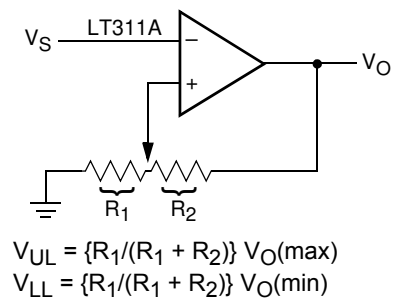
**Noninverting Amplifier**



**Voltage Regulator**



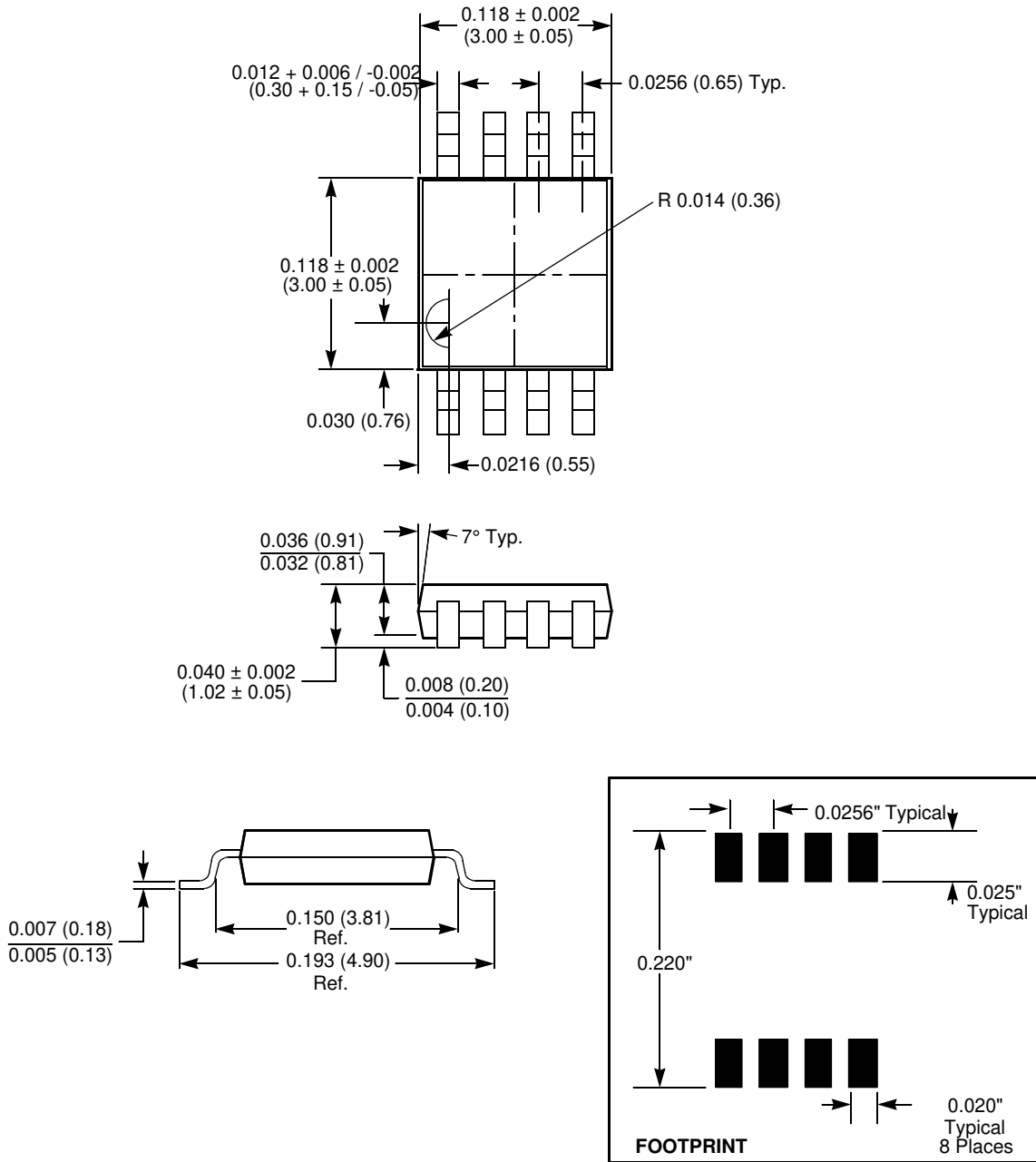
**Comparator with Hysteresis**



(for additional circuits see AN115)

Packaging Information

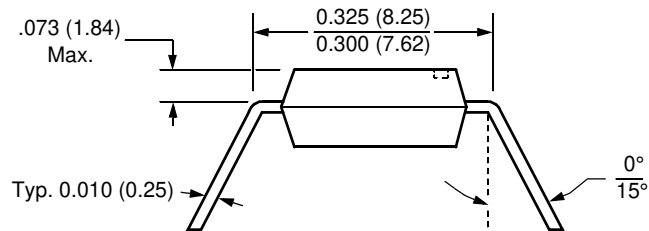
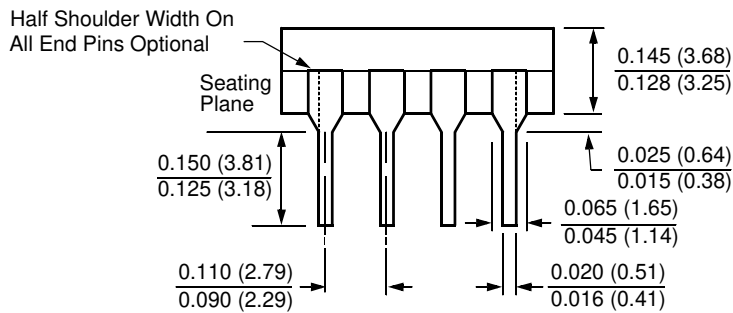
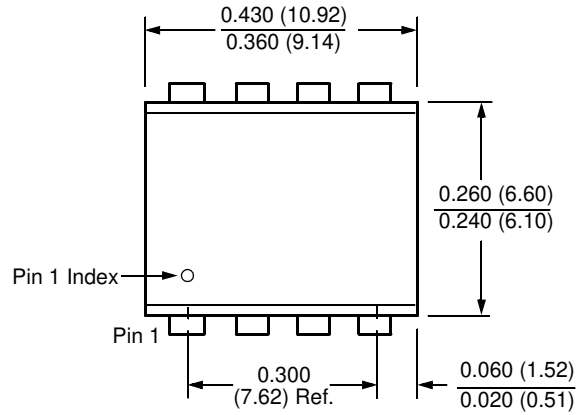
8-Lead Miniature Small Outline Gull Wing Package Type M



**NOTE:**  
 1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

Packaging Information

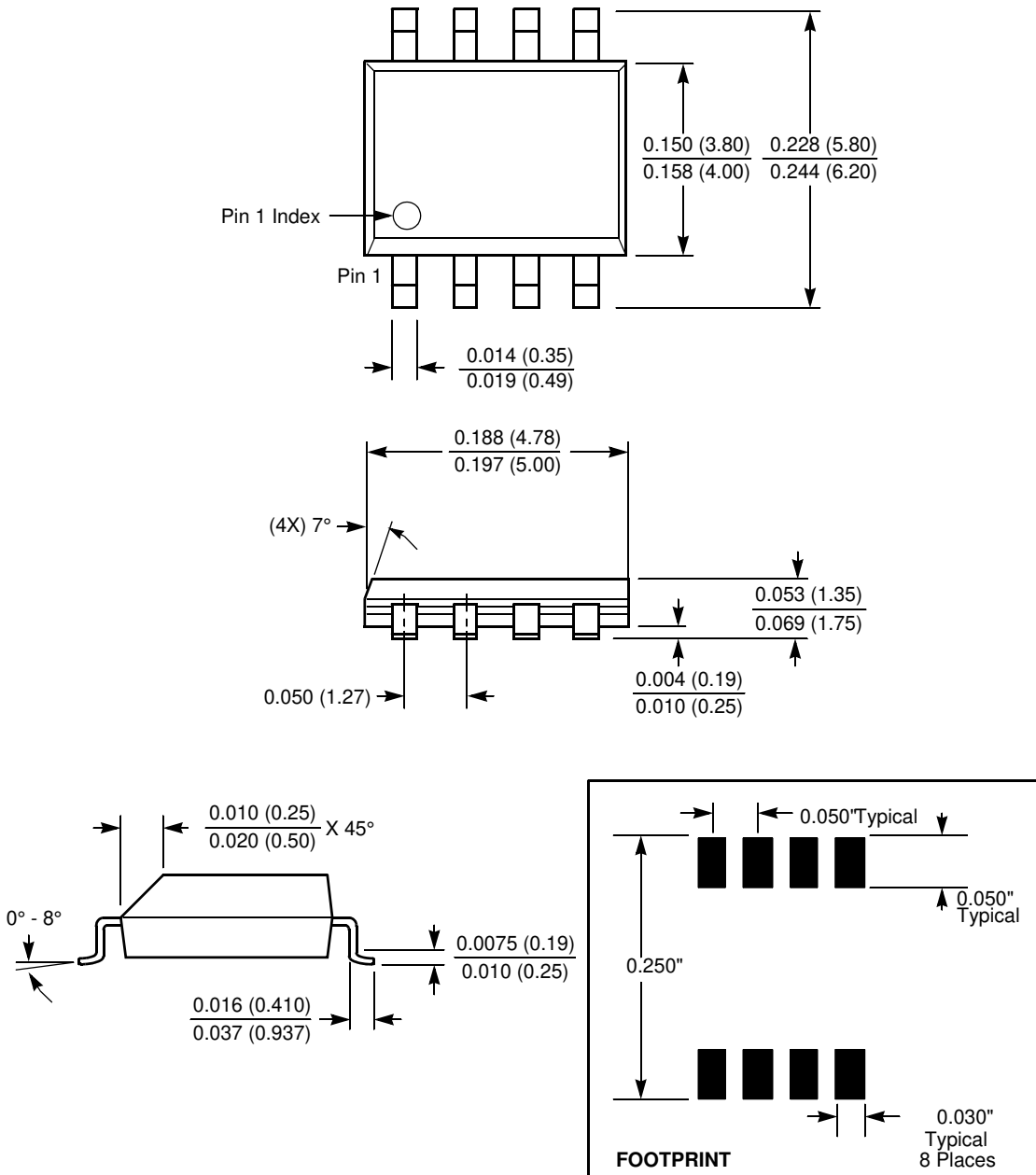
8-Lead Plastic Dual In-Line Package Type P



- NOTE:**
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
  2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

Packaging Information

8-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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**X9315**









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**Digitally Controlled Potentiometer (XDCP™)**

 <a href="#">Datasheets, Related Docs &amp; Simulations</a>	 <a href="#">Description</a>	 <a href="#">Key Features</a>	 <a href="#">Parametric Data</a>	 <a href="#">Application Diagrams</a>	 <a href="#">Related Devices</a>
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**Ordering Information**









 **RoHS/Pb-Free/Green Device**






















Part No.	Design-In Status	Temp.	Package	MSL	Price US \$	
X9315TM	Active	Comm	<a href="#">8 Ld MSOP</a>	1	1.52	<a href="#">Buy</a>
X9315TM-2.7	Active	Comm	<a href="#">8 Ld MSOP</a>	1	1.67	<a href="#">Buy</a>
X9315TM-2.7T1	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1	1.67	<a href="#">Buy</a>
X9315TMI	Active	Ind	<a href="#">8 Ld MSOP</a>	1	1.75	<a href="#">Buy</a>
X9315TMI-2.7	Active	Ind	<a href="#">8 Ld MSOP</a>	1	1.92	<a href="#">Buy</a>
X9315TMI-2.7C7898	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>
X9315TMI-2.7T1	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1	1.92	<a href="#">Buy</a>
X9315TMI-2.7T2	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	3	1.92	<a href="#">Buy</a>
X9315TMIT1	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1	1.75	<a href="#">Buy</a>
X9315TMIZ 	Active	Ind	<a href="#">8 Ld MSOP</a>	2	1.75	<a href="#">Buy</a>
X9315TMIZ-2.7 	Active	Ind	<a href="#">8 Ld MSOP</a>	2	1.92	<a href="#">Buy</a>
X9315TMIZ-2.7T1 	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	2	1.92	<a href="#">Buy</a>
X9315TMIZT1 	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	2	1.75	<a href="#">Buy</a>
X9315TMT1	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1	1.52	<a href="#">Buy</a>
X9315TMZ 	Active	Comm	<a href="#">8 Ld MSOP</a>	2	1.52	<a href="#">Buy</a>
X9315TMZ-2.7 	Active	Comm	<a href="#">8 Ld MSOP</a>	2	1.67	<a href="#">Buy</a>
X9315TMZ-2.7T1 	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	2	1.67	<a href="#">Buy</a>
X9315TMZT1 	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	2	1.52	<a href="#">Buy</a>
X9315TP	Active	Comm	<a href="#">8 Ld PDIP</a>	N/A	1.45	<a href="#">Buy</a>
X9315TP-2.7	Active	Comm	<a href="#">8 Ld PDIP</a>	N/A	1.59	<a href="#">Buy</a>
X9315TPI	Active	Ind	<a href="#">8 Ld PDIP</a>	N/A	1.66	<a href="#">Buy</a>
X9315TPI-2.7	Active	Ind	<a href="#">8 Ld PDIP</a>	N/A	1.83	<a href="#">Buy</a>
X9315TS	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.30	<a href="#">Buy</a>
X9315TS-2.7	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.59	<a href="#">Buy</a>
X9315TS-2.7T1	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.59	<a href="#">Buy</a>
X9315TSI	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.62	<a href="#">Buy</a> <a href="#">Sample</a>
X9315TSI-2.7	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.83	<a href="#">Buy</a>
X9315TSI-2.7C7898	Active	Ind	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>

X9315TSI-2.7T1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.83	<a href="#">Buy</a>	
X9315TSIT1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.62	<a href="#">Buy</a>	
X9315TSIZ 	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.62	<a href="#">Buy</a>	
X9315TSIZ-2.7 	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.83	<a href="#">Buy</a>	
X9315TSIZ-2.7T1 	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.83	<a href="#">Buy</a>	
X9315TSIZT1 	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.62	<a href="#">Buy</a>	
X9315TST1	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.30	<a href="#">Buy</a>	
X9315TSZ 	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.30	<a href="#">Buy</a>	
X9315TSZ-2.7 	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.59	<a href="#">Buy</a>	
X9315TSZ-2.7T1 	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.59	<a href="#">Buy</a>	
X9315TSZT1 	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.30	<a href="#">Buy</a>	
X9315UM	Active	Comm	<a href="#">8 Ld MSOP</a>	1	1.52	<a href="#">Buy</a>	<a href="#">Sample</a>
X9315UM-2.7	Active	Comm	<a href="#">8 Ld MSOP</a>	1	1.67	<a href="#">Buy</a>	
X9315UM-2.7C7958	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>	
X9315UM-2.7C7964	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>	
X9315UM-2.7T1	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1	1.67	<a href="#">Buy</a>	
X9315UM-2.7T1C7958	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>	
X9315UM-2.7T1C7964	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>	
X9315UM-2.7T2	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	3	1.67	<a href="#">Buy</a>	
X9315UM-2.7T2C7964	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	3		<a href="#">Buy</a>	
X9315UMI	Active	Ind	<a href="#">8 Ld MSOP</a>	1	1.75	<a href="#">Buy</a>	
X9315UMI-2.7	Active	Ind	<a href="#">8 Ld MSOP</a>	1	1.92	<a href="#">Buy</a>	
X9315UMI-2.7C7898	Active	Ind	<a href="#">8 Ld MSOP</a>	1		<a href="#">Buy</a>	
X9315UMI-2.7C7984	Active	Ind	<a href="#">8 Ld MSOP</a>	1		<a href="#">Buy</a>	
X9315UMI-2.7T1	Active	Ind	<a href="#">8 Ld MSOP</a>	1	1.92	<a href="#">Buy</a>	
X9315UMI-2.7T1C7898	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>	
X9315UMI-2.7T1C7975	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>	
X9315UMI-2.7T1C7984	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>	
X9315UMI-2.7T2	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	3	1.92	<a href="#">Buy</a>	
X9315UMI-2.7T2C7898	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	3		<a href="#">Buy</a>	
X9315UMIC7898	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>	
X9315UMIT1	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1	1.75	<a href="#">Buy</a>	
X9315UMIT2	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	3	1.75	<a href="#">Buy</a>	
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X9315UMIZ 	Active	Ind	<a href="#">8 Ld MSOP</a>	2	1.75	<a href="#">Buy</a>	



X9315UMIZ-2.7	Active	Ind	<a href="#">8 Ld MSOP</a>	2	1.92	<a href="#">Buy</a>
X9315UMIZ-2.7T1	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	2	1.92	<a href="#">Buy</a>
X9315UMIZT1	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	2	1.75	<a href="#">Buy</a>
X9315UMT1	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1	1.52	<a href="#">Buy</a>
X9315UMZ	Active	Comm	<a href="#">8 Ld MSOP</a>	2	1.52	<a href="#">Buy</a>
X9315UMZ-2.7	Active	Ind	<a href="#">8 Ld MSOP</a>	2	1.67	<a href="#">Buy</a>
X9315UMZ-2.7C7964	Active	Comm	<a href="#">8 Ld MSOP</a>	2		<a href="#">Buy</a> <a href="#">Sample</a>
X9315UMZ-2.7T1	Active	Comm	<a href="#">8 Ld MSOP</a>	2	1.67	<a href="#">Buy</a>
X9315UMZ-2.7T1C7964	Active	Comm	<a href="#">8 Ld MSOP</a>	2		<a href="#">Buy</a>
X9315UMZT1	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	2	1.52	<a href="#">Buy</a>
X9315UP	Active	Comm	<a href="#">8 Ld PDIP</a>	N/A	1.45	<a href="#">Buy</a>
X9315UP-2.7	Active	Comm	<a href="#">8 Ld PDIP</a>	N/A	1.59	<a href="#">Buy</a>
X9315UPI	Active	Ind	<a href="#">8 Ld PDIP</a>	N/A	1.66	<a href="#">Buy</a>
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X9315US-2.7T2	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	3	1.59	<a href="#">Buy</a>
X9315USI	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.62	<a href="#">Buy</a>
X9315USI-2.7	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.83	<a href="#">Buy</a>
X9315USI-2.7C7898	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1		<a href="#">Buy</a>
X9315USI-2.7T1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.83	<a href="#">Buy</a>
X9315USIT1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.62	<a href="#">Buy</a>
X9315USIZ	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.62	<a href="#">Buy</a>
X9315USIZ-2.7	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.83	<a href="#">Buy</a>
X9315USIZ-2.7T1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.83	<a href="#">Buy</a>
X9315USIZT1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.62	<a href="#">Buy</a>
X9315UST1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.30	<a href="#">Buy</a>
X9315UST2	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	3	1.30	<a href="#">Buy</a>
X9315USZ	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.30	<a href="#">Buy</a>
X9315USZ-2.7	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.59	<a href="#">Buy</a>
X9315USZ-2.7T1	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.59	<a href="#">Buy</a>
X9315USZT1	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.30	<a href="#">Buy</a>
X9315WM	Active	Comm	<a href="#">8 Ld MSOP</a>	1	1.92	<a href="#">Buy</a>
X9315WM-2.7	Active	Comm	<a href="#">8 Ld MSOP</a>	1	1.68	<a href="#">Buy</a>
X9315WM-2.7C7975	Active	Comm	<a href="#">8 Ld MSOP</a>	1		<a href="#">Buy</a>
X9315WM-2.7T1	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1	1.68	<a href="#">Buy</a>
X9315WM-2.7T1C7964	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1		<a href="#">Buy</a>

X9315WM-2.7T2	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	3	1.68	<a href="#">Buy</a>
X9315WMI	Active	Ind	<a href="#">8 Ld MSOP</a>	1	1.92	<a href="#">Buy</a>
X9315WMI-2.7	Active	Ind	<a href="#">8 Ld MSOP</a>	1	2.12	<a href="#">Buy</a>
X9315WMI-2.7C7898	Active	Ind	<a href="#">8 Ld MSOP</a>	1		<a href="#">Buy</a>
X9315WMI-2.7C7941	Active	Ind	<a href="#">8 Ld MSOP</a>	1		<a href="#">Buy</a>
X9315WMI-2.7T1	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1	2.12	<a href="#">Buy</a>
X9315WMI-2.7T1C7898	Active	Ind	<a href="#">8 Ld MSOP</a>	1		<a href="#">Buy</a>
X9315WMI-2.7T2	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	3	2.12	<a href="#">Buy</a>
X9315WMI-2.7T2C7898	Active	Ind	<a href="#">8 Ld MSOP</a>	3		<a href="#">Buy</a>
X9315WMI-2.7T2C7941	Active	Ind	<a href="#">8 Ld MSOP</a>	3		<a href="#">Buy</a>
X9315WMIT1	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	1	1.92	<a href="#">Buy</a>
X9315WMIT2	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	3	1.92	<a href="#">Buy</a>
X9315WMIZ 	Active	Ind	<a href="#">8 Ld MSOP</a>	2	1.92	<a href="#">Buy</a>
X9315WMIZ-2.7 	Active	Ind	<a href="#">8 Ld MSOP</a>	2	2.12	<a href="#">Buy</a> <a href="#">Sample</a>
X9315WMIZ-2.7T1 	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	2	2.12	<a href="#">Buy</a>
X9315WMIZT1 	Active	Ind	<a href="#">8 Ld MSOP T+R</a>	2	1.92	<a href="#">Buy</a>
X9315WMT1	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	1	1.92	<a href="#">Buy</a>
X9315WMT1C7517	Active	Comm	<a href="#">8 Ld MSOP</a>	1		<a href="#">Buy</a>
X9315WMZ 	Active	Comm	<a href="#">8 Ld MSOP</a>	2	1.92	<a href="#">Buy</a>
X9315WMZ-2.7 	Active	Comm	<a href="#">8 Ld MSOP</a>	2	1.68	<a href="#">Buy</a>
X9315WMZ-2.7T1 	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	2	1.68	<a href="#">Buy</a>
X9315WMZT1 	Active	Comm	<a href="#">8 Ld MSOP T+R</a>	2	1.92	<a href="#">Buy</a>
X9315WP	Active	Comm	<a href="#">8 Ld SOIC</a>	N/A	1.30	<a href="#">Buy</a>
X9315WP-2.7	Active	Comm	<a href="#">8 Ld SOIC</a>	N/A	1.44	<a href="#">Buy</a>
X9315WPC7898	Active	Comm	<a href="#">8 Ld SOIC</a>	N/A		<a href="#">Buy</a>
X9315WPI	Active	Ind	<a href="#">8 Ld SOIC</a>	N/A	1.62	<a href="#">Buy</a>
X9315WPI-2.7	Active	Ind	<a href="#">8 Ld SOIC</a>	N/A	1.79	<a href="#">Buy</a>
X9315WPI-2.7C7898	Active	Ind	<a href="#">8 Ld SOIC</a>	N/A		<a href="#">Buy</a>
X9315WS	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.30	<a href="#">Buy</a> <a href="#">Sample</a>
X9315WS-2.7	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.44	<a href="#">Buy</a>
X9315WS-2.7C7898	Active	Comm	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WS-2.7T1	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.44	<a href="#">Buy</a>
X9315WS-2.7T2	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	3	1.44	<a href="#">Buy</a>
X9315WSC7898	Active	Comm	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WSI	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.62	<a href="#">Buy</a>
X9315WSI-2.7	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.79	<a href="#">Buy</a>
X9315WSI-2.7C7898	Active	Ind	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WSI-2.7T1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.79	<a href="#">Buy</a>
X9315WSI-2.7T1C7898	Active	Ind	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WSI-2.7T2C7898	Active	Ind	<a href="#">8 Ld SOIC</a>	3		<a href="#">Buy</a>

X9315WSIC7898	Active	Ind	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WSIC7942	Active	Ind	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WSIT1	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.62	<a href="#">Buy</a>
X9315WSIT1C7898	Active	Ind	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WSIT1C7942	Active	Ind	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WSIT2	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	3	1.62	<a href="#">Buy</a>
X9315WSIT2C7898	Active	Ind	<a href="#">8 Ld SOIC</a>	3		<a href="#">Buy</a>
X9315WSIZ 	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.62	<a href="#">Buy</a>
X9315WSIZ-2.7 	Active	Ind	<a href="#">8 Ld SOIC</a>	1	1.79	<a href="#">Buy</a>
X9315WSIZ-2.7T1 	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.79	<a href="#">Buy</a>
X9315WSIZT1 	Active	Ind	<a href="#">8 Ld SOIC T+R</a>	1	1.62	<a href="#">Buy</a>
X9315WST1	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.30	<a href="#">Buy</a>
X9315WST1C7975	Active	Comm	<a href="#">8 Ld SOIC</a>	1		<a href="#">Buy</a>
X9315WST2	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	3	1.30	<a href="#">Buy</a>
X9315WSZ 	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.30	<a href="#">Buy</a>
X9315WSZ-2.7 	Active	Comm	<a href="#">8 Ld SOIC</a>	1	1.44	<a href="#">Buy</a>
X9315WSZ-2.7T1 	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.44	<a href="#">Buy</a>
X9315WSZT1 	Active	Comm	<a href="#">8 Ld SOIC T+R</a>	1	1.30	<a href="#">Buy</a>
XLABVIEW01	Active			N/A	91.77	<a href="#">Buy</a> <a href="#">Sample</a>
XLABVIEW01Z 	Active		Eval Board	N/A	91.77	<a href="#">Buy</a>
X9315TMIZ-2.7T2 	Coming Soon	Ind	<a href="#">8 Ld MSOP T+R</a>	3		
X9315USZ-2.7T2 	Coming Soon	Comm	<a href="#">8 Ld SOIC T+R</a>	3		
X9315WMIZ-2.7T2 	Coming Soon	Ind	<a href="#">8 Ld MSOP T+R</a>	3		
X9315WMZ-2.7T2 	Coming Soon	Comm	<a href="#">8 Ld MSOP T+R</a>	3	1.68	
X9315WSIZT2 	Coming Soon	Comm	<a href="#">8 Ld SOIC T+R</a>	3		
X9315UMIZ-2.7T2 	InActive	Ind	<a href="#">8 Ld MSOP T+R</a>	3		
X9315UMIZT2 	InActive	Ind	<a href="#">8 Ld MSOP T+R</a>	3		
X9315UMZ-2.7T2 	InActive	Comm	<a href="#">8 Ld MSOP T+R</a>	3	1.67	
X9315USZT2 	InActive	Comm	<a href="#">8 Ld SOIC T+R</a>	3		
X9315WMIZT2 	InActive	Ind	<a href="#">8 Ld MSOP T+R</a>	3		
X9315WSZ-2.7T2 	InActive	Comm	<a href="#">8 Ld SOIC T+R</a>	3	1.44	
X9315WSZT2 	InActive	Comm	<a href="#">8 Ld SOIC T+R</a>	3		

The price listed is the manufacturer's suggested retail price for quantities between 100 and 999 units. However, prices in today's market are fluid and may change without notice.

MSL = Moisture Sensitivity Level - per IPC/JEDEC J-STD-020

SMD = Standard Microcircuit Drawing

### Description

The Intersil X9315 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the CS, U/D, and INC inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

\$\$ control \$\$ parameter adjustments \$\$ signal processing

## Key Features

- Solid-state potentiometer
- 3-wire serial interface
- 32 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements
  - Temperature compensated
  - End to end resistance range  $\pm 20\%$
  - Terminal voltage, 0 to  $V_{CC}$
- Low power CMOS
  - $V_{CC} = 2.7V$  or  $5V$
  - Active current,  $50/400iA$  max.
  - Standby current,  $1iA$  max.
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- $R_{TOTAL}$  values =  $10k\Omega$ ,  $50k\Omega$ ,  $100k\Omega$
- Packages
  - 8 Ld SOIC, MSOP and PDIP
- Pb-free plus anneal available (RoHS compliant)

## Related Documentation



Application Note(s):

- [A Compendium of Application Circuits for Intersil's Digitally-Controlled \(XDCP\) Potentiometers](#)
- [A Primer on Digitally-Controlled Potentiometers](#)
- [Application of Intersil Digitally Controlled Potentiometers \(XDCP™\) as Hybrid Analog/Digital Feedback System Control Elements](#)
- [DC/DC Module Trim with Digital Potentiometers](#)
- [Designing Power Supplies Using Intersil's XDCP Mixed Signal Products](#)
- [Power Supply and DC to DC Converter Control using Intersil Digitally Controlled Potentiometers \(XDCPs\)](#)
- [Putting Analog On The Bus](#)
- [Shaft Encoder Drives Multiple Intersil Digitally Controlled Potentiometers \(XDCPs\)](#)
- [Third Generation E<sup>2</sup>POT Devices From Intersil-Part 1](#)
- [Tone, Balance, and Volume Control using a Quad XDCP](#)
- [Working with the Intersil 3-Wire DCP Devices](#)



Datasheet(s):

- [Digitally Controlled Potentiometer \(XDCP™\)](#)



Technical Brief(s):

- [Converting a Fixed PWM to an Adjustable PWM](#)



Evaluation Board(s):

- [Intersil\\_XDCP\\_Test\\_UTILITY\\_Manual\\_rev\\_3.2.3.pdf](#)
- [LabView\\_XDCP\\_Software.zip](#)
- [LabView\\_XDCP\\_Upgrade\\_3.2.3.zip](#)
- [Readme\\_XicorLabVIEW\\_V3.2.3.txt](#)
- [XDCP\\_Vref Evaluation Board Kit Documentation and Software](#)
- [accessHW.zip](#)



Technical Homepage:

- [Digitally Controlled Potentiometers \(DCPs\) and Capacitors \(DCCs\)](#)
- [Precision Analog Homepage](#)

## **PT** Parametric Data

Number of DCPs	Single
Number of Taps	32
Memory Type	Non-Volatile
Bus Interface Type	3-Wire (Up/Down)
Resistance Options (k $\Omega$ )	10, 50, 100
V <sub>CC</sub> Range (V)	2.7 to 5.5
DCP Differential Terminal Voltage (V)	0 to +5.5
Terminal Voltage Range V <sub>L</sub> to V <sub>H</sub> (V)	0 to V <sub>CC</sub>
Resistance Taper	Linear
Wiper Current (mA)	$\pm 1$
Wiper Resistance ( $\Omega$ )	200
Standby Current I <sub>SB</sub> ( $\mu$ A)	1

## Application Block Diagrams

- [Digital Projector](#)

## Related Devices

**PT** [Parametric Table](#)

- [X9313](#) Digitally Controlled Potentiometer (XD<sub>DCP</sub><sup>TM</sup>), Linear, 32 Taps, 3 Wire Interface, Terminal Voltages  $\pm V_{CC}$
- [X9314](#) Single Digitally Controlled Potentiometer (XD<sub>DCP</sub><sup>TM</sup>)
- [X93154](#) Digitally Controlled Potentiometer (XD<sub>DCP</sub><sup>TM</sup>)
- [X93155](#) Digitally Controlled Potentiometer (XD<sub>DCP</sub><sup>TM</sup>)
- [X93156](#) Single Digitally Controlled Potentiometer (XD<sub>DCP</sub><sup>TM</sup>), Low Noise, Low Power, 3 wire Up/Down, 32 Taps
- [X9511](#) Single Digitally-Controlled (XD<sub>DCP</sub><sup>TM</sup>) Potentiometer (Push Button Controlled)