Digitally Controlled Potentiometer (XDCP™)

The Intersil X9315 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

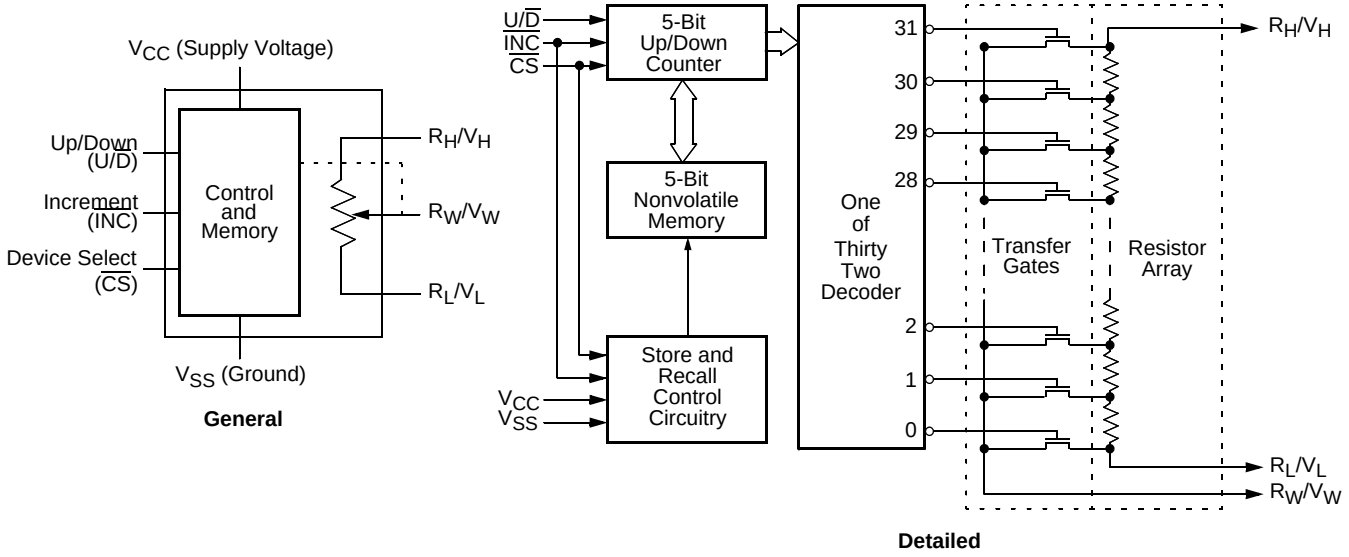
The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Control
- Parameter Adjustments
- Signal Processing

Features

- Solid-state potentiometer
- 3-wire serial interface
- 32 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements
  - Temperature compensated
  - End to end resistance range ± 20%
  - Terminal voltage, 0 to V_{CC}
- Low power CMOS
  - V_{CC} = 2.7V or 5V
  - Active current, 50/400µA max.
  - Standby current, 1µA max.
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- R_{TOTAL} values = 10kΩ, 50kΩ, 100kΩ
- Packages
  - 8 Ld SOIC, MSOP and PDIP
- Pb-free plus anneal available (RoHS compliant)

Block Diagram



Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE
X9315WM*	AAW	5 ±10%	10	0 to 70	8 Ld MSOP
X9315WMZ* (Note)	DDT			0 to 70	8 Ld MSOP (Pb-free)
X9315WMI*	AAX			-40 to 85	8 Ld MSOP
X9315WMIZ* (Note)	AKW			-40 to 85	8 Ld MSOP (Pb-free)
X9315WP	X9315WP			0 to 70	8 Ld PDIP
X9315WPI	X9315WP I			-40 to 85	8 Ld PDIP
X9315WS*	X9315W			0 to 70	8 Ld SOIC
X9315WSZ* (Note)	X9315W Z			0 to 70	8 Ld SOIC (Pb-free)
X9315WSI*	X9315W I			-40 to 85	8 Ld SOIC
X9315WSIZ* (Note)	X9315W Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9315UM*			50	0 to 70	8 Ld MSOP
X9315UMZ* (Note)	DDS			0 to 70	8 Ld MSOP (Pb-free)
X9315UMI*	AEB			-40 to 85	8 Ld MSOP
X9315UMIZ* (Note)	DDR			-40 to 85	8 Ld MSOP (Pb-free)
X9315UP	X9315UP			0 to 70	8 Ld PDIP
X9315UPI	X9315UP I			-40 to 85	8 Ld PDIP
X9315US*	X9315U			0 to 70	8 Ld SOIC
X9315USZ* (Note)	X9315U Z			0 to 70	8 Ld SOIC (Pb-free)
X9315USI*	X9315U I			-40 to 85	8 Ld SOIC
X9315USIZ* (Note)	X9315U Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9315TM*	AEJ		100	0 to 70	8 Ld MSOP
X9315TMZ* (Note)	DDN			0 to 70	8 Ld MSOP (Pb-free)
X9315TMI*	ADZ			-40 to 85	8 Ld MSOP
X9315TMIZ* (Note)	DDL			-40 to 85	8 Ld MSOP (Pb-free)
X9315TP	X9315TP			0 to 70	8 Ld PDIP
X9315TPI	X9315TP I			-40 to 85	8 Ld PDIP
X9315TS*	X9315T			0 to 70	8 Ld SOIC
X9315TSZ* (Note)	X9315T Z			0 to 70	8 Ld SOIC (Pb-free)
X9315TSI*	X9315T I			-40 to 85	8 Ld SOIC
X9315TSIZ* (Note)	X9315T Z I			-40 to 85	8 Ld SOIC (Pb-free)

Ordering Information (Continued)

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE
X9315TP-2.7	X9315TP F	2.7-5.5	10	0 to 70	8 Ld PDIP
X9315TPI-2.7	X9315TP G			-40 to 85	8 Ld PDIP
X9315WM-2.7*	AAU			0 to 70	8 Ld MSOP
X9315WMZ-2.7* (Note)	AOI			0 to 70	8 Ld MSOP (Pb-free)
X9315WMI-2.7*	AAV			-40 to 85	8 Ld MSOP
X9315WMIZ-2.7* (Note)				-40 to 85	8 Ld MSOP (Pb-free)
X9315WP-2.7	X9315WP F			0 to 70	8 Ld PDIP
X9315WPI-2.7	X9315WP G			-40 to 85	8 Ld PDIP
X9315WS-2.7*	X9315W F			0 to 70	8 Ld SOIC
X9315WSZ-2.7* (Note)	X9315W Z F			0 to 70	8 Ld SOIC (Pb-free)
X9315WSI-2.7*	X9315W G			-40 to 85	8 Ld SOIC
X9315WSIZ-2.7* (Note)	X9315W Z G			-40 to 85	8 Ld SOIC (Pb-free)
X9315UM-2.7*	AEK		50	0 to 70	8 Ld MSOP
X9315UMZ-2.7* (Note)	AKU			0 to 70	8 Ld MSOP (Pb-free)
X9315UMI-2.7*	AEA			-40 to 85	8 Ld MSOP
X9315UMIZ-2.7* (Note)	AJG			-40 to 85	8 Ld MSOP (Pb-free)
X9315UP-2.7				0 to 70	8 Ld PDIP
X9315UPI-2.7				-40 to 85	8 Ld PDIP
X9315US-2.7*	X9315U F			0 to 70	8 Ld SOIC
X9315USZ-2.7* (Note)	X9315U Z F			0 to 70	8 Ld SOIC (Pb-free)
X9315USI-2.7*	X9315U G			-40 to 85	8 Ld SOIC
X9315USIZ-2.7* (Note)	X9315U Z G			-40 to 85	8 Ld SOIC (Pb-free)
X9315TM-2.7*	AEI		100	0 to 70	8 Ld MSOP
X9315TMZ-2.7* (Note)	DDP			0 to 70	8 Ld MSOP (Pb-free)
X9315TMI-2.7*	ADY			-40 to 85	8 Ld MSOP
X9315TMIZ-2.7* (Note)	DDM			-40 to 85	8 Ld MSOP (Pb-free)
X9315TS-2.7*	X9315T F			0 to 70	8 Ld SOIC
X9315TSZ-2.7* (Note)	X9315T Z F			0 to 70	8 Ld SOIC (Pb-free)
X9315TSI-2.7*	X9315T G			-40 to 85	8 Ld SOIC
X9315TSIZ-2.7* (Note)	X9315T Z G			-40 to 85	8 Ld SOIC (Pb-free)

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Add "T1" suffix for tape and reel.

Pin Descriptions

R_H/V_H and R_L/V_L

The high (R_H/V_H) and low (R_L/V_L) terminals of the X9315 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of R_L/V_L and R_H/V_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input, and not the voltage potential on the terminal.

R_W/V_W

R_W/V_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200Ω at V_{CC} = 5V.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

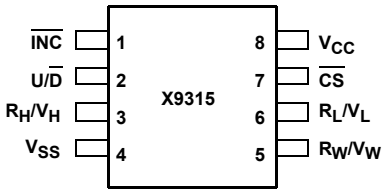
The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9315 will be placed in the low power standby mode until the device is selected once again.

Pin Configuration

DIP/SOIC/MSOP



Pin Names

SYMBOL	DESCRIPTION
R_H/V_H	High terminal
R_W/V_W	Wiper terminal
R_L/V_L	Low terminal
V_{SS}	Ground
V_{CC}	Supply voltage
U/$\overline{D}$	Up/Down control input

Pin Names

SYMBOL	DESCRIPTION
INC	Increment control input
CS	Chip Select control input

Principles of Operation

There are three sections of the X9315: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} (INC to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a five bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9315, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until

changed by the system or until a power-up/down cycle recalled the previously stored data.

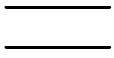
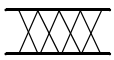
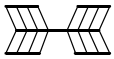
This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc...

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

CS	INC	U/$\overline{D}$	MODE
L		H	Wiper Up
L		L	Wiper Down
	H	X	Store Wiper Position
H	X	X	Standby Current
	L	X	No Store, Return to Standby

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, V_H, V_L and
V_{CC} with respect to V_{SS} . . . . . -1V to +7V
$\Delta V = |V_H - V_L|$ 5V
Lead temperature (soldering 10 seconds) . . . . . .300°C
I_W (10 seconds) . . . . . .±7.5mA

Recommended Operating Conditions

Temperature (Commercial) . . . . . 0°C to +70°C
Temperature (Industrial) . . . . . .-40°C to +85°C
Supply Voltage (V_{CC}) (Note 4) Limits
X9315 . . . . . 5V ± 10%
X9315-2.7 . . . . . 2.7V to 5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Potentiometer Characteristics (Over recommended operating conditions unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	LIMITS			
			MIN	TYP	MAX.	UNIT
	End to end resistance tolerance				±20	%
V_{VH}	V_H terminal voltage		0		V_{CC}	V
V_{VL}	V_L terminal voltage		0		V_{CC}	V
	Power rating	$R_{TOTAL} \geq 10k\Omega$			10	mW
R_W	Wiper resistance	I_W = 1mA, V_{CC} = 5V		200	400	Ω
R_W	Wiper resistance	I_W = 1mA, V_{CC} = 2.7V		400	1000	Ω
I_W	Wiper current				±3.75	mA
	Noise	Ref: 1kHz		-120		dBV
	Resolution			3		%
	Absolute linearity(1)	$V_{w(n)(actual)} - V_{w(n)(expected)}$			±1	MI(3)
	Relative linearity(2)	$V_{w(n+1)} - [V_{w(n)} + MI]$			±0.2	MI(3)
	R_{TOTAL} temperature coefficient			±300		ppm/°C
	Ratiometric temperature coefficient				±20	ppm/°C
$C_H/C_L/C_W$	Potentiometer capacitances	See circuit #3		10/10/25		pF

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{w(n)}$(actual) - $V_{w(n)}$(expected)) = ±1 MI Maximum.
(2) Relative linearity is a measure of the error in step size between taps = $R_{W(n+1)} - [R_{w(n)} + MI] = \pm 0.2$ MI.
(3) 1 MI = Minimum Increment = $R_{TOT}/31$.
(4) Typical values are for T_A = 25°C and nominal supply voltage.
(5) This parameter is periodically sampled and not 100% tested

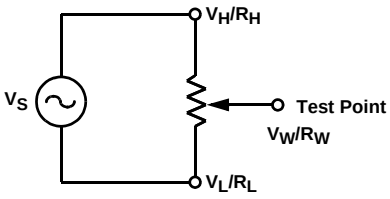
DC Electrical Specifications (Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP(4)	MAX	
I_{CC1}	V_{CC} active current (Increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V @ max. t_{CYC}			50	µA
I_{CC2}	V_{CC} active current (Store) (EEPROM Store)	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IH} @ max. t_{WR}			400	µA
I_{SB}	Standby supply current	$\overline{CS}$ = V_{CC} - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} - 0.3V			1	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input leakage current	V_{IN} = V_{SS} to V_{CC}			±10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage		-0.5		V_{CC} x 0.1	V
C_{IN}(5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz			10	pF

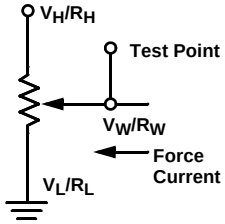
Endurance and Data Retention

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

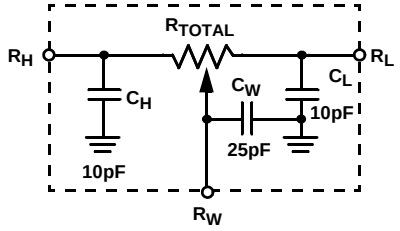
Test Circuit #1



Test Circuit #2



Circuit #3 SPICE Macro Model



AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

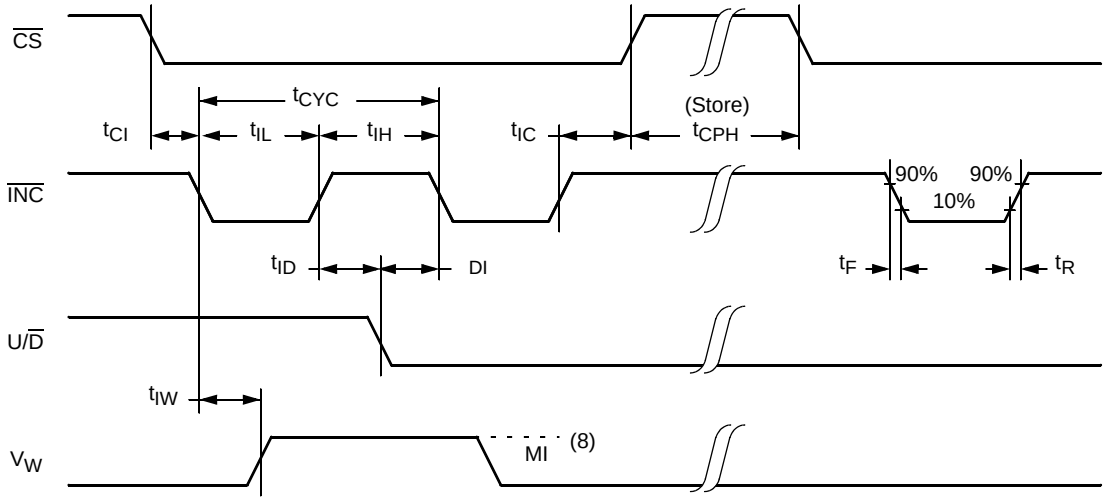
AC Electrical Specifications (Over recommended operating conditions unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP(6)	MAX	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ setup	2.9			µs
t_{IL}	$\overline{INC}$ LOW period	1			µs
t_{IH}	$\overline{INC}$ HIGH period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect time (NO STORE)	100			ns
t_{CPH}	$\overline{CS}$ Deselect time (STORE)	10			ms
t_{IW}	$\overline{INC}$ to Vw change		1	5	µs
t_{CYC}	$\overline{INC}$ cycle time	4			µs
t_R, t_F(7)	$\overline{INC}$ input rise and fall time			500	µs
t_{PU}(7)	Power-up to wiper stable			5	µs
$t_R V_{CC}$(7)	V_{CC} power-up rate	0.2		50	V/ms
t_{WR}	Store cycle		5	10	ms

Power-up and Down Requirements

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., $V_{CC} \geq V_H$, V_L, V_W. The V_{CC} ramp rate spec is always in effect.

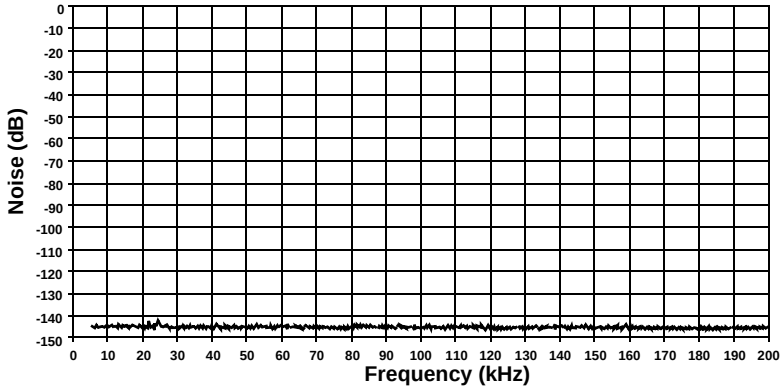
AC Timing



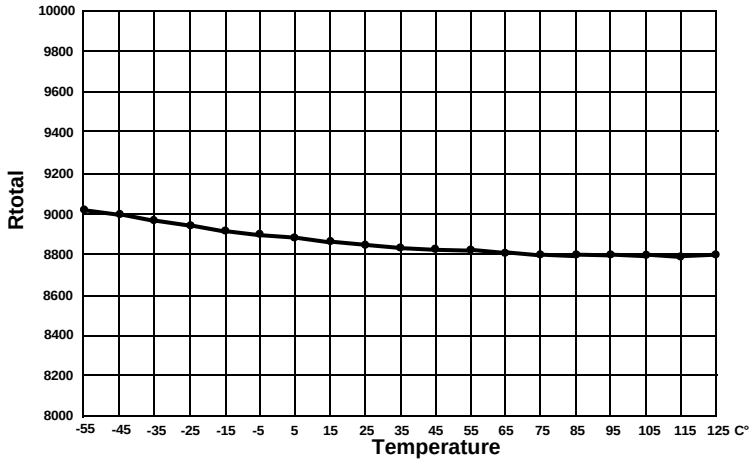
Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) This parameter is not 100% tested.
(8) MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

Performance Characteristics (Typical)

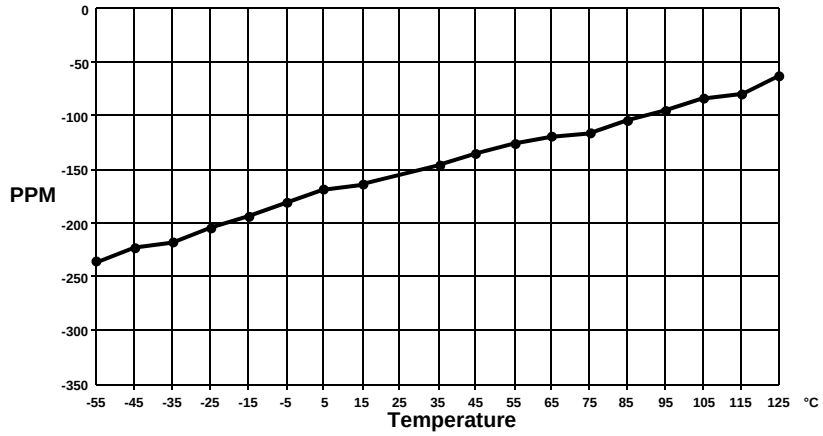
Typical Noise



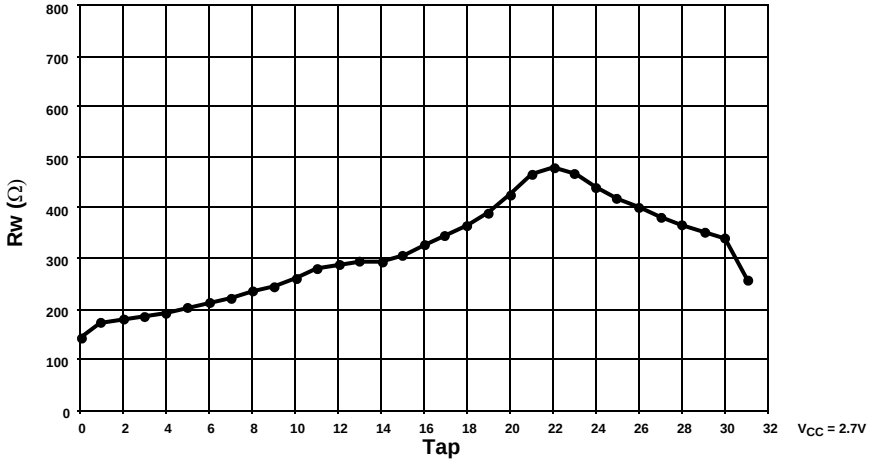
Typical Rtotal vs. Temperature



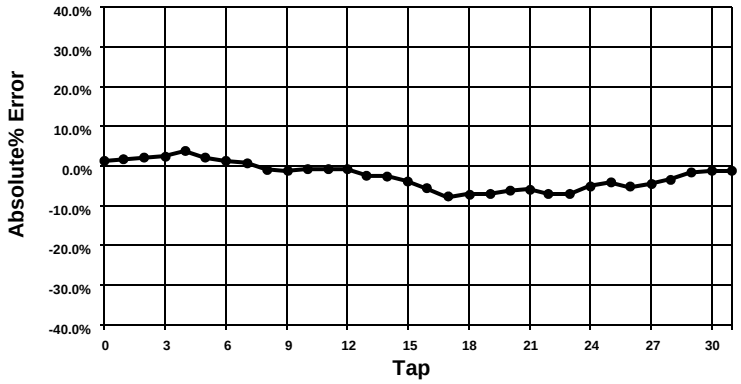
Typical Total Resistance Temperature Coefficient



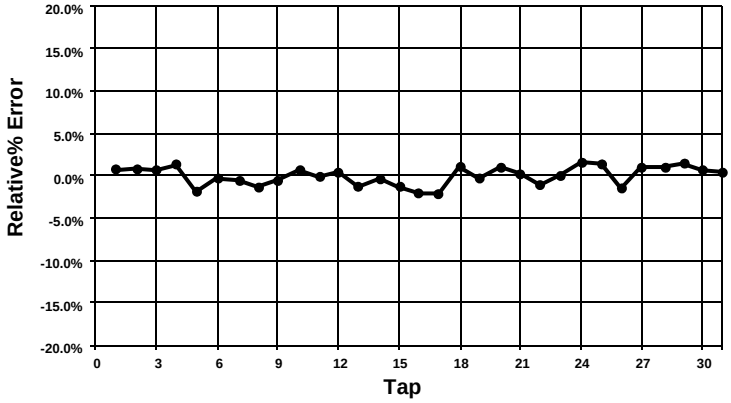
Typical Wiper Resistance



Typical Absolute% Error per Tap Position



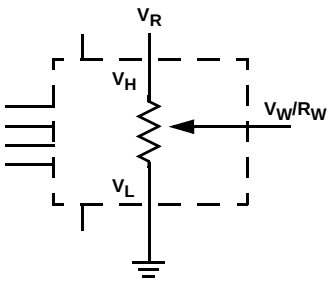
Typical Relative% Error per Tap Position



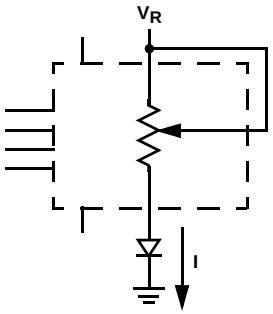
Applications Information

Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers



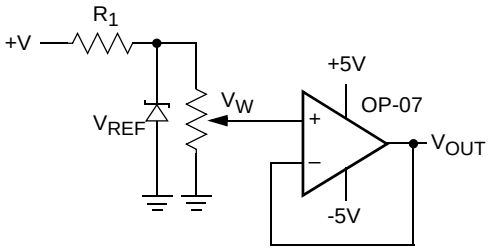
Three terminal potentiometer;
variable voltage divider



Two terminal variable resistor;
variable current

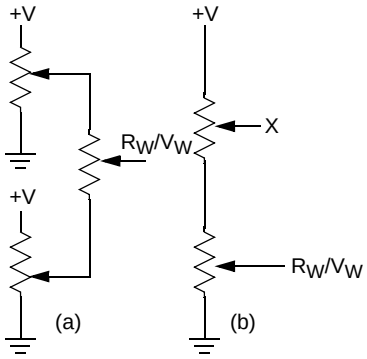
Basic Circuits

Buffered Reference Voltage

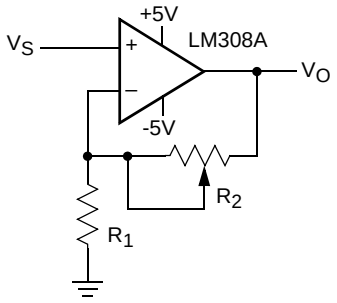


$V_{OUT} = V_W/R_W$

Cascading Techniques

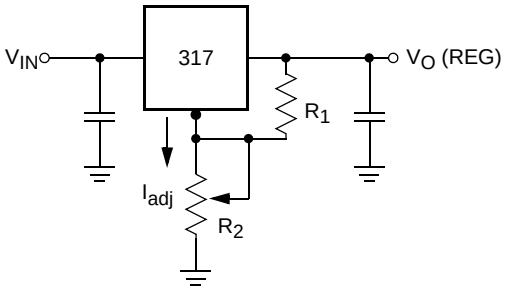


Noninverting Amplifier



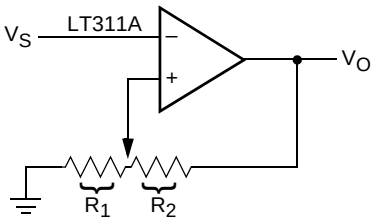
$V_O = (1 + R_2/R_1)V_S$

Voltage Regulator



V_O (REG) = 1.25V (1 + R_2/R_1) + I_{adj} R_2

Comparator with Hysteresis

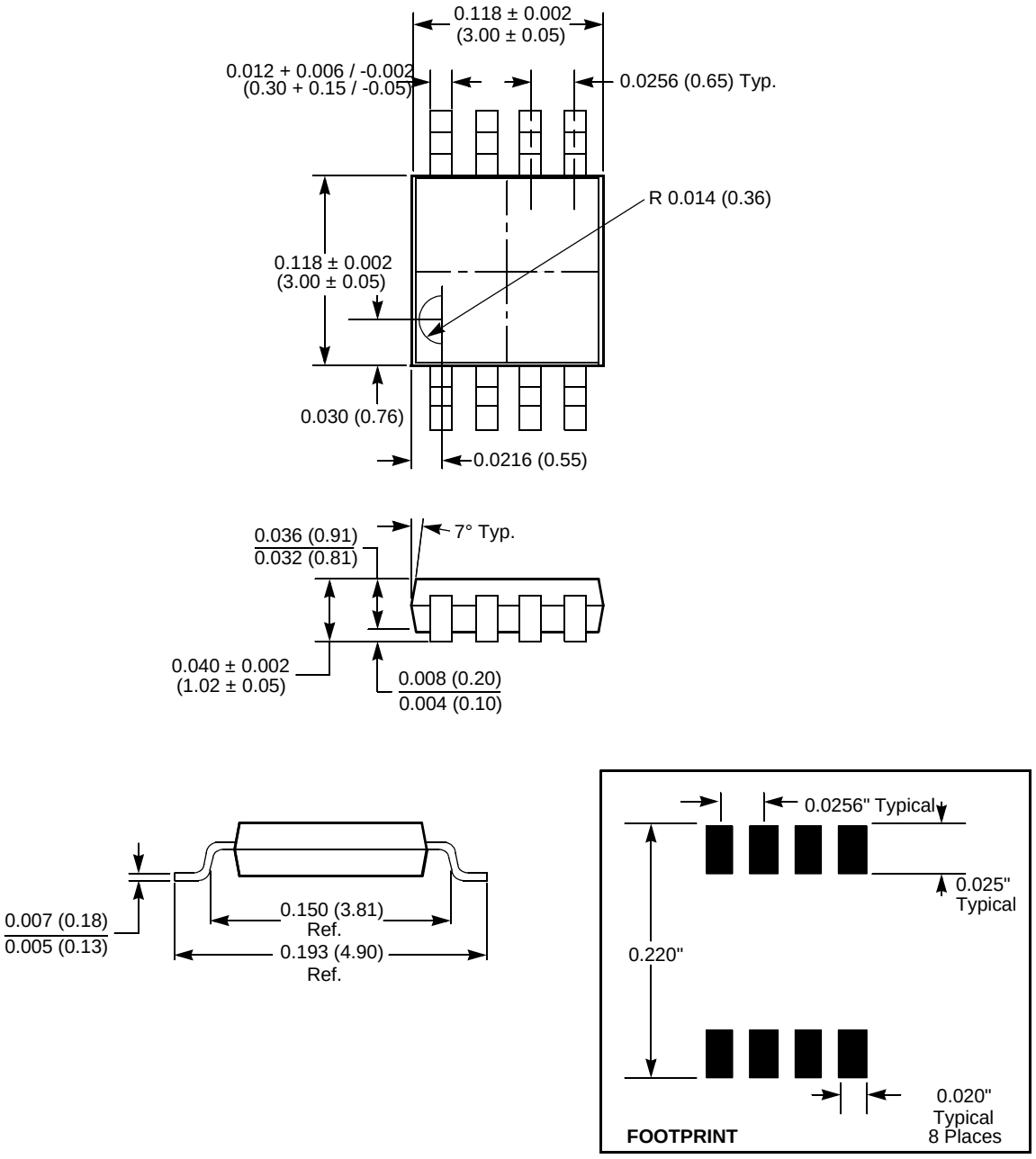


$V_{UL} = \{R_1/(R_1 + R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1 + R_2)\}\ V_O(min)$

(for additional circuits see AN115)

Packaging Information

8-Lead Miniature Small Outline Gull Wing Package Type M

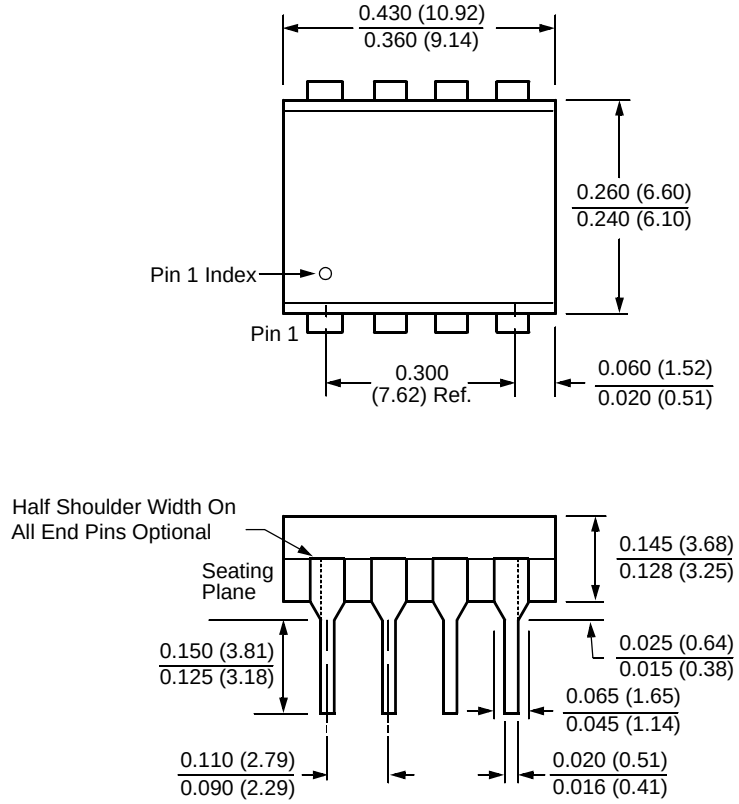


NOTE:

1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

Packaging Information

8-Lead Plastic Dual In-Line Package Type P

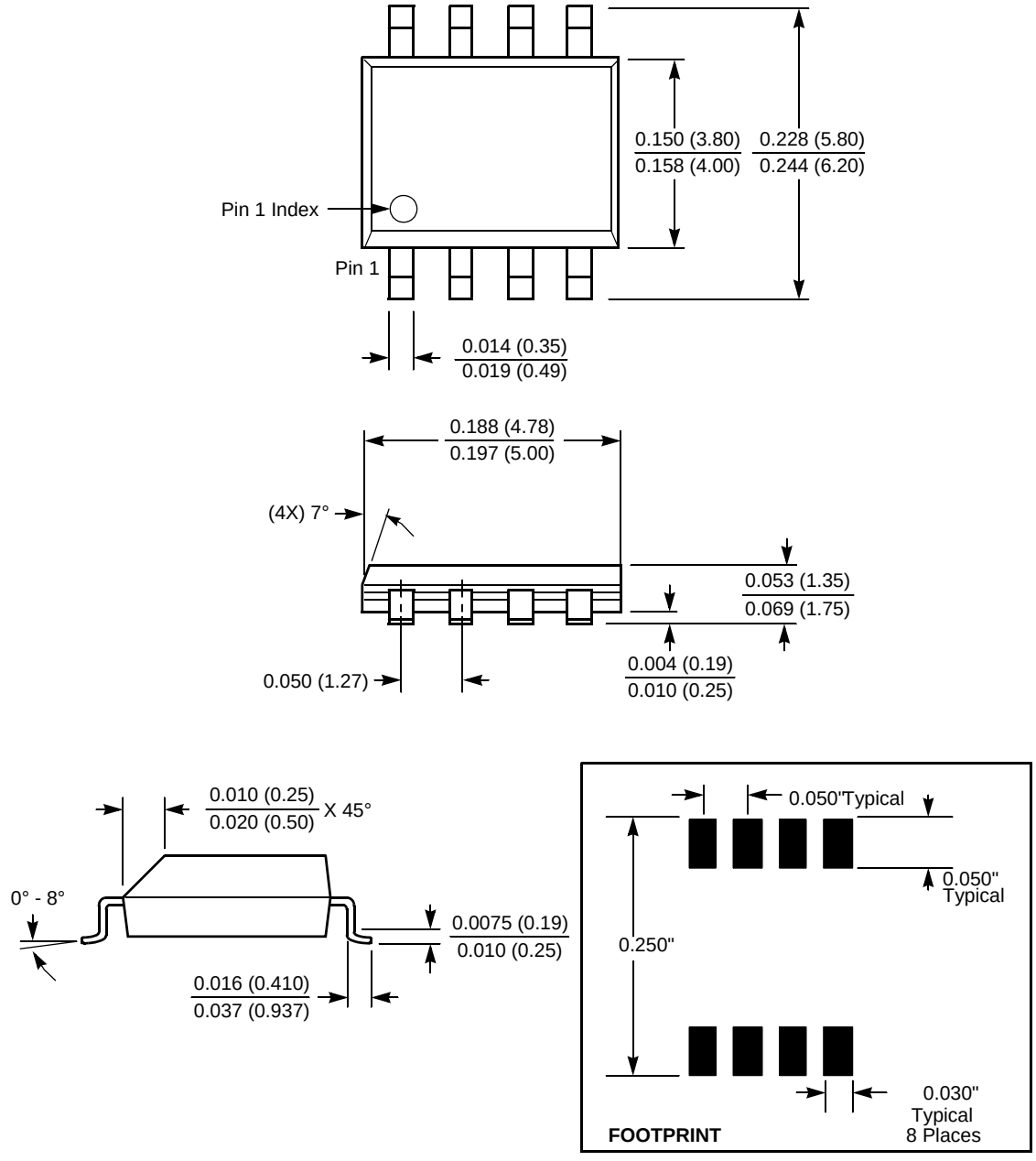


NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

Packaging Information

8-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality