

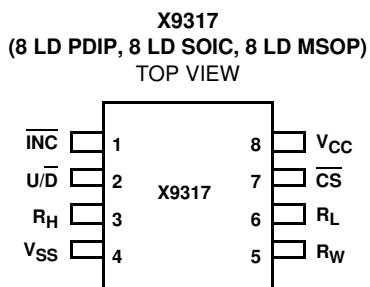
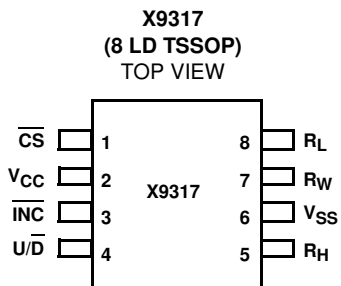
**Digitally Controlled Potentiometer (XDCP™)**

The Intersil X9317 is a digitally controlled potentiometer (XDCP™). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the CS, U/D, and INC inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer for voltage control or as a two-terminal variable resistor for current control in a wide variety of applications.

**Pinouts**



**Features**

- Solid-State Potentiometer
- 3-Wire Serial Up/Down Interface
- 100 Wiper Tap Points
  - Wiper Position Stored in Nonvolatile Memory and Recalled on Power-up
- 99 Resistive Elements
  - Temperature Compensated
  - End-to-end Resistance Range ±20%
- Low Power CMOS
  - V<sub>CC</sub> = 2.7V to 5.5V, and 5V ±10%
  - Standby Current <5μA
- High Reliability
  - Endurance, 100,000 Data Changes per Bit
  - Register Data Retention, 100 years
- R<sub>TOTAL</sub> Values = 1kΩ, 10kΩ, 50kΩ, 100kΩ
- Packages
  - 8 Ld SOIC, PDIP, TSSOP, and MSOP
- Pb-Free Available (RoHS Compliant)

**Applications**

- LCD Bias Control
- DC Bias Adjustment
- Gain and Offset Trim
- Laser Diode Bias Control
- Voltage Regulator Output Control

## Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V <sub>CC</sub> LIMITS (V)	R <sub>TOTAL</sub> (k $\Omega$ )	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #		
X9317ZM8Z	DDA	5 $\pm$ 10%	1	0 to +70	8 Ld MSOP	M8.118		
X9317ZM8IZ	DCY			-40 to +85	8 Ld MSOP	M8.118		
X9317ZS8Z	X9317Z Z			0 to +70	8 Ld SOIC	M8.15E		
X9317ZS8IZ	X9317Z Z I			-40 to +85	8 Ld SOIC	M8.15E		
X9317ZV8Z	9317Z Z			0 to +70	8 Ld TSSOP	M8.173		
X9317ZV8IZ	9317Z IZ			-40 to +85	8 Ld TSSOP	M8.173		
X9317WM8Z	DCW			10	0 to +70	8 Ld MSOP	M8.118	
X9317WM8IZ	DCT				-40 to +85	8 Ld MSOP	M8.118	
X9317WS8Z	X9317W Z		0 to +70		8 Ld SOIC	M8.15E		
X9317WS8IZ	X9317W ZI		-40 to +85		8 Ld SOIC	M8.15E		
X9317WV8Z	9317W Z		0 to +70		8 Ld TSSOP	M8.173		
X9317WV8IZ	9317W IZ		-40 to +85		8 Ld TSSOP	M8.173		
X9317UM8Z	DCS		0 to +70		8 Ld MSOP	M8.118		
X9317UM8IZ	DCR		-40 to +85		8 Ld MSOP	M8.118		
X9317US8Z	X9317U Z		50	0 to +70	8 Ld SOIC	M8.15E		
X9317US8IZ	X9317U ZI			-40 to +85	8 Ld SOIC	M8.15E		
X9317UV8Z	9317U Z			0 to +70	8 Ld TSSOP	M8.173		
X9317UV8IZ	9317U IZ			-40 to +85	8 Ld TSSOP	M8.173		
X9317TM8Z	DCN			100	0 to +70	8 Ld MSOP	M8.118	
X9317TM8IZ	DCL				-40 to +85	8 Ld MSOP	M8.118	
X9317TS8Z	X9317T Z				0 to +70	8 Ld SOIC	M8.15E	
X9317TS8IZ	X9317T ZI				-40 to +85	8 Ld SOIC	M8.15E	
X9317TV8Z	9317T Z		0 to +70		8 Ld TSSOP	M8.173		
X9317TV8IZ	9317T IZ		-40 to +85		8 Ld TSSOP	M8.173		
X9317ZM8Z-2.7	AOA		2.7 to 5.5		1	0 to +70	8 Ld MSOP	M8.118
X9317ZM8IZ-2.7	DCZ					-40 to +85	8 Ld MSOP	M8.118
X9317ZS8Z-2.7	X9317Z ZF			0 to +70		8 Ld SOIC	M8.15E	
X9317ZS8IZ-2.7	X9317Z ZG			-40 to +85		8 Ld SOIC	M8.15E	
X9317ZV8Z-2.7	9317Z FZ	0 to +70		8 Ld TSSOP		M8.173		
X9317ZV8IZ-2.7	9317Z GZ	-40 to +85		8 Ld TSSOP		M8.173		
X9317WM8Z-2.7	DCX	10		0 to +70		8 Ld MSOP	M8.118	
X9317WM8IZ-2.7	DCU			-40 to +85		8 Ld MSOP	M8.118	
X9317WS8Z-2.7	X9317W ZF			0 to +70	8 Ld SOIC	M8.15E		
X9317WS8IZ-2.7	X9317W ZG			-40 to +85	8 Ld SOIC	M8.15E		
X9317WV8Z-2.7	9317W FZ			0 to +70	8 Ld TSSOP	M8.173		
X9317WV8IZ-2.7	AKZ			-40 to +85	8 Ld TSSOP	M8.173		
X9317UM8Z-2.7	AOB			0 to +70	8 Ld MSOP	M8.118		
X9317UM8IZ-2.7	AOH			-40 to +85	8 Ld MSOP	M8.118		
X9317US8Z-2.7	X9317U ZF	50		0 to +70	8 Ld SOIC	M8.15E		
X9317US8IZ-2.7	X9317U ZG			-40 to +85	8 Ld SOIC	M8.15E		
X9317UV8Z-2.7	9317U FZ			0 to +70	8 Ld TSSOP	M8.173		
X9317UV8IZ-2.7	9317U GZ			-40 to +85	8 Ld TSSOP	M8.173		

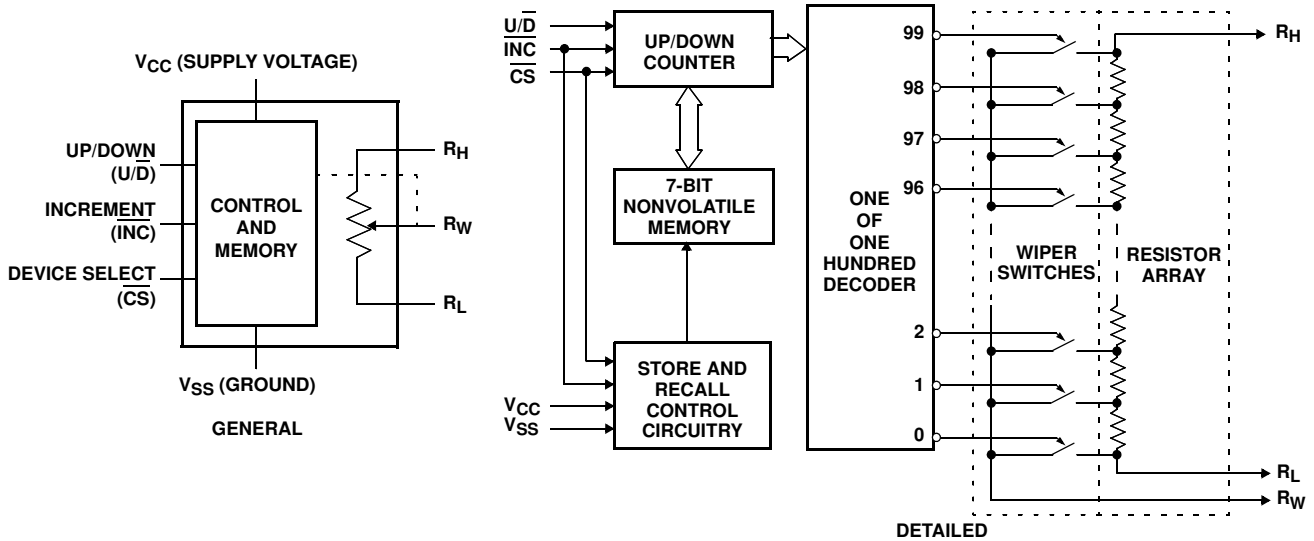
**Ordering Information** (Continued)

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V <sub>CC</sub> LIMITS (V)	R <sub>TOTAL</sub> (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #
X9317TM8Z-2.7	DCP	2.7 to 5.5	100	0 to +70	8 Ld MSOP	M8.118
X9317TM8IZ-2.7	DCM			-40 to +85	8 Ld MSOP	M8.118
X9317TS8Z-2.7	X9317T ZF			0 to +70	8 Ld SOIC	M8.15E
X9317TS8IZ-2.7	X9317T ZG			-40 to +85	8 Ld SOIC	M8.15E
X9317TV8Z-2.7	9317T FZ			0 to +70	8 Ld TSSOP	M8.173
X9317TV8IZ-2.7	9317T GZ			-40 to +85	8 Ld TSSOP	M8.173

NOTES:

1. Add "-T1" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [X9317](#). For more information on MSL please see tech brief [TB363](#).

**Block Diagram**



**Pin Descriptions**

PDIP/SOIC/MSOP	TSSOP	SYMBOL	BRIEF DESCRIPTION
1	3	$\overline{INC}$	<b>Increment</b> Toggling $\overline{INC}$ while $\overline{CS}$ is low moves the wiper either up or down.
2	4	$U/\overline{D}$	<b>Up/Down</b> The $U/\overline{D}$ input controls the direction of the wiper movement.
3	5	R <sub>H</sub>	The high terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
4	6	V <sub>SS</sub>	<b>Ground</b>
5	7	R <sub>W</sub>	The wiper terminal is equivalent to the movable terminal of a mechanical potentiometer.
6	8	R <sub>L</sub>	The low terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
7	1	$\overline{CS}$	<b>Chip Select</b> The device is selected when the $\overline{CS}$ input is LOW, and de-selected when $\overline{CS}$ is high.
8	2	V <sub>CC</sub>	<b>Supply Voltage</b>

**Absolute Maximum Ratings**

$I_W$  (10s) ..... ±8.8mA  
 $R_H$ ,  $R_W$ ,  $R_L$  to Ground ..... +6V  
 Voltage on CS, INC, U/D and  $V_{CC}$   
 with Respect to  $V_{SS}$  ..... -1V to +7V

**Thermal Information**

Junction Temperature Under Bias ..... -65°C to +135°C  
 Storage Temperature ..... -65°C to +150°C  
 Pb-free reflow profile ..... see link below  
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**Potentiometer Specifications**  $V_{CC}$  = Full Range,  $T_A$  = Full Operating Temperature Range, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN (Note 11)	TYP (Note 7)	MAX (Note 11)	UNIT
$R_{TOTAL}$	End-to-end Resistance Tolerance	See "Ordering Information" beginning on page 2 for values	-20		+20	%
$V_{RH/RL}$	$R_H/R_L$ Terminal Voltage	$V_{SS} = 0V$	$V_{SS}$		$V_{CC}$	V
	Power Rating	$R_{TOTAL} \geq 10k\Omega$			10	mW
		$R_{TOTAL} = 1k\Omega$			25	mW
$R_W$	Wiper Resistance	$I_W = [V(R_H) - V(R_L)] / R_{TOTAL}$ , $V_{CC} = 5V$		200	400	$\Omega$
		$I_W = [V(R_H) - V(R_L)] / R_{TOTAL}$ , $V_{CC} = 2.7V$		400	1000	$\Omega$
$I_W$	Wiper Current (Note 8)	See "Test Circuit" on page 5	-4.4		+4.4	mA
	Noise (Note 10)	Ref: 1kHz		-120		dBV
	Resolution			1		%
	Absolute Linearity (Note 4)	$V(R_H) = V_{CC}$ , $V(R_L) = 0V$	-1		+1	MI (Note 6)
	Relative Linearity (Note 5)	$V(R_H) = V_{CC}$ , $V(R_L) = 0V$	-0.2		+0.2	MI (Note 6)
	$R_{TOTAL}$ Temperature Coefficient (Note 8)	$V(R_H) = V_{CC}$ , $V(R_L) = 0V$		±300		ppm/°C
	Ratiometric Temperature Coefficient (Notes 8, 9)			±20		ppm/°C
$C_H/C_L/C_W$ (Note 8)	Potentiometer Capacitances	See "Equivalent Circuit" on page 5		10/10/25		pF
$V_{CC}$	Supply Voltage	X9317	4.5		5.5	V
		X9317-2.7	2.7		5.5	V

**DC Electrical Specifications**  $V_{CC} = 5V \pm 10\%$ ,  $T_A$  = Full Operating Temperature Range, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP (Note 7)	MAX (Note 11)	UNIT
$I_{CC1}$	$V_{CC}$ Active Current (Increment)	$\overline{CS} = V_{IL}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = V_{IL}/V_{IH}$ @ min. $t_{CYC}$ $R_L$ , $R_H$ , $R_W$ not connected			80	$\mu A$
$I_{CC2}$	$V_{CC}$ Active Current (Store) (non-volatile write)	$\overline{CS} = V_{IH}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = V_{IL}$ or $V_{IH}$ . $R_L$ , $R_H$ , $R_W$ not connected			400	$\mu A$
$I_{SB}$	Standby Supply Current	$\overline{CS} \geq V_{IH}$ , $U/\overline{D}$ and $\overline{INC} = V_{IL}$ $R_L$ , $R_H$ , $R_W$ not connected			5	$\mu A$
$I_{LI}$	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input Leakage Current	$V_{IN} = V_{SS}$ to $V_{CC}$	-10		+10	$\mu A$
$V_{IH}$	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input HIGH Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
$V_{IL}$	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input LOW Voltage		-0.5		$V_{CC} \times 0.1$	V
$C_{IN}$ (Note 8)	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input Capacitance	$V_{CC} = 5V$ , $V_{IN} = V_{SS}$ , $T_A = +25^\circ C$ , $f = 1MHz$		10		pF

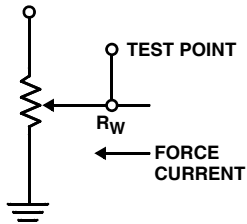
**Endurance and Data Retention**  $V_{CC} = 5V \pm 10\%$ ,  $T_A =$  Full Operating Temperature Range.

PARAMETER	MIN	UNIT
Minimum Endurance	100,000	Data changes per bit
Data Retention	100	Years

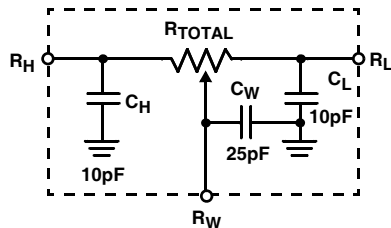
NOTES:

- Absolute linearity is utilized to determine actual wiper voltage versus expected voltage =  $[V(R_{W(n)}(actual)) - V(R_{W(n)}(expected))] / MI$   
 $V(R_{W(n)}(expected)) = n(V(R_H) - V(R_L)) / 99 + V(R_L)$ , with n from 0 to 99.
- Relative linearity is a measure of the error in step size between taps =  $[V(R_{W(n+1)}) - (V(R_{W(n)}) - MI)] / MI$ .
- 1 MI = Minimum Increment =  $[V(R_H) - V(R_L)] / 99$ .
- Typical values are for  $T_A = +25^\circ C$  and nominal supply voltage.
- This parameter is not 100% tested.
- Ratiometric temperature coefficient =  $(V(R_{W(n)})_{T1} - V(R_{W(n)})_{T2}) / [V(R_{W(n)})_{T1} (T1 - T2) \times 10^6]$ , with T1 and T2 being 2 temperatures, and n from 0 to 99.
- Measured with wiper at tap position 99,  $R_L$  grounded, using test circuit.
- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

**Test Circuit**



**Equivalent Circuit**



**AC Conditions of Test**

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

**AC Electrical Specifications**  $V_{CC} = 5V \pm 10\%$ ,  $T_A =$  Full Operating Temperature Range, unless otherwise stated.

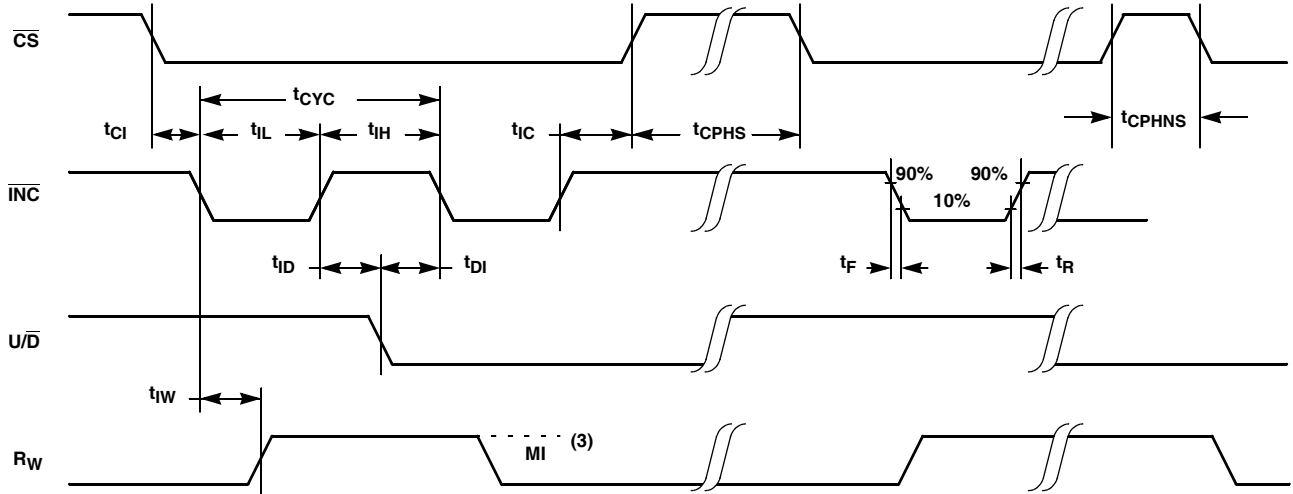
SYMBOL	PARAMETER	MIN (Note 11)	TYP (Note 7)	MAX (Note 11)	UNIT
$t_{CI}$	$\overline{CS}$ to $\overline{INC}$ Setup	50			ns
$t_{ID}$ (Note 8)	$\overline{INC}$ HIGH to $\overline{U/D}$ Change	100			ns
$t_{DI}$ (Note 8)	$\overline{U/D}$ to $\overline{INC}$ Setup	1			$\mu s$
$t_{IL}$	$\overline{INC}$ LOW Period	960			ns
$t_{IH}$	$\overline{INC}$ HIGH Period	960			ns
$t_{IC}$	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			$\mu s$
$t_{CPHS}$	$\overline{CS}$ Deselect Time (STORE)	10			ms
$t_{CPHNS}$ (Note 8)	$\overline{CS}$ Deselect Time (NO STORE)	100			ns
$t_{IW}$	$\overline{INC}$ to $R_W$ Change		1	5	$\mu s$
$t_{CYC}$	$\overline{INC}$ Cycle Time	2			$\mu s$
$t_R, t_F$ (Note 8)	$\overline{INC}$ Input Rise and Fall Time			500	$\mu s$
$t_{PU}$ (Note 8)	Power-up to Wiper Stable			5	$\mu s$
$t_R V_{CC}$ (Note 8)	$V_{CC}$ Power-up Rate	0.2		50	V/ms
$t_{WR}$	Store Cycle		5	10	ms

**Power-up and Down Requirements**

The recommended power-up sequence is to apply  $V_{CC}/V_{SS}$  first, then the potentiometer voltages. During power-up, the data sheet parameters for the DCP do not fully apply until

1 ms after  $V_{CC}$  reaches its final value. The  $V_{CC}$  ramp spec is always in effect. In order to prevent unwanted tap position changes, or an inadvertent store, bring the  $\overline{CS}$  and  $\overline{INC}$  high before or concurrently with the  $V_{CC}$  pin on power-up.

**AC Timing**



**Typical Performance Characteristic**

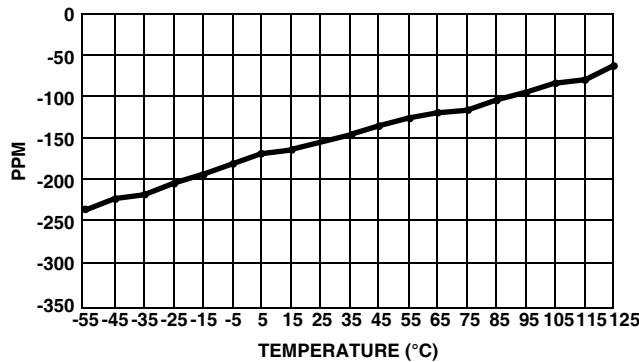


FIGURE 1. TYPICAL TOTAL RESISTANCE TEMPERATURE COEFFICIENT

## Pin Descriptions

### R<sub>H</sub> AND R<sub>L</sub>

The high (R<sub>H</sub>) and low (R<sub>L</sub>) terminals of the X9317 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R<sub>L</sub> and R<sub>H</sub> references the relative position of the terminal in relation to wiper movement direction selected by the U/ $\bar{D}$  input and not the voltage potential on the terminal.

### R<sub>W</sub>

R<sub>W</sub> is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200Ω.

### UP/DOWN (U/ $\bar{D}$ )

The U/ $\bar{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

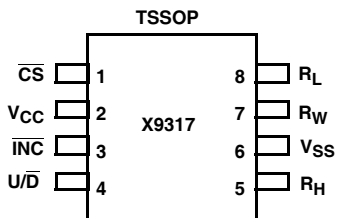
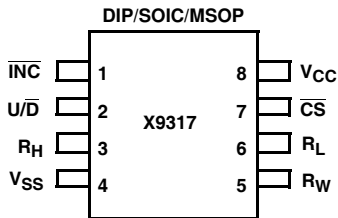
### INCREMENT ( $\bar{INC}$ )

The  $\bar{INC}$  input is negative-edge triggered. Toggling  $\bar{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/ $\bar{D}$  input.

### CHIP SELECT ( $\bar{CS}$ )

The device is selected when the  $\bar{CS}$  input is LOW. The current counter value is stored in nonvolatile memory when  $\bar{CS}$  is returned HIGH while the  $\bar{INC}$  input is also HIGH. After the store operation is complete, the X9317 will be placed in the low power standby mode until the device is selected once again.

## Pin Configuration



## Pin Names

SYMBOL	DESCRIPTION
R <sub>H</sub>	High terminal
R <sub>W</sub>	Wiper terminal
R <sub>L</sub>	Low terminal
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply voltage
U/ $\bar{D}$	Up/Down control input
$\bar{INC}$	Increment control input
$\bar{CS}$	Chip select control input

## Principles of Operation

There are three sections of the X9317: the control section, the nonvolatile memory, and the resistor array. The control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. Electronic switches at either end of the array and between each resistor provide an electrical connection to the wiper pin, R<sub>W</sub>.

The wiper acts like its mechanical equivalent and does not move beyond the first or last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t<sub>IW</sub> (INC to V<sub>W</sub> change). The R<sub>TOTAL</sub> value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

## Instructions and Programming

The  $\bar{INC}$ , U/ $\bar{D}$  and  $\bar{CS}$  inputs control the movement of the wiper along the resistor array. With  $\bar{CS}$  set LOW, the device is selected and enabled to respond to the U/ $\bar{D}$  and  $\bar{INC}$  inputs. HIGH to LOW transitions on  $\bar{INC}$  will increment or decrement (depending on the state of the U/ $\bar{D}$  input) a 7-bit counter. The output of this counter is decoded to select one of one hundred wiper positions along the resistive array.







The value of the counter is stored in nonvolatile memory whenever  $\bar{CS}$  transitions HIGH while the  $\bar{INC}$  input is also HIGH.

The system may select the X9317, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep  $\overline{\text{INC}}$  LOW while taking  $\overline{\text{CS}}$  HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalls the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of  $\text{U}/\overline{\text{D}}$  may be changed while  $\overline{\text{CS}}$  remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

### **Mode Selection**

$\overline{\text{CS}}$	$\overline{\text{INC}}$	$\text{U}/\overline{\text{D}}$	MODE
L		H	Wiper up
L		L	Wiper down
	H	X	Store wiper position to nonvolatile memory
H	X	X	Standby
	L	X	No store, return to standby
	L	H	Wiper Up (not recommended)
	L	L	Wiper Down (not recommended)

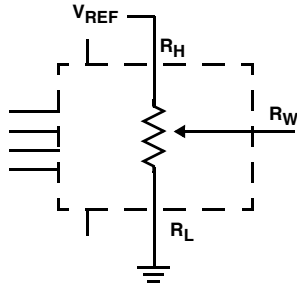
### **Applications Information**

Electronic digitally controlled (XDCCP) potentiometers provide three powerful application advantages:

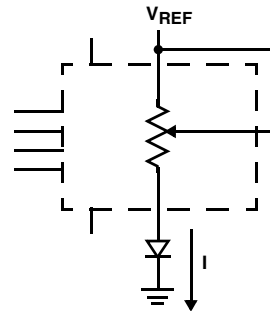
1. the variability and reliability of a solid-state potentiometer,
2. the flexibility of computer-based digital controls, and
3. the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.



Basic Configurations of Electronic Potentiometers



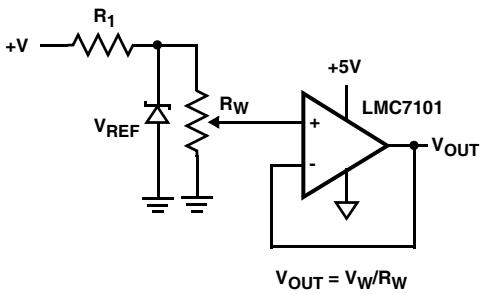
THREE TERMINAL POTENTIOMETER;  
VARIABLE VOLTAGE DIVIDER



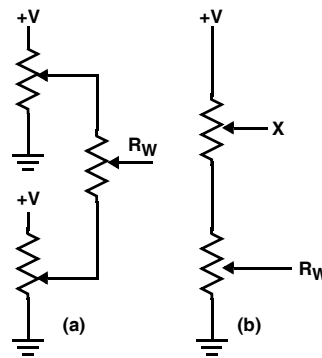
TWO TERMINAL VARIABLE RESISTOR;  
VARIABLE CURRENT

Basic Circuits

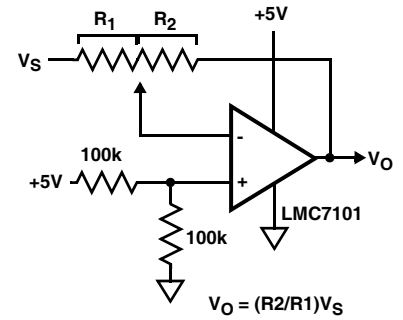
BUFFERED REFERENCE VOLTAGE



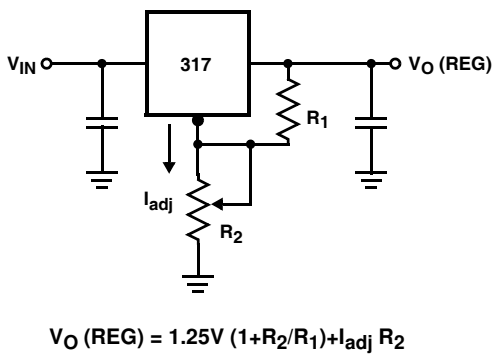
CASCADING TECHNIQUES



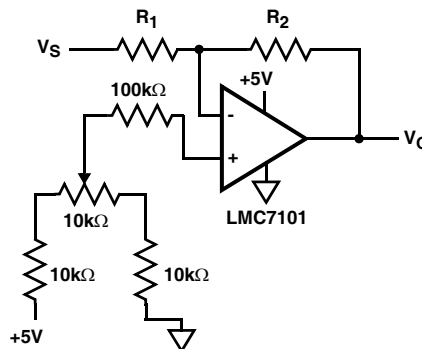
SINGLE SUPPLY INVERTING AMPLIFIER



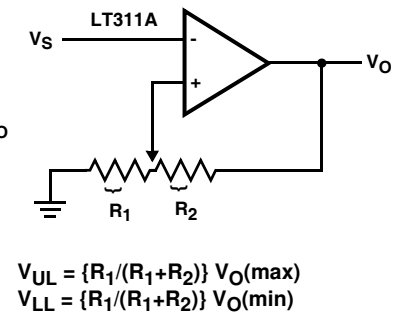
VOLTAGE REGULATOR



OFFSET VOLTAGE ADJUSTMENT



COMPARATOR WITH HYSTERESIS

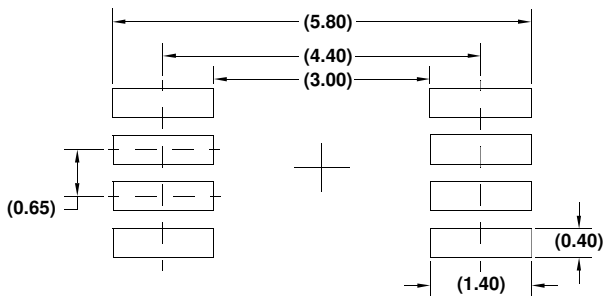
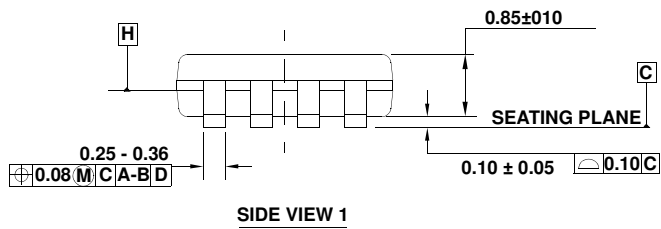
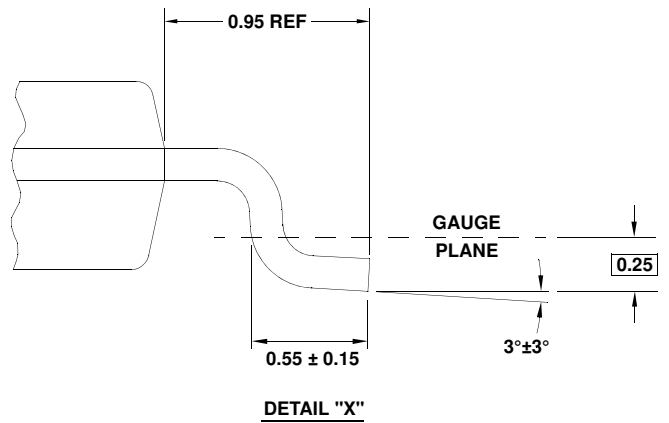
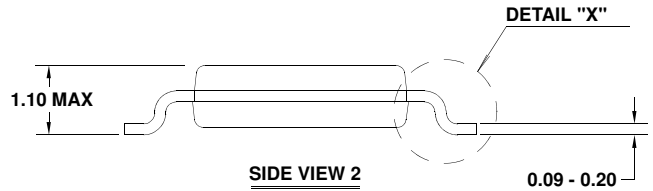
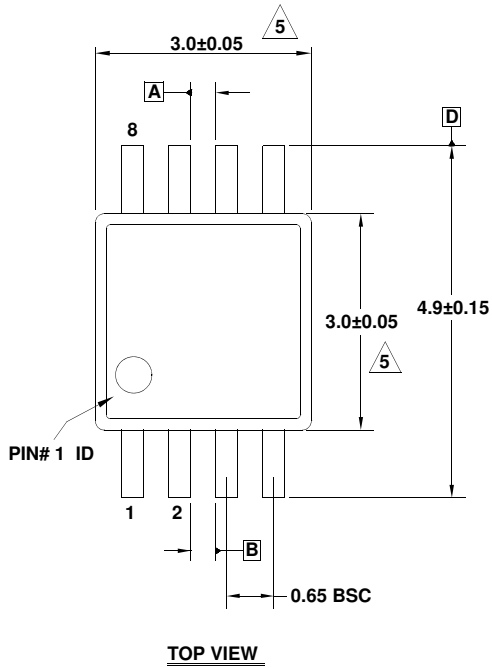


# Package Outline Drawing

## M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11



**NOTES:**

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.

5. Dimensions are measured at Datum Plane "H".

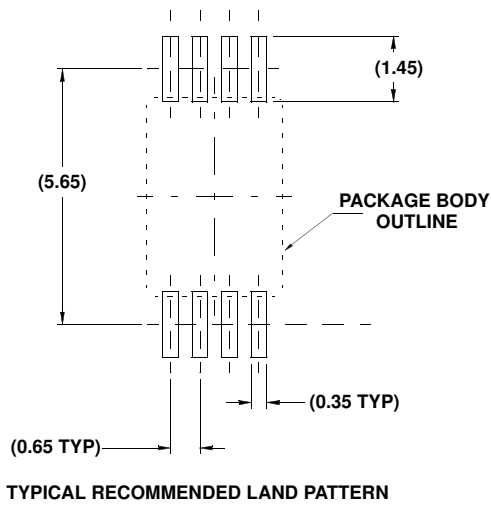
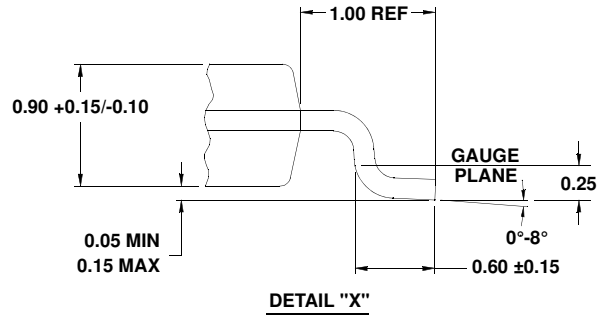
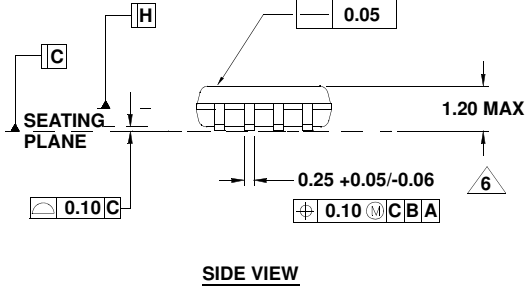
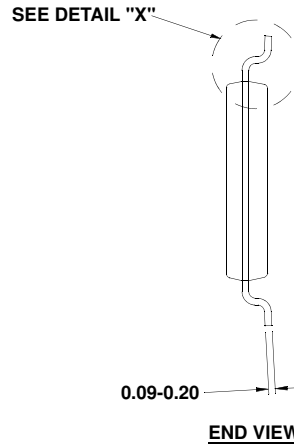
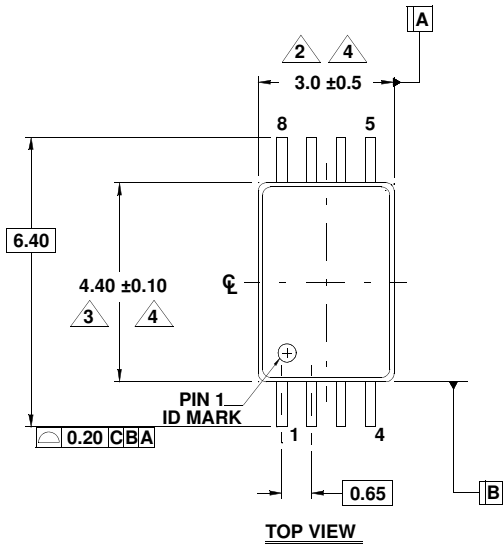
6. Dimensions in ( ) are for reference only.

# Package Outline Drawing

## M8.173

8 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

Rev 2, 01/10



**NOTES:**

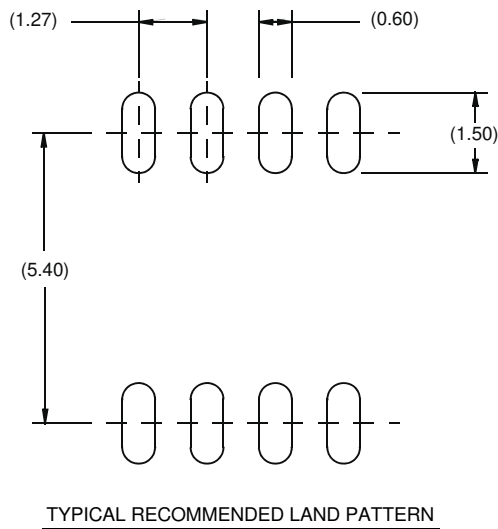
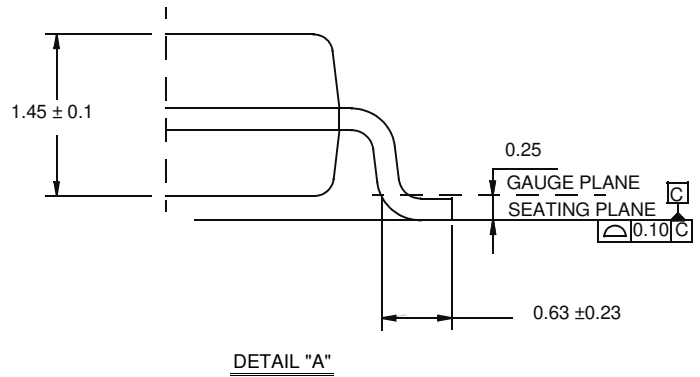
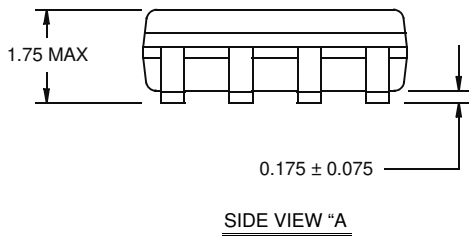
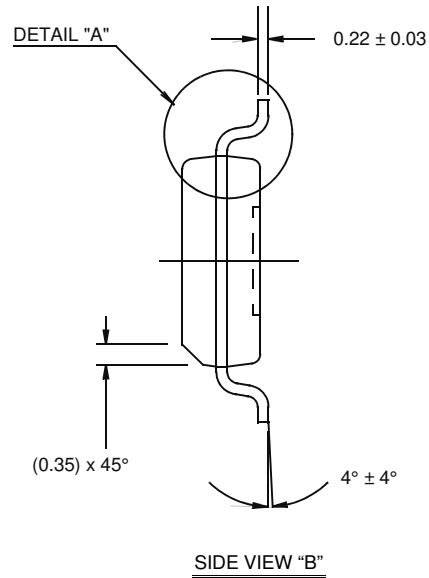
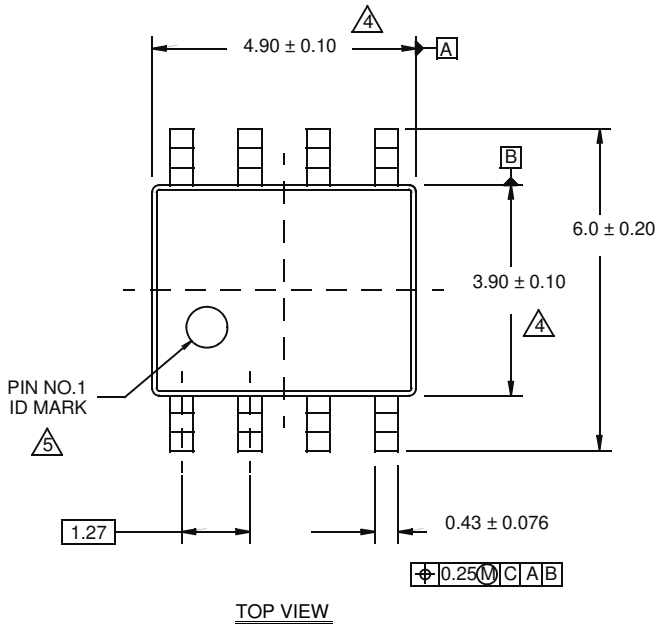
1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 per side.
4. Dimensions are measured at datum plane H.
5. Dimensioning and tolerancing per ASME Y14.5M-1994.
6. Dimension on lead width does not include dambar protrusion. Allowable protrusion shall be 0.08 mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
7. Conforms to JEDEC MO-153, variation AC. Issue E

# Package Outline Drawing

## M8.15E

### 8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

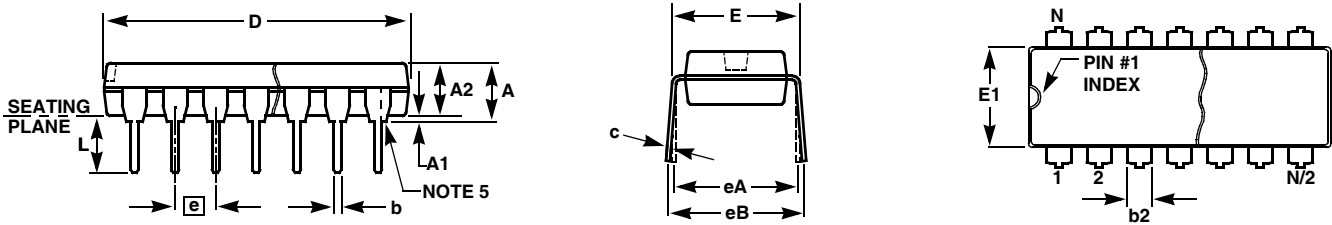
Rev 0, 08/09



NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
4. Dimension does not include interlead flash or protrusions.  
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

**Plastic Dual-In-Line Packages (PDIP)**



**MDP0031**

**PLASTIC DUAL-IN-LINE PACKAGE**

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.  
Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)