Low Noise, Low Power, 100 Taps, Digitally Controlled Potentiometer (XDCP™)

X9317

The Intersil X9317 is a digitally controlled potentiometer (XDCP™). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer for voltage control or as a two-terminal variable resistor for current control in a wide variety of applications.

Applications

- LCD bias control
- DC bias adjustment
- Gain and offset trim
- Laser diode bias control
- Voltage regulator output control

Features

- Solid-state potentiometer
- 3-wire serial up/down interface
- 100 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 99 resistive elements
  - Temperature compensated
  - End-to-end resistance range ±20%
- Low power CMOS
  - V_{CC} = 2.7V to 5.5V, and 5V ±10%
  - Standby current <5µA
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- R_{TOTAL} values = 10kΩ, 50kΩ, 100kΩ
- Packages
  - 8 Ld SOIC, TSSOP, and MSOP
- Pb-free (RoHS compliant)

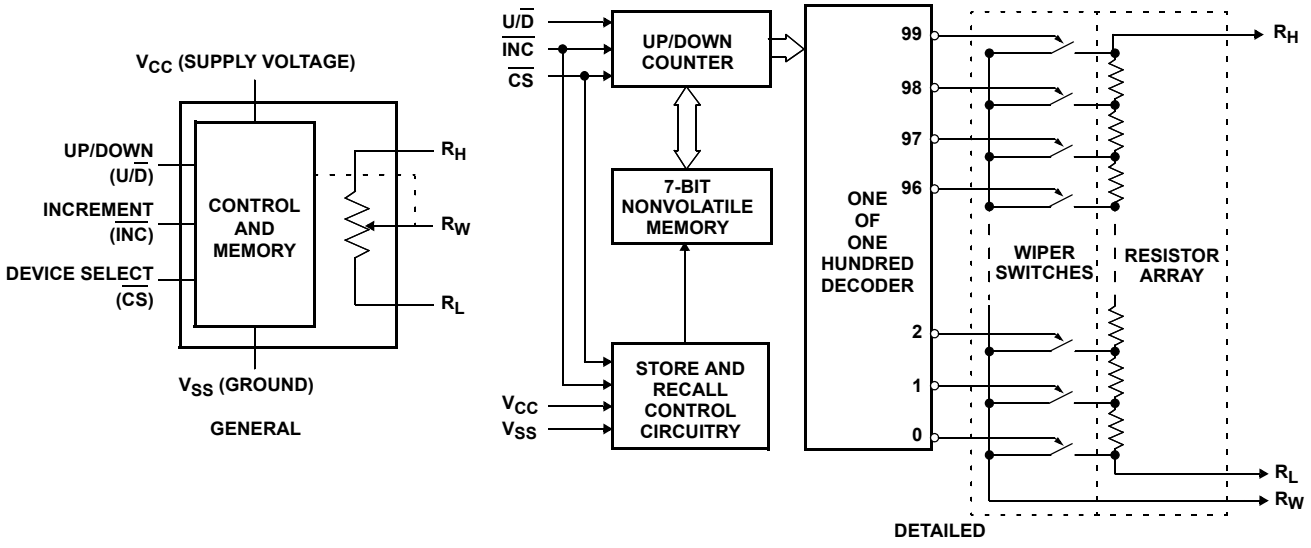


FIGURE 1. BLOCK DIAGRAM

Ordering Information

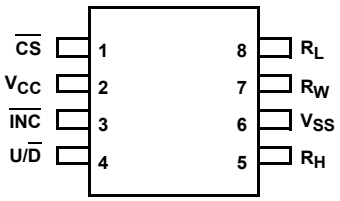
PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
X9317WM8Z	DCW	5 ±10%	10	0 to +70	8 Ld MSOP	M8.118
X9317WM8IZ	DCT			-40 to +85	8 Ld MSOP	M8.118
X9317WS8Z	X9317W Z			0 to +70	8 Ld SOIC	M8.15E
X9317WS8IZ	X9317W ZI			-40 to +85	8 Ld SOIC	M8.15E
X9317WV8Z	9317W Z			0 to +70	8 Ld TSSOP	M8.173
X9317WV8IZ	9317W IZ			-40 to +85	8 Ld TSSOP	M8.173
X9317UM8Z	DCS		50	0 to +70	8 Ld MSOP	M8.118
X9317UM8IZ	DCR			-40 to +85	8 Ld MSOP	M8.118
X9317US8Z	X9317U Z			0 to +70	8 Ld SOIC	M8.15E
X9317US8IZ	X9317U ZI			-40 to +85	8 Ld SOIC	M8.15E
X9317UV8Z	9317U Z			0 to +70	8 Ld TSSOP	M8.173
X9317UV8IZ	9317U IZ			-40 to +85	8 Ld TSSOP	M8.173
X9317TM8Z	DCN		100	0 to +70	8 Ld MSOP	M8.118
X9317TM8IZ	DCL			-40 to +85	8 Ld MSOP	M8.118
X9317TS8Z	X9317T Z			0 to +70	8 Ld SOIC	M8.15E
X9317TS8IZ	X9317T ZI			-40 to +85	8 Ld SOIC	M8.15E
X9317TV8Z	9317T Z			0 to +70	8 Ld TSSOP	M8.173
X9317TV8IZ	9317T IZ			-40 to +85	8 Ld TSSOP	M8.173
X9317WM8Z-2.7	DCX	2.7 to 5.5	10	0 to +70	8 Ld MSOP	M8.118
X9317WM8IZ-2.7	DCU			-40 to +85	8 Ld MSOP	M8.118
X9317WS8Z-2.7	X9317W ZF			0 to +70	8 Ld SOIC	M8.15E
X9317WS8IZ-2.7	X9317W ZG			-40 to +85	8 Ld SOIC	M8.15E
X9317WV8Z-2.7	9317W FZ			0 to +70	8 Ld TSSOP	M8.173
X9317WV8IZ-2.7	AKZ			-40 to +85	8 Ld TSSOP	M8.173
X9317UM8Z-2.7	AOB		50	0 to +70	8 Ld MSOP	M8.118
X9317UM8IZ-2.7	AOH			-40 to +85	8 Ld MSOP	M8.118
X9317US8Z-2.7	X9317U ZF			0 to +70	8 Ld SOIC	M8.15E
X9317US8IZ-2.7	X9317U ZG			-40 to +85	8 Ld SOIC	M8.15E
X9317UV8Z-2.7	9317U FZ			0 to +70	8 Ld TSSOP	M8.173
X9317UV8IZ-2.7	9317U GZ			-40 to +85	8 Ld TSSOP	M8.173
X9317TM8Z-2.7	DCP		100	0 to +70	8 Ld MSOP	M8.118
X9317TM8IZ-2.7	DCM			-40 to +85	8 Ld MSOP	M8.118
X9317TS8Z-2.7	X9317T ZF			0 to +70	8 Ld SOIC	M8.15E
X9317TS8IZ-2.7	X9317T ZG			-40 to +85	8 Ld SOIC	M8.15E
X9317TV8Z-2.7	9317T FZ			0 to +70	8 Ld TSSOP	M8.173
X9317TV8IZ-2.7	9317T GZ			-40 to +85	8 Ld TSSOP	M8.173

NOTES:

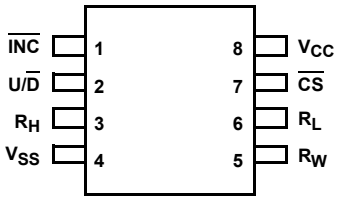
1. Add “T1” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for X9317. For more information on MSL please see tech brief TB363.

Pin Configurations

X9317
(8 LD TSSOP)
TOP VIEW



X9317
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



Pin Descriptions

SOIC/MSOP	TSSOP	SYMBOL	BRIEF DESCRIPTION
1	3	$\overline{INC}$	**Increment** Toggling $\overline{INC}$ while $\overline{CS}$ is low moves the wiper either up or down.
2	4	U/$\overline{D}$	**Up/Down** The U/$\overline{D}$ input controls the direction of the wiper movement.
3	5	R_H	The high terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
4	6	V_{SS}	**Ground**
5	7	R_W	The wiper terminal is equivalent to the movable terminal of a mechanical potentiometer.
6	8	R_L	The low terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
7	1	$\overline{CS}$	**Chip Select** The device is selected when the $\overline{CS}$ input is LOW, and de-selected when $\overline{CS}$ is high.
8	2	V_{CC}	**Supply Voltage**

Absolute Maximum Ratings

I_W (10s) . . . . . ±8.8mA
R_H, R_W, R_L to Ground . . . . . +6V
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
with Respect to V_{SS} . . . . . -1V to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Notes 4, 5)	115	60
MSOP Package (Notes 4, 5)	145	55
TSSOP Package (Notes 4, 5)	155	49

Junction Temperature Under Bias . . . . . -65°C to +135°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Potentiometer Specifications

V_{CC} = full range. **Boldface limits apply across the operating temperature range, -40°C to +85°C (Industrial) and 0°C to +70°C (Commercial).**

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN (Note 13)	TYP (Note 9)	MAX (Note 13)	UNIT
R_{TOTAL}	End-to-end Resistance Tolerance	See "Ordering Information" on page 2 for values	**-20**		**+20**	%
V_{RH}/R_L	R_H/R_L Terminal Voltage	V_{SS} = 0V	**V_{SS}**		**V_{CC}**	V
	Power Rating	R_{TOTAL} ≥ 10kΩ			**10**	mW
R_W	Wiper Resistance	I_W = [V(R_H) - V(R_L)]/ R_{TOTAL}, V_{CC} = 5V		200	**400**	Ω
		I_W = [V(R_H) - V(R_L)]/ R_{TOTAL}, V_{CC} = 2.7V		400	**1000**	Ω
I_W	Wiper Current (Note 10)	See "Test Circuit" on page 5	**-4.4**		**+4.4**	mA
	Noise (Note 12)	Ref: 1kHz		-120		dBV
	Resolution			1		%
	Absolute Linearity (Note 6)	V(R_H) = V_{CC}, V(R_L) = 0V	**-1**		**+1**	MI (Note 8)
	Relative Linearity (Note 7)	V(R_H) = V_{CC}, V(R_L) = 0V	**-0.2**		**+0.2**	MI (Note 8)
	R_{TOTAL} Temperature Coefficient (Note 10)	V(R_H) = V_{CC}, V(R_L) = 0V		±300		ppm/°C
	Ratiometric Temperature Coefficient (Notes 10, 11)			±20		ppm/°C
$C_H/C_L/C_W$ (Note 10)	Potentiometer Capacitances	See "Equivalent Circuit" on page 5		10/10/25		pF
V_{CC}	Supply Voltage	X9317	**4.5**		**5.5**	V
		X9317-2.7	**2.7**		**5.5**	V

DC Electrical Specifications

V_{CC} = 5V ±10%. **Boldface limits apply across the operating temperature range, -40°C to +85°C (Industrial) and 0°C to +70°C (Commercial).**

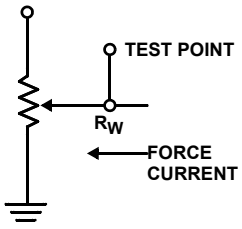
SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 13)	TYP (Note 9)	MAX (Note 13)	UNIT
I_{CC1}	V_{CC} Active Current (Increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IL}/V_{IH} at min. t_{CYC} R_L, R_H, R_W not connected			**80**	µA
I_{CC2}	V_{CC} Active Current (Store) (non-volatile write)	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IL} or V_{IH}. R_L, R_H, R_W not connected			**400**	µA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, U/$\overline{D}$ and $\overline{INC}$ = V_{IL} R_L, R_H, R_W not connected			**5**	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current	V_{IN} = V_{SS} to V_{CC}	**-10**		**+10**	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage		**V_{CC} x 0.7**		**V_{CC} + 0.5**	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Voltage		**-0.5**		**V_{CC} x 0.1**	V
C_{IN} (Note 10)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = +25°C, f = 1MHz		10		pF

Endurance and Data Retention

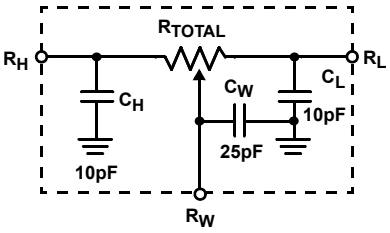
V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range.

PARAMETER	MIN	UNIT
Minimum Endurance	100,000	Data changes per bit
Data Retention	100	Years

Test Circuit



Equivalent Circuit



AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

AC Electrical Specifications

V_{CC} = 5V ±10%. **Boldface limits apply across the operating temperature range, -40°C to +85°C (Industrial) and 0°C to +70°C (Commercial).**

SYMBOL	PARAMETER	MIN (Note 13)	TYP (Note 9)	MAX (Note 13)	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	**50**			ns
t_{ID} (Note 10)	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	**100**			ns
t_{DI} (Note 10)	U/$\overline{D}$ to $\overline{INC}$ Setup	**1**			µs
t_{IL}	$\overline{INC}$ LOW Period	**960**			ns
t_{IH}	$\overline{INC}$ HIGH Period	**960**			ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	**1**			µs
t_{CPHS}	$\overline{CS}$ Deselect Time (STORE)	**10**			ms
t_{CPHNS} (Note 10)	$\overline{CS}$ Deselect Time (NO STORE)	**100**			ns
t_{IW}	$\overline{INC}$ to R_W Change		1	**5**	µs
t_{CYC}	$\overline{INC}$ Cycle Time	**2**			µs

AC Electrical Specifications V_{CC} = 5V ±10%. **Boldface limits apply across the operating temperature range, -40°C to +85°C (Industrial) and 0°C to +70°C (Commercial). (Continued)**

SYMBOL	PARAMETER	MIN (Note 13)	TYP (Note 9)	MAX (Note 13)	UNIT
t_R, t_F (Note 10)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU} (Note 10)	Power-up to Wiper Stable			5	µs
t_R V_{CC} (Note 10)	V_{CC} Power-up Rate	0.2		50	V/ms
t_{WR}	Store Cycle		5	10	ms

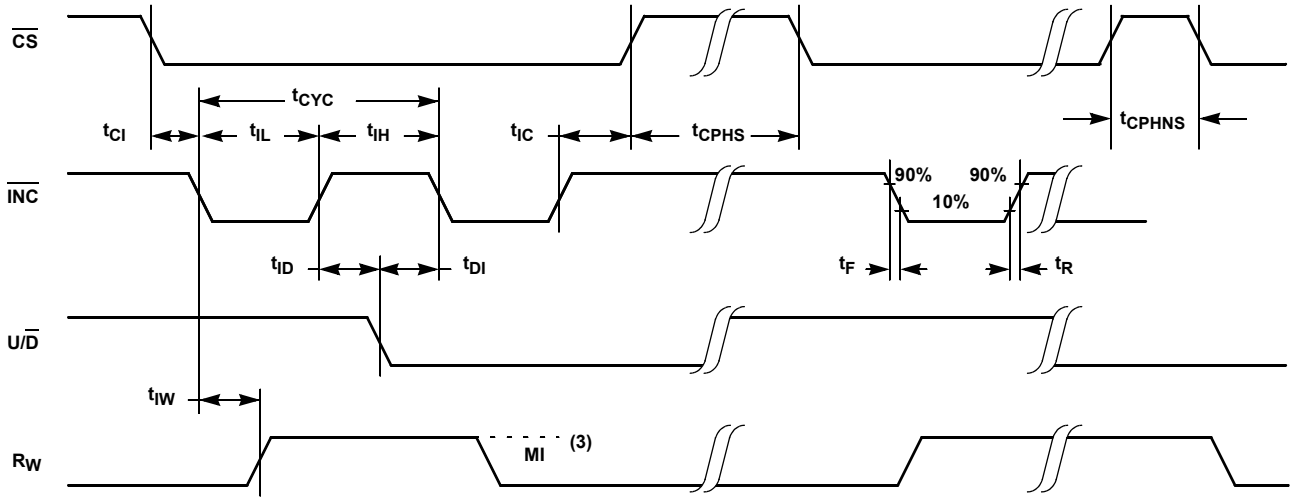
NOTES:

6. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $[V(R_{W(n)(actual)})-V(R_{W(n)(expected)})]/MI$ $V(R_{W(n)(expected)}) = n(V(R_H)-V(R_L))/99 + V(R_L)$, with n from 0 to 99.
7. Relative linearity is a measure of the error in step size between taps = $[V(R_{W(n+1)})-(V(R_{W(n)}) - MI)]/MI$.
8. 1 MI = Minimum Increment = $[V(R_H)-V(R_L)]/99$.
9. Typical values are for T_A = +25°C and nominal supply voltage.
10. This parameter is not 100% tested.
11. Ratiometric temperature coefficient = $(V(R_W)_{T1(n)}-V(R_W)_{T2(n)})/[V(R_W)_{T1(n)}(T1-T2) \times 10^6]$, with T1 and T2 being 2 temperatures, and n from 0 to 99.
12. Measured with wiper at tap position 99, R_L grounded, using test circuit.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Power-up and Down Requirements

The recommended power-up sequence is to apply V_{CC}/V_{SS} first, then the potentiometer voltages. During power-up, the data sheet parameters for the DCP do not fully apply until 1ms after V_{CC} reaches its final value. The V_{CC} ramp spec is always in effect. In order to prevent unwanted tap position changes, or an inadvertent store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin on power-up.

AC Timing



Typical Performance Characteristic

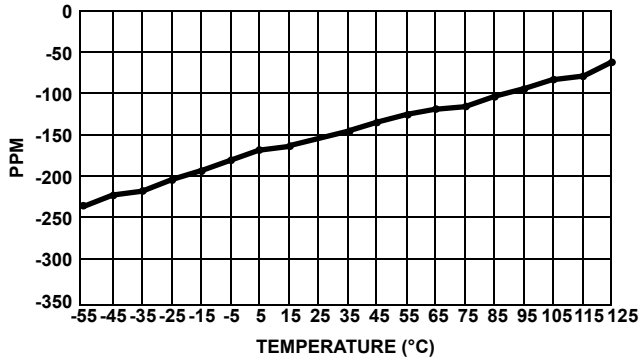


FIGURE 2. TYPICAL TOTAL RESISTANCE TEMPERATURE COEFFICIENT

Pin Descriptions

R_H and R_L

The high (R_H) and low (R_L) terminals of the X9317 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete, the X9317 will be placed in the low power standby mode until the device is selected once again.

Principles of Operation

There are three sections of the X9317: the control section, the nonvolatile memory, and the resistor array. The control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. Electronic switches at either end of the array and between each resistor provide an electrical connection to the wiper pin, R_W.

The wiper acts like its mechanical equivalent and does not move beyond the first or last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH-to-LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a 7-bit counter. The output of this counter is decoded to select one of one hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9317, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalls the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper up
L	↘	L	Wiper down
↗	H	X	Store wiper position to nonvolatile memory
H	X	X	Standby
↗	L	X	No store, return to standby
↘	L	H	Wiper up (not recommended)
↘	L	L	Wiper down (not recommended)

Applications Information

Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages:

1. The variability and reliability of a solid-state potentiometer,
2. The flexibility of computer-based digital controls, and
3. The retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers

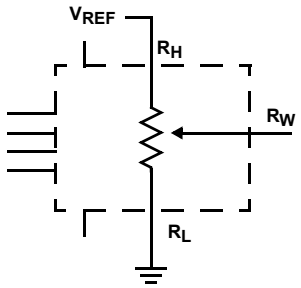


FIGURE 3. THREE TERMINAL POTENTIOMETER; VARIABLE VOLTAGE DIVIDER

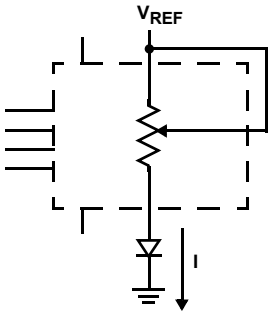


FIGURE 4. TWO TERMINAL VARIABLE RESISTOR; VARIABLE CURRENT

Basic Circuits

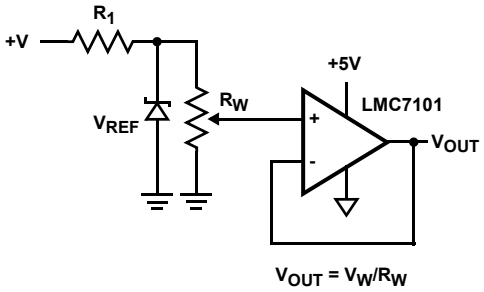


FIGURE 5. BUFFERED REFERENCE VOLTAGE

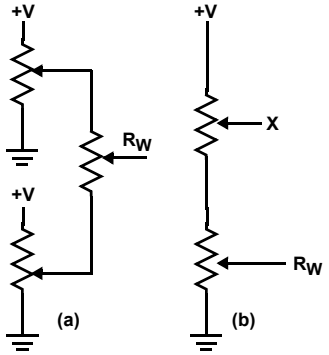


FIGURE 6. CASCADING TECHNIQUES

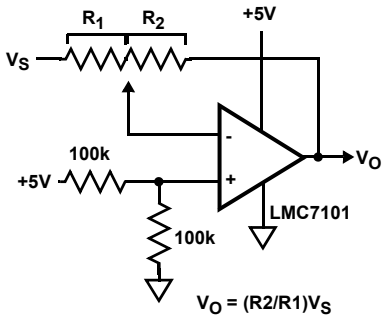


FIGURE 7. SINGLE SUPPLY INVERTING AMPLIFIER

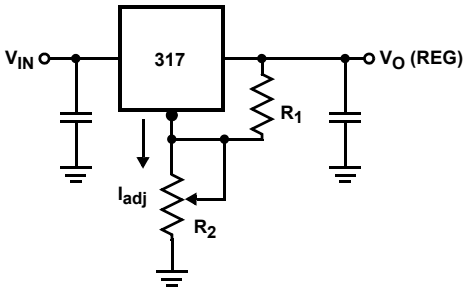


FIGURE 8. VOLTAGE REGULATOR

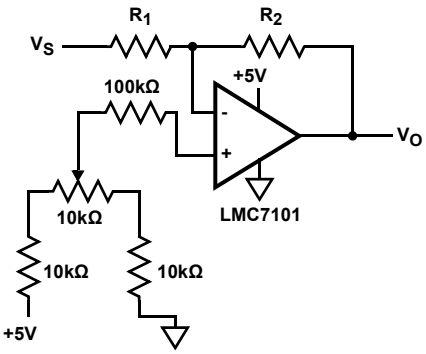


FIGURE 9. OFFSET VOLTAGE ADJUSTMENT

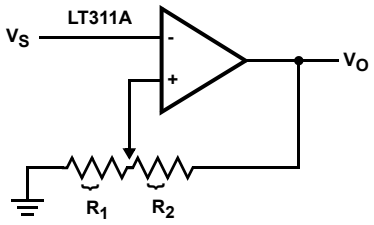


FIGURE 10. COMPARATOR WITH HYSTERESIS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
November 4, 2014	FN8183.9	Added Revision History Converted to New Template and added new Intersil Standards. Updated Ordering Information to show all U parts in column for Rtotal (kΩ) to show 50 as the value. Added thermal information (Tja and Tjc).

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

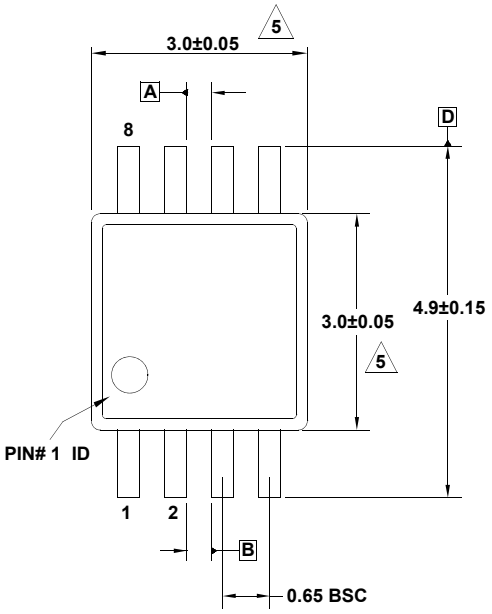
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

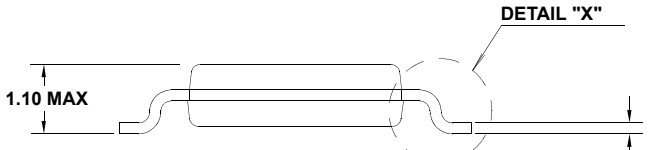
M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

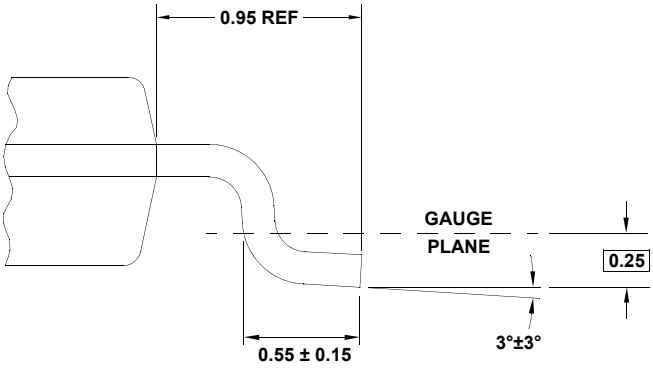
Rev 4, 7/11



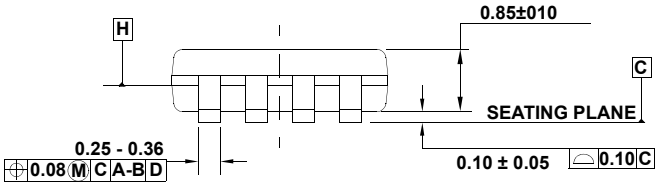
TOP VIEW



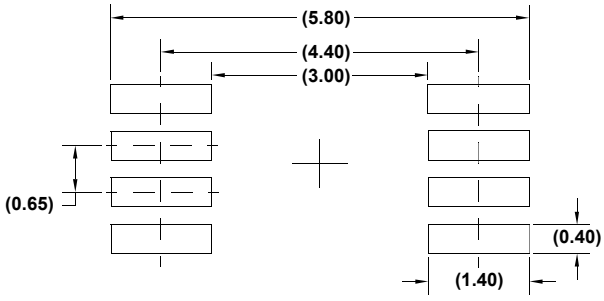
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

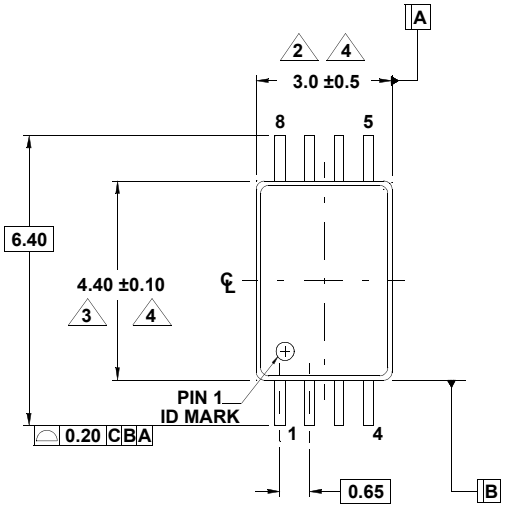
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Package Outline Drawing

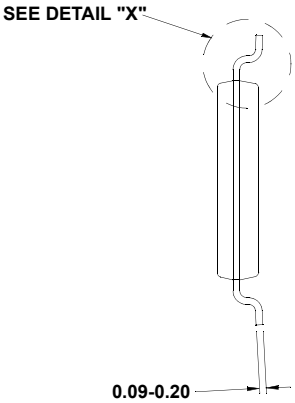
M8.173

8 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

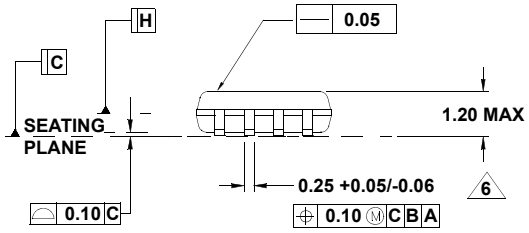
Rev 2, 01/10



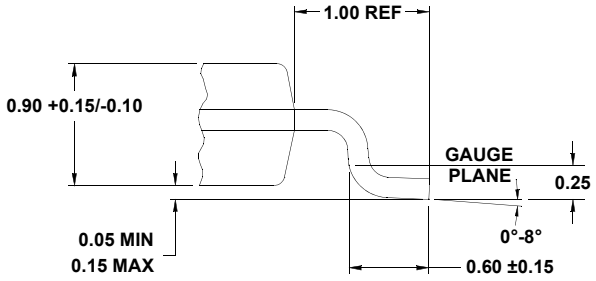
TOP VIEW



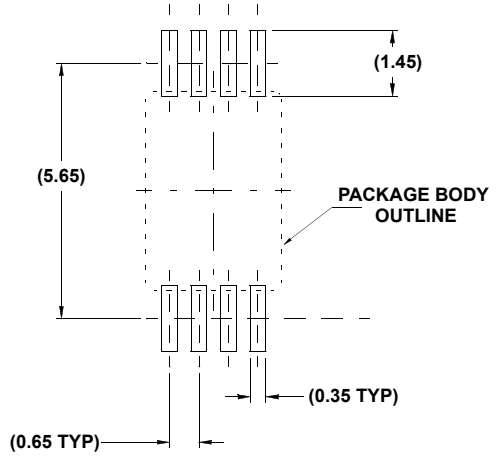
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

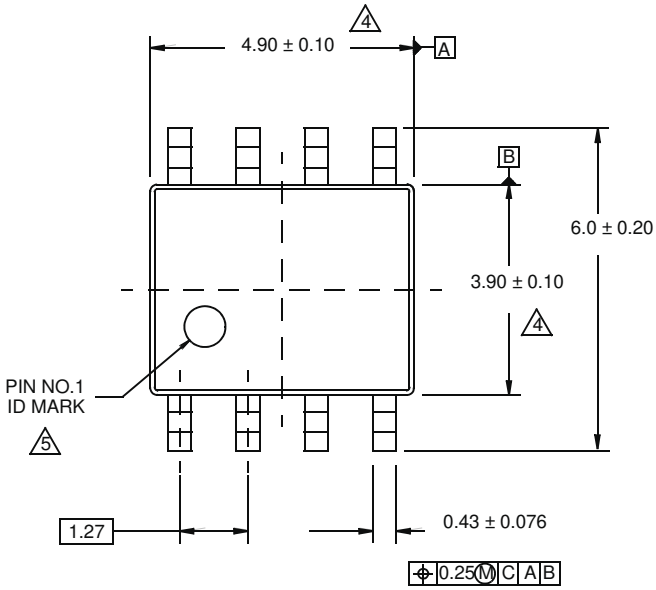
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 per side.
4. Dimensions are measured at datum plane H.
5. Dimensioning and tolerancing per ASME Y14.5M-1994.
6. Dimension on lead width does not include dambar protrusion. Allowable protrusion shall be 0.08 mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
7. Conforms to JEDEC MO-153, variation AC. Issue E

Package Outline Drawing

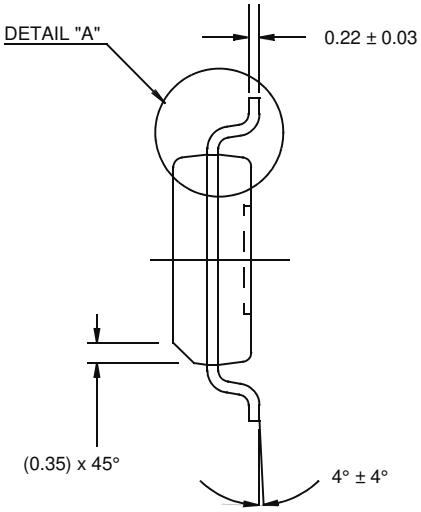
M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

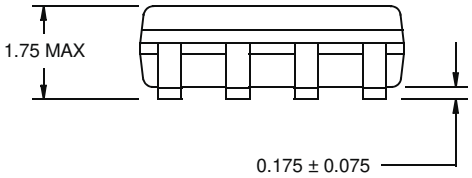
Rev 0, 08/09



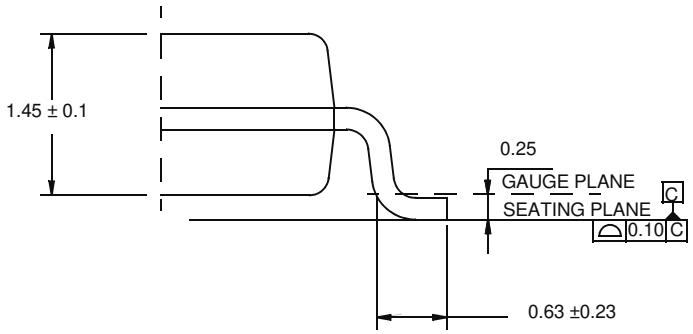
TOP VIEW



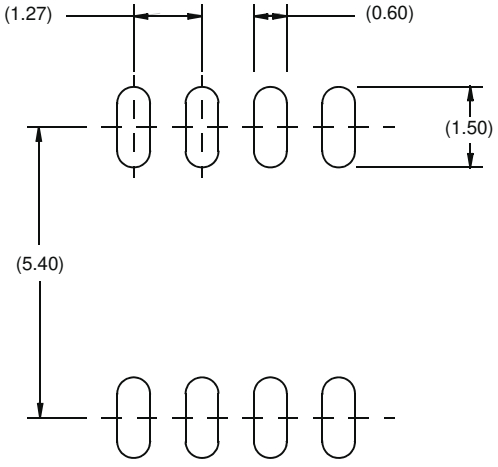
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.