



# 32-Tap Digitally Programmable Potentiometer (DPP™)



## FEATURES

- 32-position linear taper potentiometer
- Low power CMOS technology
- Single supply operation: 2.5V – 6V
- Increment up/down serial interface
- Resistance values: 10kΩ, 50kΩ and 100kΩ
- Available in PDIP, SOIC, TSSOP, MSOP and space saving 2 x 2.5mm TDFN packages

## APPLICATIONS

- Automated product calibration
- Remote control adjustments
- Offset, gain and zero control
- Tamper-proof calibrations
- Contrast, brightness and volume controls
- Motor controls and feedback systems
- Programmable analog functions

For Ordering Information details, see page 13.

## DESCRIPTION

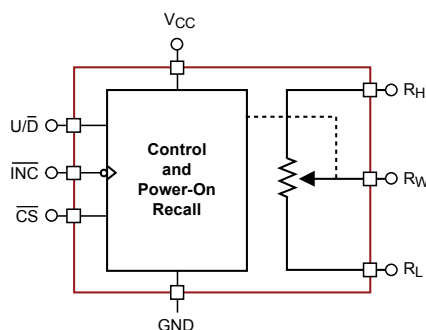
The CAT5115 is a single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5115 contains a 32-tap series resistor array connected between two terminals  $R_H$  and  $R_L$ . An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper,  $R_W$ . The wiper is always set to the mid point, tap 15 at power up. The tap position is not stored in memory. Wiper-control of the CAT5115 is accomplished with three input control pins,  $\overline{CS}$ ,  $U/\overline{D}$ , and  $\overline{INC}$ . The  $\overline{INC}$  input increments the wiper in the direction which is determined by the logic state of the  $U/\overline{D}$  input. The  $\overline{CS}$  input is used to select the device.

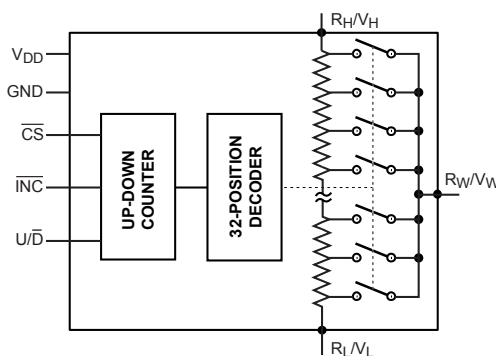
The digitally programmable potentiometer can be used as a three-terminal resistive divider or as a two-terminal variable resistor. DPPs bring variability and programmability to a wide variety of applications including control, parameter adjustments, and signal processing.

For a pin-compatible device that recalls a stored tap position on power-up refer to the CAT5114 data sheet.

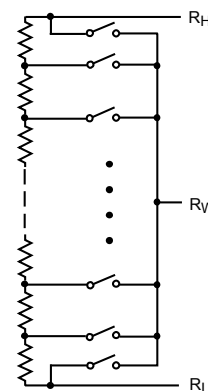
## FUNCTIONAL DIAGRAM



General

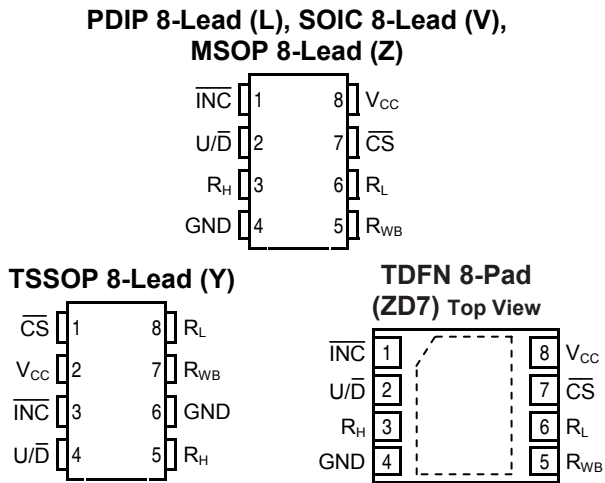


Detailed



Electronic Potentiometer Implementation

**PIN CONFIGURATION**



**PIN DESCRIPTIONS**

Name	Function
$\overline{INC}$	Increment Control
$U/\overline{D}$	Up/Down Control
$R_H$	Potentiometer High Terminal
GND	Ground
$R_W$	Buffered Wiper Terminal
$R_L$	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
$V_{CC}$	Supply Voltage

**PIN FUNCTION**

**$\overline{INC}$ :** Increment Control Input

The  $\overline{INC}$  input moves the wiper in the up or down direction determined by the condition of the  $U/\overline{D}$  input.

**$U/\overline{D}$ :** Up/Down Control Input

The  $U/\overline{D}$  input controls the direction of the wiper movement. When in a high state and  $\overline{CS}$  is low, any high-to-low transition on  $\overline{INC}$  will cause the wiper to move one increment toward the  $R_H$  terminal. When in a low state and  $\overline{CS}$  is low, any high-to-low transition on  $\overline{INC}$  will cause the wiper to move one increment towards the  $R_L$  terminal.

**$R_H$ :** High End Potentiometer Terminal

$R_H$  is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the  $R_L$  terminal. Voltage applied to the  $R_H$  terminal cannot exceed the supply voltage,  $V_{CC}$  or go below ground, GND.

**$R_W$ :** Wiper Potentiometer Terminal

$R_W$  is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs,  $\overline{INC}$ ,  $U/\overline{D}$  and  $\overline{CS}$ . Voltage applied to the  $R_W$  terminal cannot exceed the supply voltage,  $V_{CC}$  or go below ground, GND.

**$R_L$ :** Low End Potentiometer Terminal

$R_L$  is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the  $R_H$  terminal. Voltage applied to the  $R_L$  terminal cannot exceed the supply voltage,  $V_{CC}$  or go below ground, GND.  $R_L$  and  $R_H$  are electrically interchangeable.

**$\overline{CS}$ :** Chip Select

The chip select input is used to activate the control input of the CAT5115 and is active low. When in a high state, activity on the  $\overline{INC}$  and  $U/\overline{D}$  inputs will not affect or change the position of the wiper.

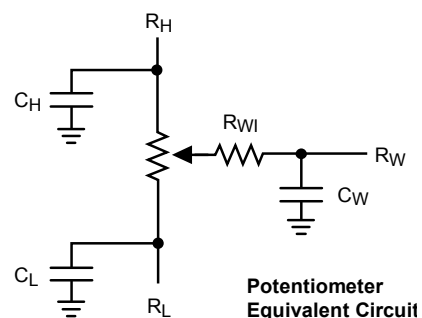
**DEVICE OPERATION**

The CAT5115 operates like a digitally controlled potentiometer with  $R_H$  and  $R_L$  equivalent to the high and low terminals and  $R_W$  equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points,  $R_H$  and  $R_L$ . There are 31 resistor elements connected in series between the  $R_H$  and  $R_L$  terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs,  $\overline{INC}$ ,  $U/\overline{D}$  and  $\overline{CS}$ . These inputs control a five-bit up/down counter whose output is decoded to select the wiper position.

With  $\overline{CS}$  set LOW the CAT5115 is selected and will respond to the  $U/\overline{D}$  and  $\overline{INC}$  inputs. HIGH to LOW transitions on  $\overline{INC}$  will increment or decrement the wiper (depending on the state of the  $U/\overline{D}$  input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. When the CAT5115 is powered-down, the wiper position is reset. When power is restored, the counter is set to the mid point, tap 15.

## OPERATION MODES

$\overline{\text{INC}}$	$\overline{\text{CS}}$	$\text{U}/\overline{\text{D}}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby

ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Parameters	Ratings	Units
Supply Voltage $V_{CC}$ to GND	-0.5 to +7V	V
Inputs		
$\overline{\text{CS}}$ to GND	-0.5 to $V_{CC} + 0.5$	V
$\overline{\text{INC}}$ to GND	-0.5 to $V_{CC} + 0.5$	V
$\text{U}/\overline{\text{D}}$ to GND	-0.5 to $V_{CC} + 0.5$	V
H to GND	-0.5 to $V_{CC} + 0.5$	V
L to GND	-0.5 to $V_{CC} + 0.5$	V
W to GND	-0.5 to $V_{CC} + 0.5$	V

Parameters	Ratings	Units
Operating Ambient Temperature Industrial ('I' suffix)	-40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	-65 to 150	°C
Lead Soldering (10s max)	+300	°C

## RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
$V_{ZAP}^{(2)}$	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			V
$I_{LTH}^{(2)(3)}$	Latch-Up	JEDEC Standard 17	100			mA
$T_{DR}$	Data Retention	MIL-STD-883, Test Method 1008	100			Years
$N_{END}$	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

## DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +2.5V$  to  $+6V$  unless otherwise specified

## Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{CC}$	Operating Voltage Range		2.5	–	6	V
$I_{CC1}$	Supply Current (Increment)	$V_{CC} = 6V, f = 1MHz, I_W = 0$	–	–	100	$\mu A$
		$V_{CC} = 6V, f = 250kHz, I_W = 0$	–	–	50	$\mu A$
$I_{SB1}^{(3)}$	Supply Current (Standby)	$\overline{\text{CS}} = V_{CC} - 0.3V$ $\text{U}/\overline{\text{D}}, \overline{\text{INC}} = V_{CC} - 0.3V$ or GND	–	0.01	1	$\mu A$

## Notes:

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.
- This parameter is tested initially and after a design or process change that affects the parameter.
- Latch-up protection is provided for stresses up to 100mA on address and data pins from  $-1V$  to  $V_{CC} + 1V$ .
- $I_W$  = source or sink.
- These parameters are periodically sampled and are not 100% tested.

Logic Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IH}$	Input Leakage Current	$V_{IN} = V_{CC}$	-	-	10	$\mu A$
$I_{IL}$	Input Leakage Current	$V_{IN} = 0V$	-	-	-10	$\mu A$
$V_{IH1}$	TTL High Level Input Voltage	$4.5V \leq V_{CC} \leq 5.5V$	2	-	$V_{CC}$	V
$V_{IL1}$	TTL Low Level Input Voltage		0	-	0.8	V
$V_{IH2}$	CMOS High Level Input Voltage	$2.5V \leq V_{CC} \leq 6V$	$V_{CC} \times 0.7$	-	$V_{CC} + 0.3$	V
$V_{IL2}$	CMOS Low Level Input Voltage		-0.3	-	$V_{CC} \times 0.2$	V

Potentiometer Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$R_{POT}$	Potentiometer Resistance	-10 Device		10		k $\Omega$
		-50 Device		50		
		-00 Device		100		
	Pot. Resistance Tolerance				$\pm 20$	%
$V_{RH}$	Voltage on $R_H$ pin		0		$V_{CC}$	V
$V_{RL}$	Voltage on $R_L$ pin		0		$V_{CC}$	V
	Resolution			3.2		%
INL	Integral Linearity Error	$I_W \leq 2\mu A$		0.5	1	LSB
DNL	Differential Linearity Error	$I_W \leq 2\mu A$		0.25	0.5	LSB
$R_{WI}$	Wiper Resistance	$V_{CC} = 5V, I_W = 1mA$		70	200	$\Omega$
		$V_{CC} = 2.5V, I_W = 1mA$		150	400	$\Omega$
$I_W$	Wiper Current	(1)			1	mA
$TC_{RPOT}$	TC of Pot Resistance			$\pm 50$	$\pm 300$	ppm/ $^{\circ}C$
$TC_{RATIO}$	Ratiometric TC				20	ppm/ $^{\circ}C$
$V_N$	Noise	100kHz / 1kHz		8/24		nV/ $\sqrt{Hz}$
$C_H/C_L/C_W$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10k $\Omega$		1.7		MHz

## AC CONDITIONS OF TEST

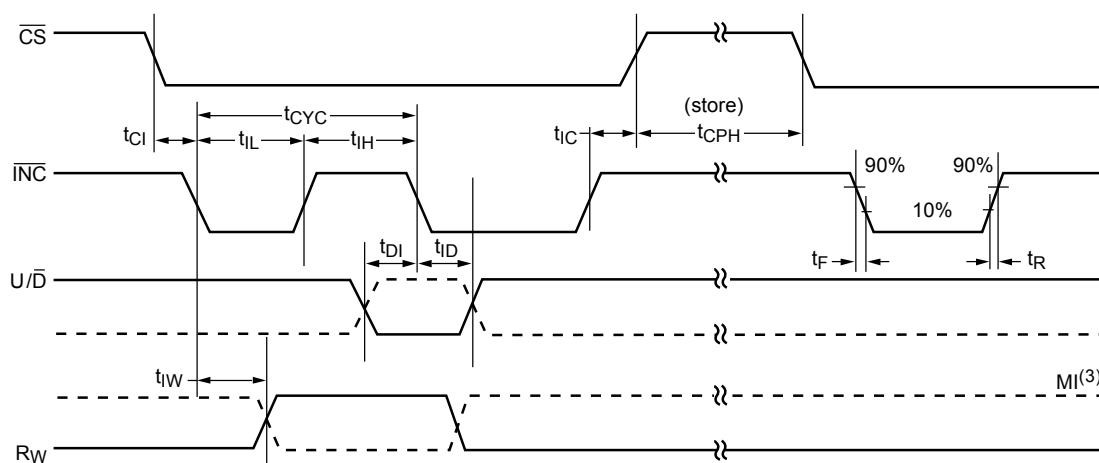
$V_{CC}$ Range	$2.5V \leq V_{CC} \leq 6.0V$
Input Pulse Levels	$0.2V_{CC}$ to $0.7V_{CC}$
Input Rise and Fall Times	10ns
Input Reference Levels	$0.5V_{CC}$

## AC OPERATING CHARACTERISTICS

$V_{CC} = +2.5V$  to  $+6.0V$ ,  $V_H = V_{CC}$ ,  $V_L = 0V$ , unless otherwise specified

Symbol	Parameter	Min	Typ <sup>(1)</sup>	Max	Units
$t_{CI}$	$\overline{CS}$ to $\overline{INC}$ Setup	100	–	–	ns
$t_{DI}$	$U/\overline{D}$ to $\overline{INC}$ Setup	50	–	–	ns
$t_{ID}$	$U/\overline{D}$ to $\overline{INC}$ Hold	100	–	–	ns
$t_{IL}$	$\overline{INC}$ LOW Period	250	–	–	ns
$t_{IH}$	$\overline{INC}$ HIGH Period	250	–	–	ns
$t_{IC}$	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	–	–	$\mu s$
$t_{CPH}$	$\overline{CS}$ Deselect Time	100	–	–	ns
$t_{IW}$	$\overline{INC}$ to $V_{OUT}$ Change	–	1	5	$\mu s$
$t_{CYC}$	$\overline{INC}$ Cycle Time	1	–	–	$\mu s$
$t_R, t_F^{(2)}$	$\overline{INC}$ Input Rise and Fall Time	–	–	500	$\mu s$
$t_{PU}^{(2)}$	Power-up to Wiper Stable	–	–	1	ms

## A.C. TIMING

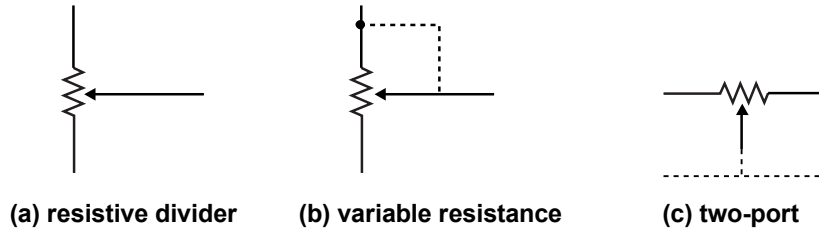


## Notes:

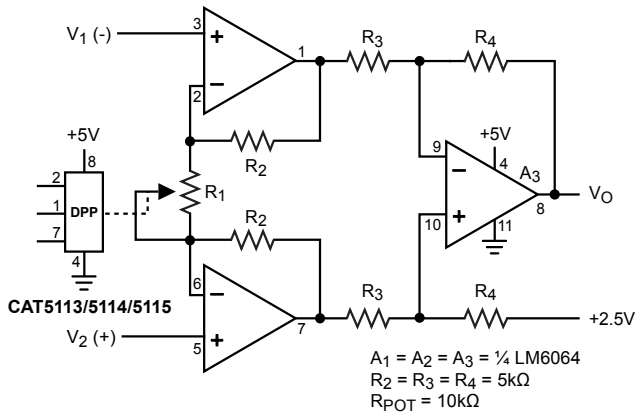
- (1) Typical values are for  $T_A = 25^\circ C$  and nominal supply voltage.
- (2) This parameter is periodically sampled and not 100% tested.
- (3)  $Ml$  in the A.C. Timing diagram refers to the minimum incremental change in the  $W$  output due to a change in the wiper position.

APPLICATIONS INFORMATION

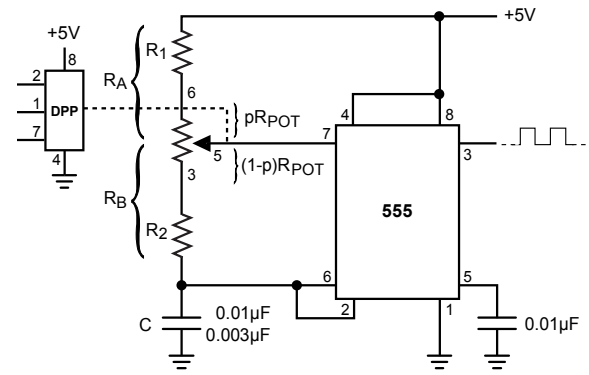
POTENTIOMETER CONFIGURATION



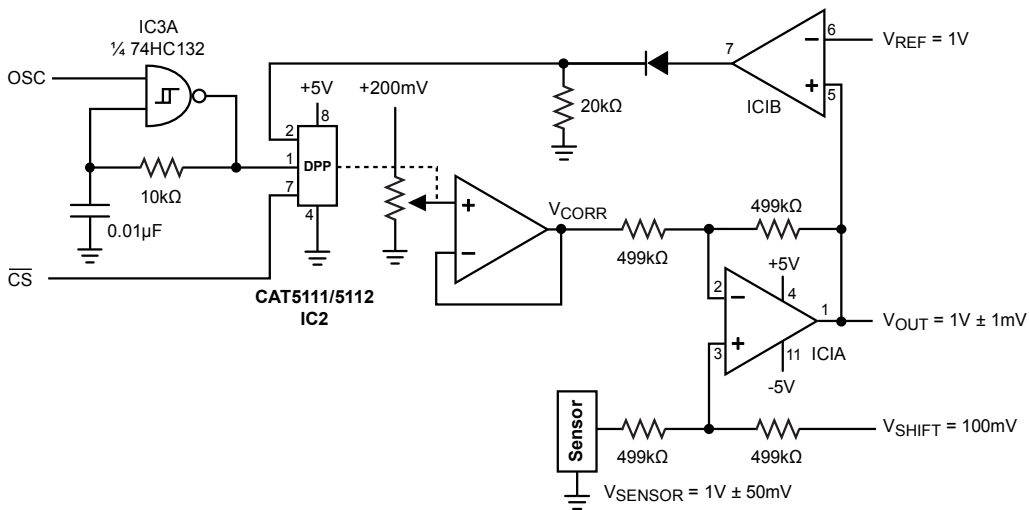
APPLICATIONS



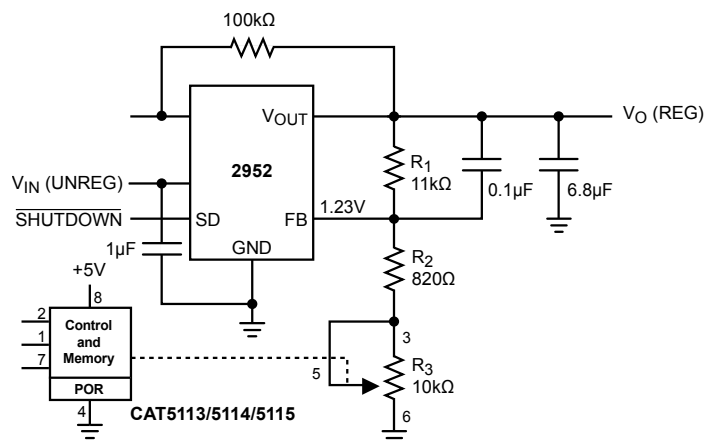
Programmable Instrumentation Amplifier



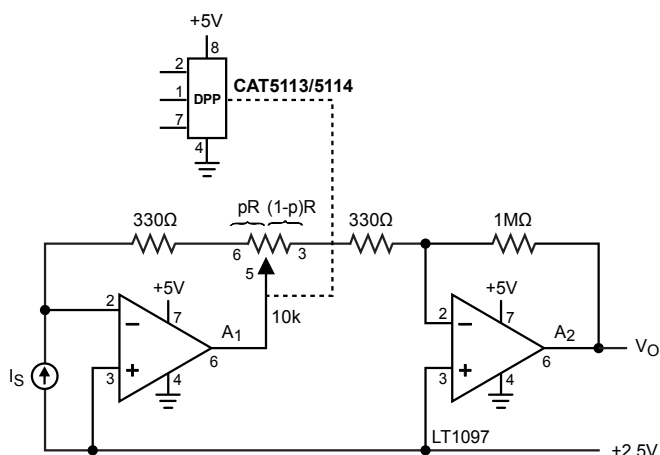
Programmable Sq. Wave Oscillator (555)



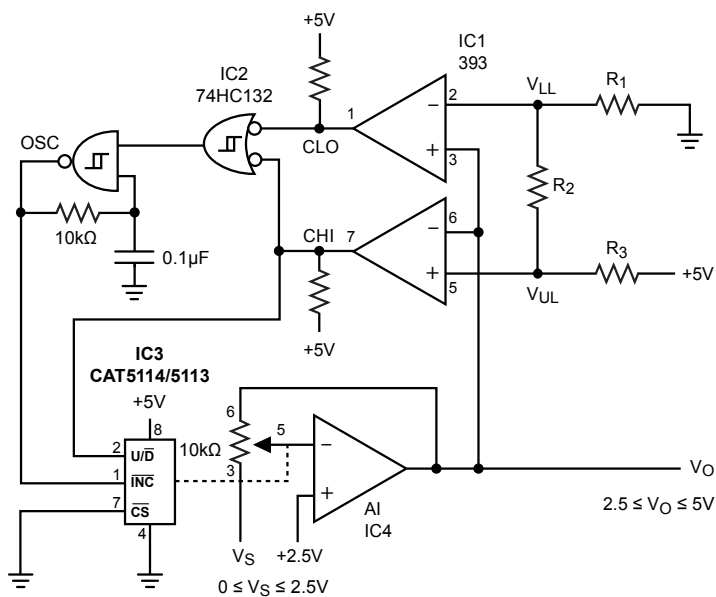
Sensor Auto Referencing Circuit



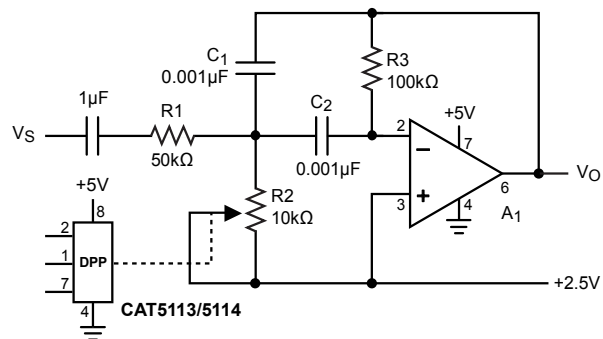
Programmable Voltage Regulator



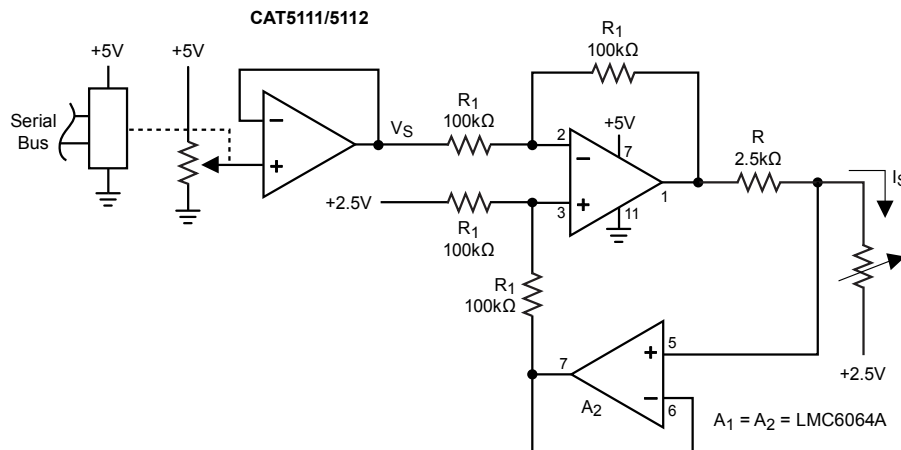
Programmable I to V Converter



Automatic Gain Control



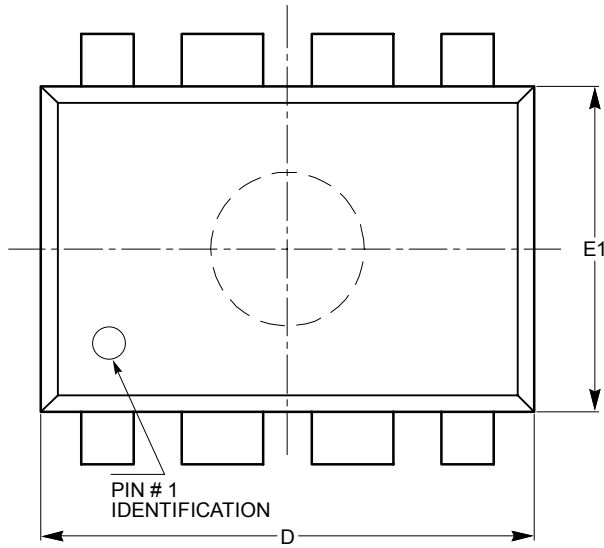
Programmable Bandpass Filter



Programmable Current Source/Sink

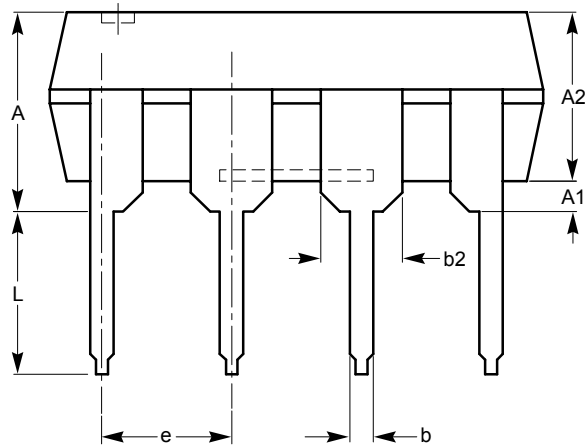
**PACKAGE OUTLINE DRAWINGS**

**PDIP 8-Lead 300mils (L) <sup>(1)(2)</sup>**

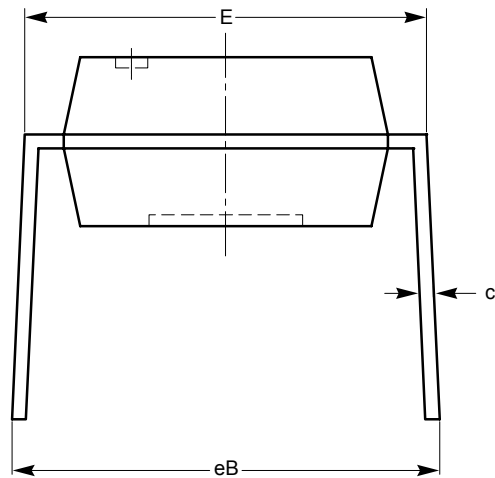


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
e	2.54 BSC		
E1	6.10	6.35	7.11
eB	7.87		10.92
L	2.92	3.30	3.80



**SIDE VIEW**



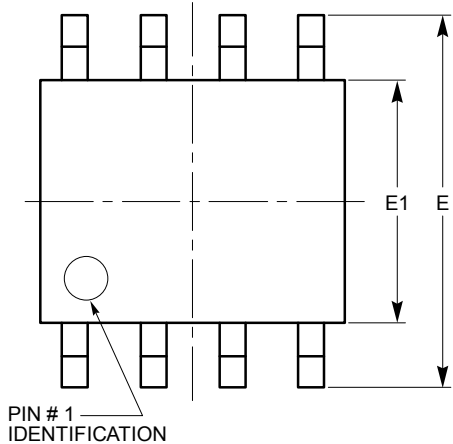
**END VIEW**

**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC standard MS-001.

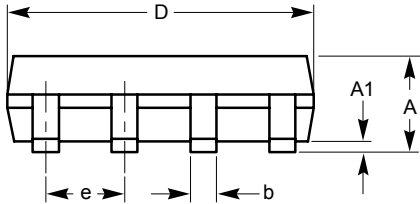


SOIC 8-Lead 150mils (V) <sup>(1)(2)</sup>

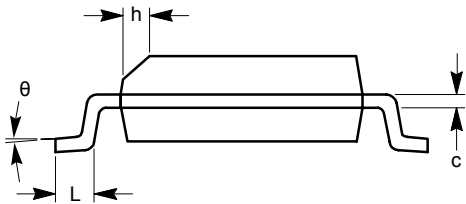


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



SIDE VIEW

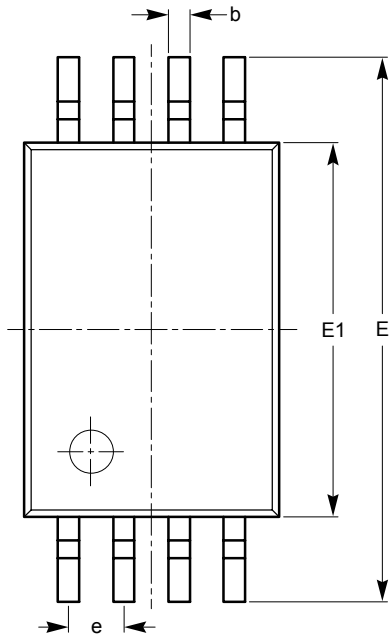


END VIEW

Notes:

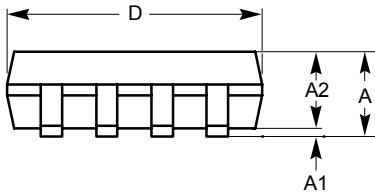
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MS-012.

TSSOP 8-Lead 4.4mm (Y) <sup>(1)(2)</sup>

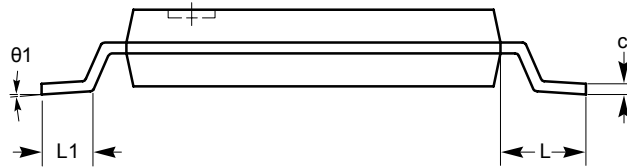


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
$\theta 1$	0°		8°



SIDE VIEW

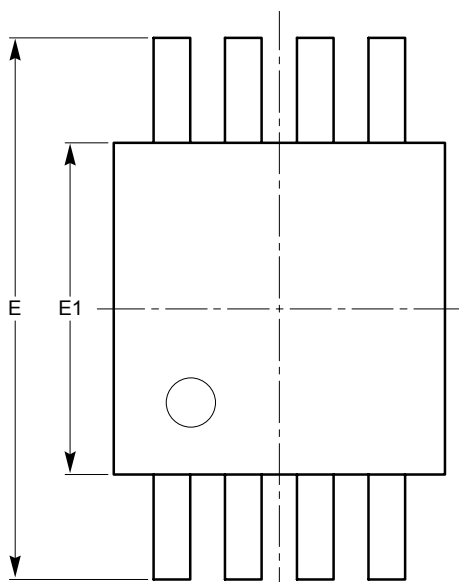


END VIEW

Notes:

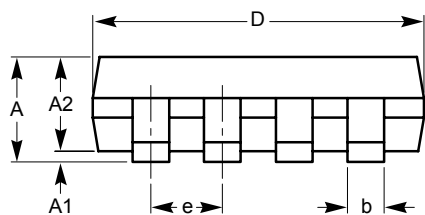
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MO-153.

MSOP 8-Lead 3.0 x 3.0mm (Z) <sup>(1)(2)</sup>

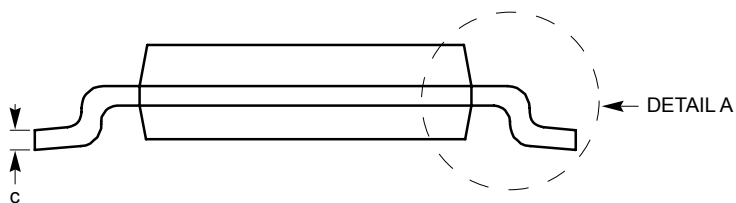


TOP VIEW

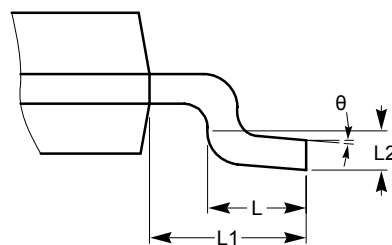
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
$\theta$	0°		6°



SIDE VIEW



END VIEW

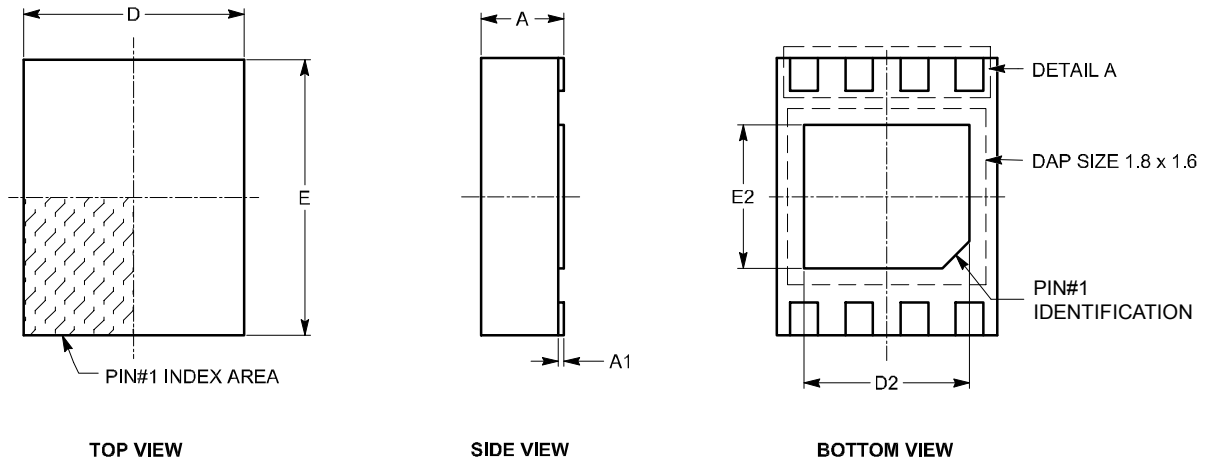


DETAIL A

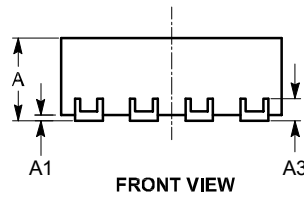
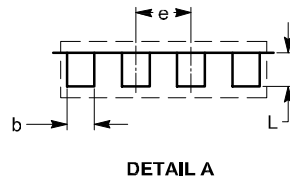
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MO-187.

TDFN 8-Pad 2 x 2.5mm (ZD7) <sup>(1)(2)</sup>



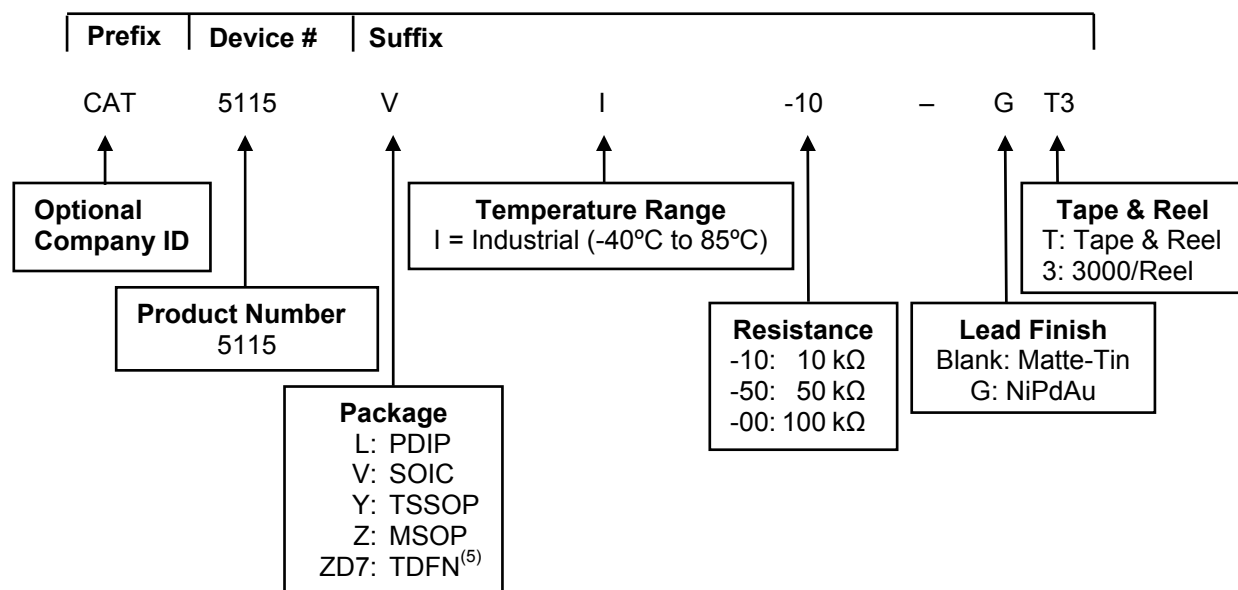
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
E	2.40	2.50	2.60
E2	1.20	1.30	1.40
e	0.50 TYP		
L	0.20	0.30	0.40



Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC standard MO-229.

## EXAMPLE OF ORDERING INFORMATION



## ORDERING INFORMATION


ORDERABLE PART NUMBER
CAT5115LI-10-G
CAT5115LI-50-G
CAT5115LI-00-G
CAT5115VI-10-GT3
CAT5115VI-50-GT3
CAT5115VI-00-GT3
CAT5115YI-10-GT3
CAT5115YI-50-GT3
CAT5115YI-00-GT3
CAT5115ZI-10-GT3
CAT5115ZI-50-GT3
CAT5115ZI-00-GT3
CAT5115ZD7I-10-T3 <sup>(6)</sup>
CAT5115ZD7I-50-T3 <sup>(6)</sup>
CAT5115ZD7I-00-T3 <sup>(6)</sup>

## Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) This device used in the above example is a CAT5115VI-10-GT3 (SOIC, Industrial Temperature, 10kΩ, NiPdAu, Tape & Reel).
- (4) For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
- (5) TDFN is not available in NiPdAu (-G) version.
- (6) Contact factory for package availability.

**REVISION HISTORY**

Date	Rev.	Description
25-Sep-03	B	Changed designation to Preliminary. Updated Description. Updated Potentiometer Parameters table.
10-Mar-04	C	Updated Potentiometer Parameters table.
29-Mar-04	D	Changed Green Package marking for SOIC from W to V
12-Apr-04	E	Updated Tape and Reel specs in Ordering Information
31-Aug-04	F	Deleted I <sub>CC2</sub> from DC Characteristics table Updated AC Operating Characteristics table Updated A.C. Timing diagram.
06-Jul-07	G	Update Absolute Maximum Ratings table Update DC Electrical Characteristics tables Update AC Conditions of Test table Update all Package Outline Drawings Update Example of Ordering Information Update Ordering Part Number
02-Feb-08	H	Update Functional Diagram Update Package Outline Drawings
21-Nov-08	I	Change logo and fine print to ON Semiconductor
31-Jul-09	J	Update Ordering Information

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center:**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative