

ISL22319

Single Digitally Controlled Potentiometer (XDCP™) Low Noise, Low Power, I²C Bus, 128 Taps, Wiper Only

FN6310
 Rev 1.00
 September 9, 2009

The ISL22319 integrates a single digitally controlled potentiometer (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

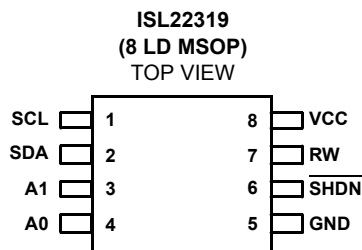
The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I²C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power up the device recalls the content of the DCP's IVR to the WR.

The DCP can be used as a voltage divider in a wide variety of applications including control, parameter adjustments, AC measurement and signal processing.

Features

- 128 resistor taps
- I²C serial interface
 - Two address pins, up to four devices/bus
- Non-volatile storage of wiper position
- Wiper resistance: 70Ω typical @ 3.3V
- Shutdown mode
- Shutdown current 5μA max
- Power supply: 2.7V to 5.5V
- 50kΩ or 10kΩ total resistance
- High reliability
 - Endurance: 1,000,000 data changes per bit per register
 - Register data retention: 50 years @ T ≤ +55 °C
- 8 Ld MSOP
- Pb-free (RoHS compliant)

Pinout

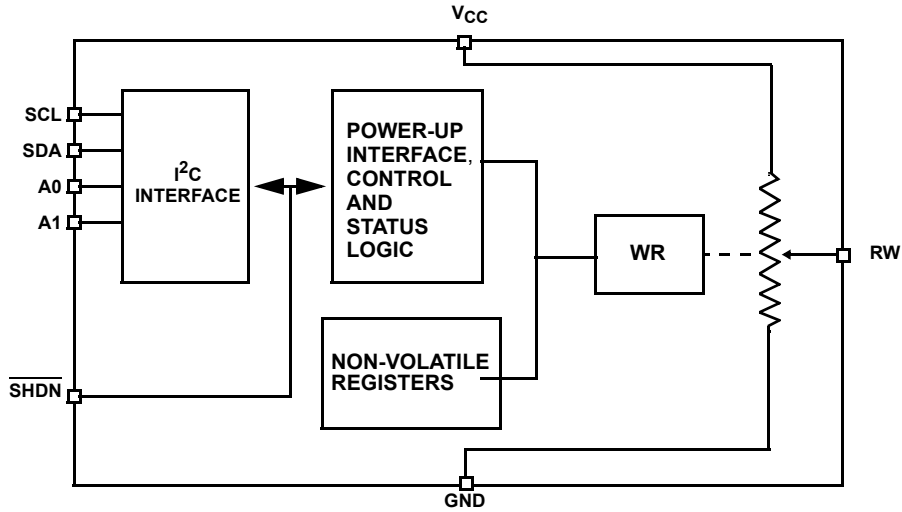


Ordering Information

| PART NUMBER (Note) | PART MARKING | RESISTANCE OPTION (kΩ) | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|-----------------------|--------------|---------------------------|---------------------|----------------------|-------------|
| ISL22319UFU8Z* | 319UZ | 50 | -40 to +125 | 8 Ld MSOP | M8.118 |
| ISL22319WUFU8Z* | 319WZ | 10 | -40 to +125 | 8 Ld MSOP | M8.118 |

*Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
 NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

| MSOP PIN | SYMBOL | DESCRIPTION |
|----------|--------------------------|---|
| 1 | SCL | Open drain I ² C interface clock input |
| 2 | SDA | Open drain serial data I/O for the I ² C interface |
| 3 | A1 | Device address input for the I ² C interface |
| 4 | A0 | Device address input for the I ² C interface |
| 5 | GND | Device ground pin |
| 6 | $\overline{\text{SHDN}}$ | Shutdown active low input |
| 7 | RW | "Wiper" terminal of DCP |
| 8 | V _{CC} | Power supply pin |

Absolute Maximum Ratings

| | |
|---|---------------------------|
| Storage Temperature | -65°C to +150°C |
| Voltage at any Digital Interface Pin with Respect to GND | -0.3V to $V_{CC}+0.3$ |
| V_{CC} | -0.3V to +6V |
| Voltage at any DCP Pin with Respect to GND | -0.3V to V_{CC} |
| I_W (10s) | ±6mA |
| Latchup (Note 2) | Class II, Level B @+125°C |
| ESD Rating | |
| Human Body Model | .5kV |
| Charged Device Model | 1kV |

Thermal Information

| | |
|--|---|
| Thermal Resistance (Typical, Note 1) | θ_{JA} (°C/W) |
| 8 Lead MSOP | 165 |
| Maximum Junction Temperature (Plastic Package) | +150°C |
| Pb-Free Reflow Profile | see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp |

Recommended Operating Conditions

| | |
|---|-----------------|
| Ambient Temperature (Extended Industrial) | -40°C to +125°C |
| V_{CC} Voltage for DCP Operation | 2.7V to 5.5V |
| Wiper Current | -3mA to 3mA |
| Power Rating | .5mW |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the SHDN pin, and using a max negative pulse of -1V for all pins.

Analog Specifications Over recommended operating conditions unless otherwise stated.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 14) | TYP (Note 3) | MAX (Note 14) | UNIT |
|--|-------------------------------------|---|------------------|-----------------|------------------|---------------------|
| R_{TOTAL} | End-to-End Resistance | W option | | 10 | | k Ω |
| | | U option | | 50 | | k Ω |
| | End-to-End Resistance Tolerance | | -20 | | +20 | % |
| | End-to-End Temperature Coefficient | W option | | | ±50 | |
| U option | | | | ±80 | | ppm/°C (Note 12) |
| R_W (Note 12) | Wiper Resistance | $V_{CC} = 3.3V @ +25^\circ C$, wiper current = V_{CC}/R_{TOTAL} | | 70 | | Ω |
| C_W (Note 12) | Wiper Capacitance | | | 25 | | pF |
| I_{LkgRW} | Leakage on RW Pin | Voltage at pin from GND to V_{CC} | | 2 | 4 | μA |
| VOLTAGE DIVIDER MODE (measured at R_W , unloaded) | | | | | | |
| INL (Note 8) | Integral Non-linearity | | -1 | | 1 | LSB (Note 4) |
| DNL (Note 7) | Differential Non-linearity | Monotonic over all tap positions | -0.5 | | 0.5 | LSB (Note 4) |
| ZSerror (Note 5) | Zero-scale Error | W option | 0 | 1 | 5 | LSB (Note 4) |
| | | U option | 0 | 0.5 | 2 | |
| FSerror (Note 6) | Full-scale Error | W option | -5 | -1 | 0 | LSB (Note 4) |
| | | U option | -2 | -1 | 0 | |
| TC_V (Notes 9, 12) | Ratiometric Temperature Coefficient | DCP register set to 40 hex | | ±4 | | ppm/°C |

Operating Specifications Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 14) | TYP (Note 3) | MAX (Note 14) | UNIT |
|-----------------------------------|---|--|------------------|-----------------|------------------|--------|
| I _{CC1} | V _{CC} Supply Current (volatile write/read) | 10k DCP, f _{SCL} = 400kHz; (for I ² C active, read and write states) | | | 1 | mA |
| | V _{CC} Supply Current (volatile write/read, non-volatile read) | 50k DCP, f _{SCL} = 400kHz; (for I ² C active, read and write states) | | | 0.5 | mA |
| I _{CC2} | V _{CC} Supply Current (non-volatile write/read) | 10k DCP, f _{SCL} = 400kHz; (for I ² C active, read and write states) | | | 3.2 | mA |
| | V _{CC} Supply Current (non-volatile write/read) | 50k DCP, f _{SCL} = 400kHz; (for I ² C active, read and write states) | | | 2.7 | mA |
| I _{SB} | V _{CC} Current (standby) | V _{CC} = +5.5V, 10k DCP, I ² C interface in standby state | | | 850 | μA |
| | | V _{CC} = +3.6V, 10k DCP, I ² C interface in standby state | | | 550 | μA |
| | | V _{CC} = +5.5V, 50k DCP, I ² C interface in standby state | | | 160 | μA |
| | | V _{CC} = +3.6V, 50k DCP, I ² C interface in standby state | | | 100 | μA |
| I _{SD} | V _{CC} Current (shutdown) | V _{CC} = +5.5V @ +85°C, I ² C interface in standby state | | | 3 | μA |
| | | V _{CC} = +5.5V @ +125°C, I ² C interface in standby state | | | 5 | μA |
| | | V _{CC} = +3.6V @ +85°C, I ² C interface in standby state | | | 2 | μA |
| | | V _{CC} = +3.6V @ +125°C, I ² C interface in standby state | | | 4 | μA |
| I _{LkgDig} | Leakage Current, at Pins A0, A1, SHDN, SDA, and SCL | Voltage at pin from GND to V _{CC} | -1 | | 1 | μA |
| t _{DCP} (Note 12) | DCP Wiper Response Time | SCL falling edge of last bit of DCP data byte to wiper new position | | 1.5 | | μs |
| t _{ShdnRec} (Note 12) | DCP Recall Time from Shutdown Mode | From rising edge of $\overline{\text{SHDN}}$ signal to wiper stored position and RH connection | | 1.5 | | μs |
| | | SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection | | 1.5 | | μs |
| V _{por} | Power-on Recall Voltage | Minimum V _{CC} at which memory recall occurs | 2.0 | | 2.6 | V |
| V _{CC} Ramp | V _{CC} Ramp Rate | | 0.2 | | | V/ms |
| t _D | Power-up Delay | V _{CC} above V _{por} , to DCP Initial Value Register recall completed, and I ² C Interface in standby state | | | 3 | ms |
| EEPROM SPECIFICATION | | | | | | |
| | EEPROM Endurance | | 1,000,000 | | | Cycles |
| | EEPROM Retention | Temperature T ≤ +55°C | 50 | | | Years |
| t _{WC} (Note 13) | Non-volatile Write Cycle Time | | | 12 | 20 | ms |

Operating Specifications Over the recommended operating conditions unless otherwise specified. (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 14) | TYP (Note 3) | MAX (Note 14) | UNIT |
|-------------------------------|---|--|--------------------------|-----------------|----------------------|------|
| SERIAL INTERFACE SPECS | | | | | | |
| V _{IL} | A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL Input Buffer LOW Voltage | | -0.3 | | 0.3*V _{CC} | V |
| V _{IH} | A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL Input Buffer HIGH Voltage | | 0.7*V _{CC} | | V _{CC} +0.3 | V |
| Hysteresis | SDA and SCL Input Buffer Hysteresis | | 0.05* V _{CC} | | | V |
| V _{OL} | SDA Output Buffer LOW Voltage, Sinking 4mA | | 0 | | 0.4 | V |
| C _{pin} | A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL Pin Capacitance | | | | 10 | pF |
| f _{SCL} | SCL Frequency | | | | 400 | kHz |
| t _{sp} | Pulse Width Suppression Time at SDA and SCL Inputs | Any pulse narrower than the max spec is suppressed | | | 50 | ns |
| t _{AA} | SCL Falling Edge to SDA Output Data Valid | SCL falling edge crossing 30% of V _{CC} , until SDA exits the 30% to 70% of V _{CC} window | | | 900 | ns |
| t _{BUF} | Time the Bus Must be Free before the Start of a New Transmission | SDA crossing 70% of V _{CC} during a STOP condition, to SDA crossing 70% of V _{CC} during the following START condition | 1300 | | | ns |
| t _{LOW} | Clock LOW Time | Measured at the 30% of V _{CC} crossing | 1300 | | | ns |
| t _{HIGH} | Clock HIGH Time | Measured at the 70% of V _{CC} crossing | 600 | | | ns |
| t _{SU:STA} | START Condition Setup Time | SCL rising edge to SDA falling edge; both crossing 70% of V _{CC} | 600 | | | ns |
| t _{HD:STA} | START Condition Hold Time | From SDA falling edge crossing 30% of V _{CC} to SCL falling edge crossing 70% of V _{CC} | 600 | | | ns |
| t _{SU:DAT} | Input Data Setup Time | From SDA exiting the 30% to 70% of V _{CC} window, to SCL rising edge crossing 30% of V _{CC} | 100 | | | ns |
| t _{HD:DAT} | Input Data Hold Time | From SCL rising edge crossing 70% of V _{CC} to SDA entering the 30% to 70% of V _{CC} window | 0 | | | ns |
| t _{SU:STO} | STOP Condition Setup Time | From SCL rising edge crossing 70% of V _{CC} , to SDA rising edge crossing 30% of V _{CC} | 600 | | | ns |
| t _{HD:STO} | STOP Condition Hold Time for Read, or Volatile Only Write | From SDA rising edge to SCL falling edge; both crossing 70% of V _{CC} | 1300 | | | ns |
| t _{DH} | Output Data Hold Time | From SCL falling edge crossing 30% of V _{CC} , until SDA enters the 30% to 70% of V _{CC} window | 0 | | | ns |
| t _R | SDA and SCL Rise Time | From 30% to 70% of V _{CC} | 20 + 0.1*Cb | | 250 | ns |
| t _F | SDA and SCL Fall Time | From 70% to 30% of V _{CC} | 20 + 0.1*Cb | | 250 | ns |
| C _b | Capacitive Loading of SDA or SCL | Total on-chip and off-chip | 10 | | 400 | pF |

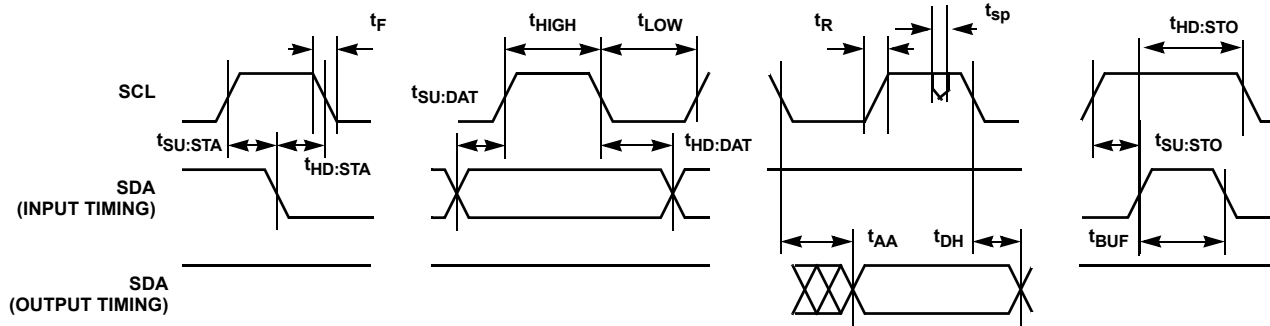
Operating Specifications Over the recommended operating conditions unless otherwise specified. (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 14) | TYP (Note 3) | MAX (Note 14) | UNIT |
|-------------------|---|---|---------------|--------------|---------------|------------------|
| Rpu | SDA and SCL Bus Pull-up Resistor Off-chip | Maximum is determined by t_R and t_F For $C_b = 400\text{pF}$, max is about $2\text{k}\Omega\sim 2.5\text{k}\Omega$ For $C_b = 40\text{pF}$, max is about $15\text{k}\Omega\sim 20\text{k}\Omega$ | 1 | | | $\text{k}\Omega$ |
| $t_{\text{SU:A}}$ | A1 and A0 Setup Time | Before START condition | 600 | | | ns |
| $t_{\text{HD:A}}$ | A1 and A0 Hold Time | After STOP condition | 600 | | | ns |

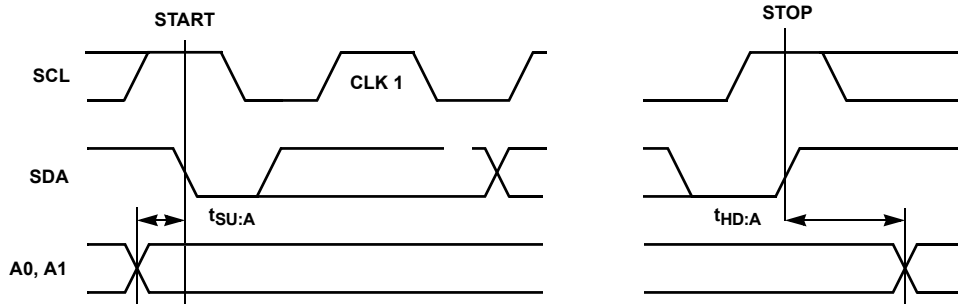
NOTES:

- Typical values are for $T_A = +25^\circ\text{C}$ and 3.3V supply voltage.
- LSB: $[V(RW)_{127} - V(RW)_0]/127$. $V(RW)_{127}$ and $V(RW)_0$ are $V(RW)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
- $Z\text{Serror} = V(RW)_0/\text{LSB}$.
- $F\text{Serror} = [V(RW)_{127} - V_{CC}]/\text{LSB}$.
- $\text{DNL} = [V(RW)_i - V(RW)_{i-1}]/\text{LSB} - 1$, for $i = 1$ to 127. i is the DCP register setting.
- $\text{INL} = [V(RW)_i - (i \cdot \text{LSB}) - V(RW)_0]/\text{LSB}$ for $i = 1$ to 127
- $T_{\text{CV}} = \frac{\text{Max}(V(RW)_i) - \text{Min}(V(RW)_i)}{[\text{Max}(V(RW)_i) + \text{Min}(V(RW)_i)]/2} \times \frac{10^6}{+165^\circ\text{C} \text{ voltage}}$ and $\text{Min}()$ is the minimum value of the wiper voltage over the temperature range.
- $\text{MI} = |RW_{127} - RW_0|/127$. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
- $\text{Roffset} = RW_0/\text{MI}$, when measuring between RW and RL.
 $\text{Roffset} = RW_{127}/\text{MI}$, when measuring between RW and RH.
- This parameter is not 100% tested.
- t_{WC} is the time from a valid STOP condition at the end of a Write sequence of I²C serial interface, to the end of the self-timed internal non-volatile write cycle.
- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ\text{C}$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SDA vs SCL Timing



A0 and A1 Pin Timing



Typical Performance Curves

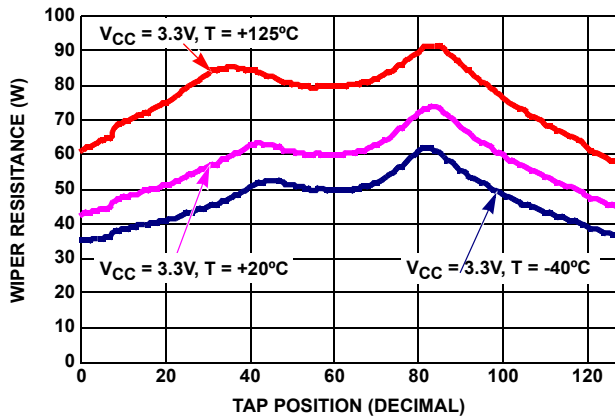


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

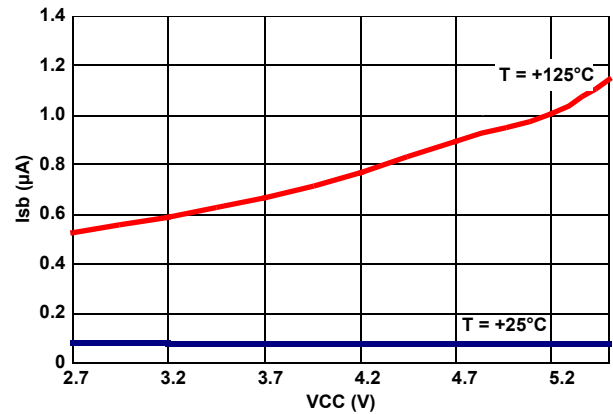


FIGURE 2. STANDBY I_{sb} vs V_{CC}

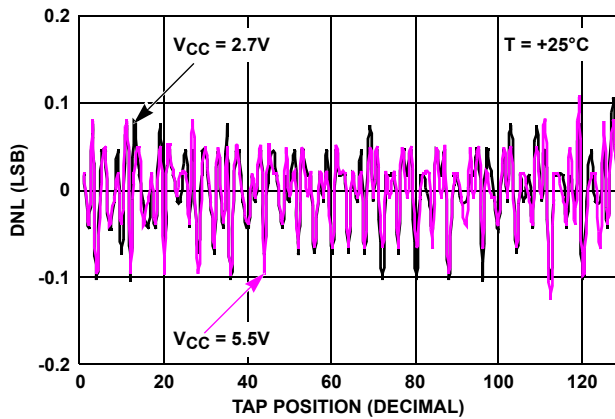


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

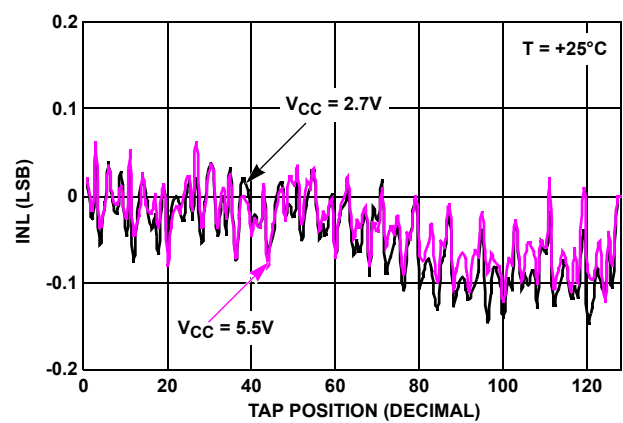


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

Typical Performance Curves (Continued)

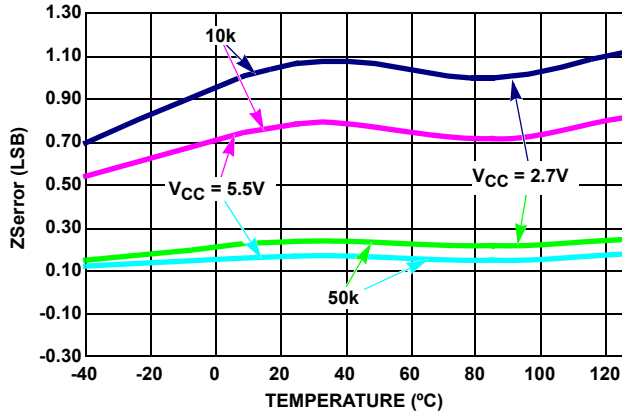


FIGURE 5. ZError vs TEMPERATURE

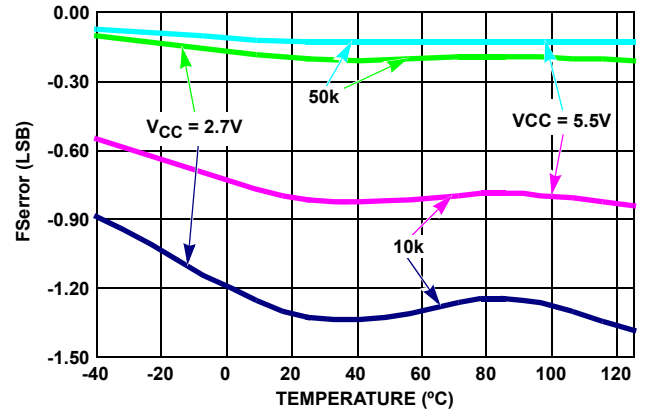


FIGURE 6. FError vs TEMPERATURE

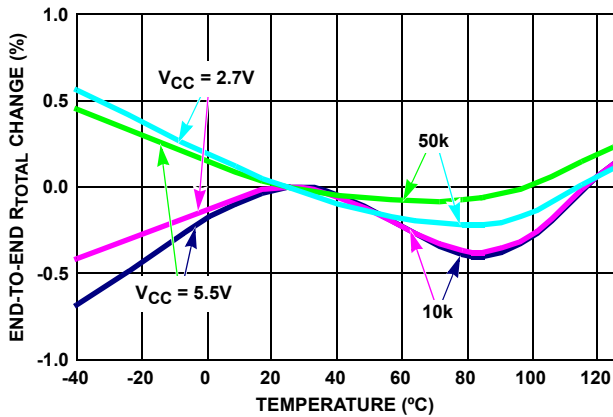


FIGURE 7. END-TO-END R_{TOTAL} % CHANGE vs TEMPERATURE

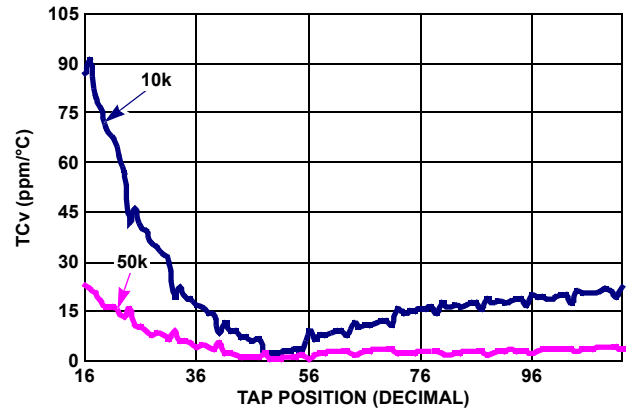


FIGURE 8. TC FOR VOLTAGE DIVIDER MODE IN ppm

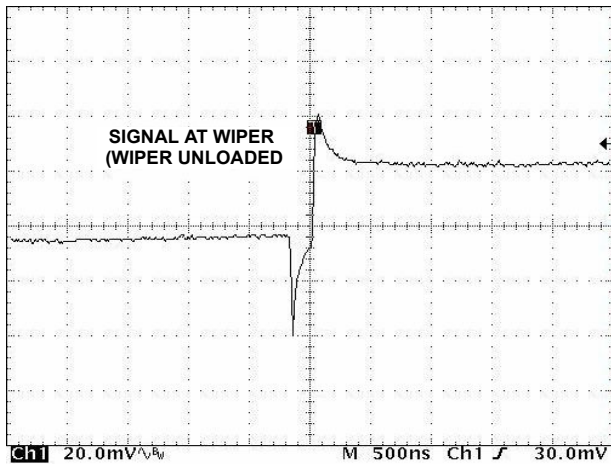


FIGURE 9. MIDSACLE GLITCH, CODE 3Fh TO 40h

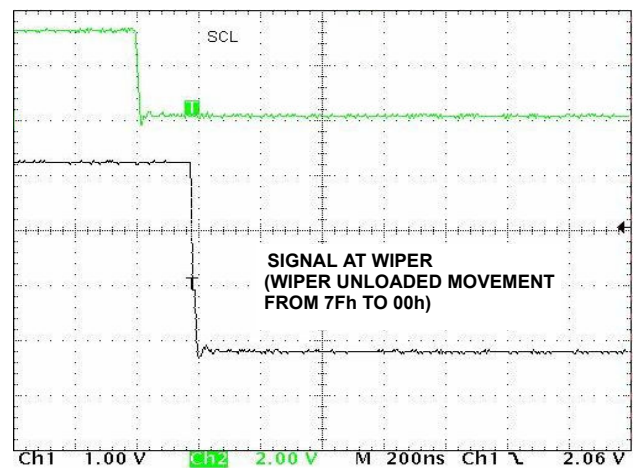


FIGURE 10. LARGE SIGNAL SETTLING TIME

Pin Description

Potentiometers Pins

RW

RW is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

SHDN

The active low $\overline{\text{SHDN}}$ pin forces the resistor to end-to-end open circuit condition and shorts RWi to GND. When $\overline{\text{SHDN}}$ is returned to logic high, the previous latch settings put RW at the same resistance setting prior to shutdown. This pin is logically ANDed with SHDN bit in ACR register. I²C interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation (see Figure 11).

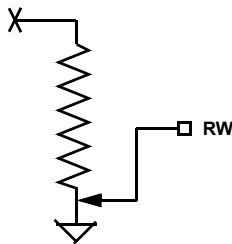


FIGURE 11. DCP CONNECTION IN SHUTDOWN MODE

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for I²C interface. It receives device address, operation code, wiper address and data from an I²C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

SERIAL CLOCK (SCL)

This is the serial clock input of the I²C serial interface. SCL requires an external pull-up resistor, since it is an open drain input.

DEVICE ADDRESS (A1, A0)

The address inputs are used to set the least significant 2 bits of the 7-bit I²C interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL22319. A maximum of 4 ISL22319 devices may occupy the I²C serial bus.

Principles of Operation

The ISL22319 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and an I²C serial interface providing direct communication between a

host and the potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the contents of the IVR is recalled and loaded into the WR to set the wiper to the initial value.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer and internally connected to V_{CC} and GND. The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 7-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR[6:0]= 00h), its wiper terminal (RW) is closest to GND. When the WR register of a DCP contains all ones (WR[6:0] = 7Fh), its wiper terminal (RW) is closest to V_{CC}. As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to GND to the closest to V_{CC}.

While the ISL22319 is being powered up, the WR is reset to 40h (64 decimal), which locates RW roughly at the center between V_{CC} and GND. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reload with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the I²C serial interface as described in the following sections.

Memory Description

The ISL22319 contains one non-volatile 8-bit register, known as the Initial Value Register (IVR), and two volatile 8-bit registers, Wiper Register (WR) and Access Control Register (ACR). The memory map of ISL22319 is on Table 1. The non-volatile register (IVR) at address 0, contains initial wiper position and volatile register (WR) contains current wiper position.

TABLE 1. MEMORY MAP

| ADDRESS | NON-VOLATILE | VOLATILE |
|---------|--------------|----------|
| 2 | — | ACR |
| 1 | Reserved | |
| 0 | IVR | WR |

The non-volatile IVR and volatile WR registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2.

The VOL bit (ACR[7]) determines whether the access is to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

| | | | | | | | |
|-----|------|-----|---|---|---|---|---|
| VOL | SHDN | WIP | 0 | 0 | 0 | 0 | 0 |
|-----|------|-----|---|---|---|---|---|

If VOL bit is 0, the non-volatile IVR register is accessible. If VOL bit is 1, only the volatile WR is accessible. Note, value is written to IVR register also is written to the WR. The default value of this bit is 0.

The SHDN bit (ACR[6]) disables or enables Shutdown mode. This bit is logically ANDed with $\overline{\text{SHDN}}$ pin. When this bit is 0, DCP is in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR[5]) is read only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the WR or ACR while WIP bit is 1.

Shutdown Mode

The device can be put in Shutdown mode either by pulling the $\overline{\text{SHDN}}$ pin to GND or setting the SHDN bit in the ACR register to 0. The truth table for Shutdown mode is in Table 3.

TABLE 3.

| $\overline{\text{SHDN}}$ pin | SHDN bit | Mode |
|------------------------------|----------|------------------|
| High | 1 | Normal operation |
| Low | 1 | Shutdown |
| High | 0 | Shutdown |
| Low | 0 | Shutdown |

I²C Serial Interface

The ISL22319 supports an I²C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22319 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 12). On power-up of the ISL22319 the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22319 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 12). A START condition is ignored during the power-up of the device.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 12). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 13).

The ISL22319 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22319 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is the Read/Write bit. Its value is "1" for a Read operation, and "0" for a Write operation (see Table 4).

TABLE 4. IDENTIFICATION BYTE FORMAT

Logic values at pins A1 and A0 respectively

| | | | | | | | |
|-------|---|---|---|---|----|----|-------|
| 0 | 1 | 0 | 1 | 0 | A1 | A0 | R/W |
| (MSB) | | | | | | | (LSB) |

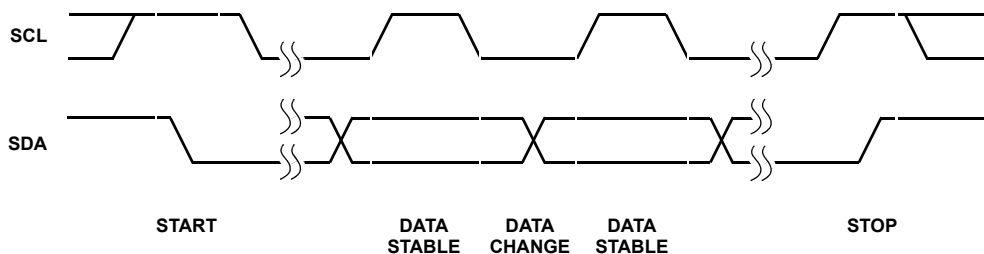


FIGURE 12. VALID DATA CHANGES, START, AND STOP CONDITIONS

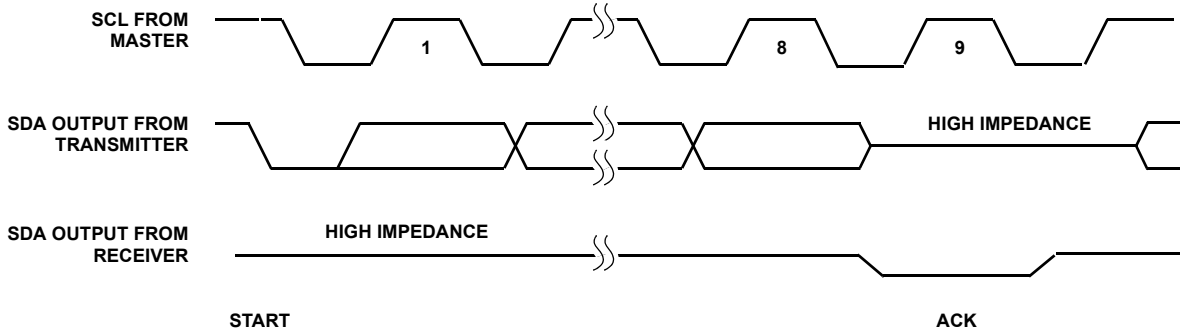


FIGURE 13. ACKNOWLEDGE RESPONSE FROM RECEIVER

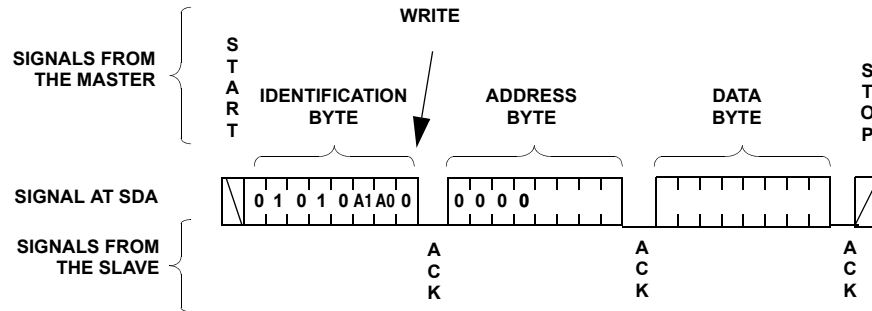


FIGURE 14. BYTE WRITE SEQUENCE

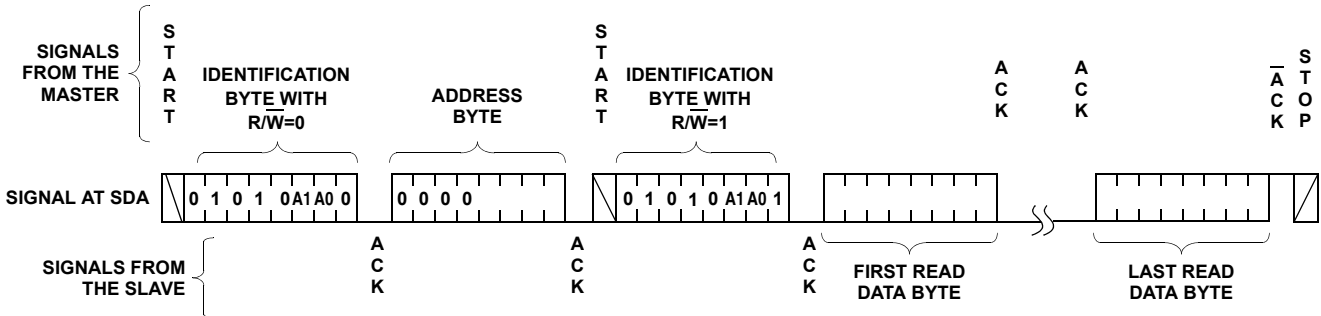


FIGURE 15. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22319 responds with an ACK. At this time, the device enters its standby state (see Figure 14).

The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure15). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/W bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/W bit set to “1”. After each of the three bytes, the ISL22319

responds with an ACK. Then the ISL22319 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a ACK and STOP condition) following the last bit of the last Data Byte (see Figure15).

In order to read back the non-volatile IVR, it is recommended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

Applications Information

The typical application diagram is shown on Figure 16. For proper operation adding 0.1µF decoupling ceramic capacitor to V_{CC} is recommended. The capacitor value may vary based on expected noise frequency of the design.

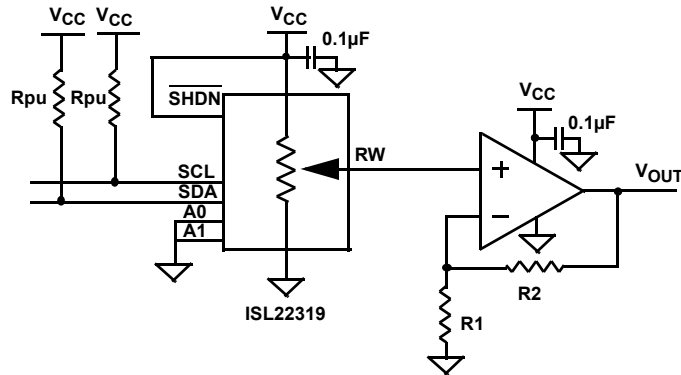


FIGURE 16. TYPICAL APPLICATION DIAGRAM FOR IMPLEMENTING ADJUSTABLE VOLTAGE REFERENCE

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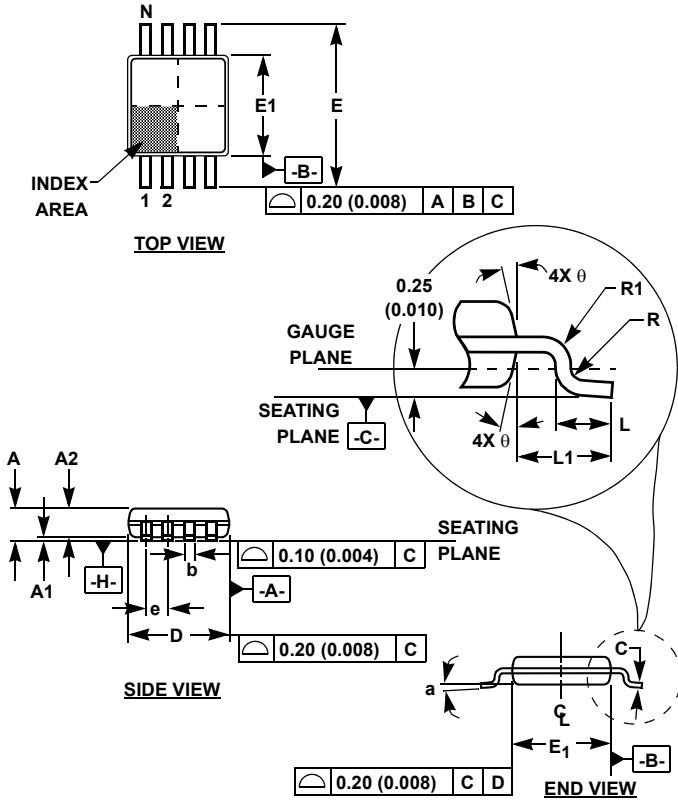
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Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.037 | 0.043 | 0.94 | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 | - |
| b | 0.010 | 0.014 | 0.25 | 0.36 | 9 |
| c | 0.004 | 0.008 | 0.09 | 0.20 | - |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 3 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.187 | 0.199 | 4.75 | 5.05 | - |
| L | 0.016 | 0.028 | 0.40 | 0.70 | 6 |
| L1 | 0.037 REF | | 0.95 REF | | - |
| N | 8 | | 8 | | 7 |
| R | 0.003 | - | 0.07 | - | - |
| R1 | 0.003 | - | 0.07 | - | - |
| θ | 5° | 15° | 5° | 15° | - |
| α | 0° | 6° | 0° | 6° | - |

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. [-H-] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A-] and [-B-] to be determined at Datum plane [-H-].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.