# ISL22349

Quad Digitally Controlled Potentiometers (XDCP™) Low Noise, Low Power, I^{2}C™ Bus, 128 Taps, Wiper Only

The ISL22349 integrates four digitally controlled potentiometers (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^{2}C bus interface. Each potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power up the device recalls the contents of the two DCP's IVR to the corresponding WRs.

The DCPs can be used as a voltage divider in a wide variety of applications including control, parameter adjustments, AC measurement and signal processing.
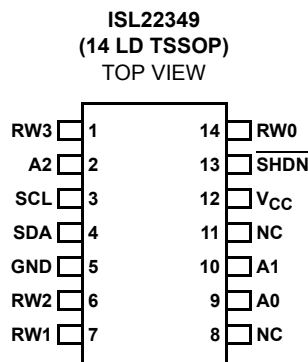
Features

- Four potentiometers in one package

- 128 resistor taps

- I^{2}C serial interface
  - Three address pins, up to eight devices/bus

- Non-volatile storage of wiper position

- Wiper resistance: 70Ω typical

- Shutdown mode

- Shutdown current 6.5µA max

- Power supply: 2.7V to 5.5V

- 50kΩ or 10kΩ total resistance

- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C

- 14 Ld TSSOP

- Pb-free (RoHS compliant)

Pinout

**ISL22349
(14 LD TSSOP)
TOP VIEW**

RW3	1	14	RW0
A2	2	13	$\overline{\text{SHDN}}$
SCL	3	12	V$_{CC}$
SDA	4	11	NC
GND	5	10	A1
RW2	6	9	A0
RW1	7	8	NC

Ordering Information

PART NUMBER (Note)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL22349UFV14Z*	22349 UFVZ	50	-40 to +125	14 Ld TSSOP	M14.173
ISL22349WFV14Z*	22349 WFVZ	10	-40 to +125	14 Ld TSSOP	M14.173

*Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram
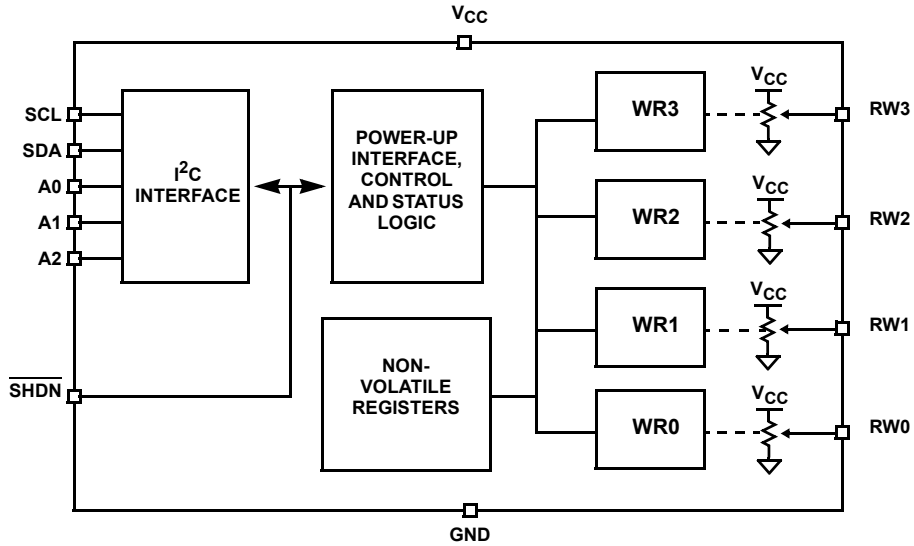
Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	RW3	"Wiper" terminal of DCP3
2	A2	Device address input for the I^2C interface
3	SCL	Open drain I^2C interface clock input
4	SDA	Open drain serial data I/O for the I^2C interface
5	GND	Device ground pin and the RL connection for each DCP
6	RW2	"Wiper" terminal of DCP2
7	RW1	"Wiper" terminal of DCP1
8	NC	
9	A0	Device address input for the I^2C interface
10	A1	Device address input for the I^2C interface
11	NC	
12	V_{CC}	Power supply pin and the RH connection for each DCP
13	$\overline{SHDN}$	Shutdown active low input
14	RW0	"Wiper" terminal of DCP0

Absolute Maximum Ratings

Storage Temperature . . . . -65°C to +150°C
Voltage at any Digital Interface Pin
  with Respect to GND . . . . -0.3V to V_{CC} + 0.3
V_{CC} . . . . -0.3V to +6V
Voltage at any DCP Pin with Respect to GND . . . . -0.3V to V_{CC}
I_W (10s) . . . . ±6mA
Latchup (Note 2) . . . . Class II, Level B @ +125°C
ESD Rating
  Human Body Model 2.5kV
  Charged Device Model 1kV

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
  14 Ld TSSOP package . . . .   +100
Max Junction Temperature (Plastic Package) . .   +50°C to +150°C
Pb-Free Reflow Profile . . . . .see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature . . . . -40°C to +125°C
V_{CC} Voltage for DCP Operation . . . . 2.7V to 5.5V
Wiper Current . . . . -3mA to 3mA
Power Rating 5mW

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

2. Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the SHDN pin, and using a max negative pulse of -0.8V for all pins.

Analog Specifications   Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 13)	TYP (Note 3)	MAX (Note 13)	UNIT
R_{TOTAL}	End-to-End Resistance	W option		10		kΩ
		U option		50		kΩ
	End-to-End Resistance Tolerance	W and U option	-20		+20	%
	End-to-End Temperature Coefficient	W option		±50		ppm/°C (Note 11)
		U option		±80		ppm/°C (Note 11)
R_W (Note 13)	Wiper Resistance	V_{CC} = 3.3V @ +25°C, wiper current = V_{CC}/R_{TOTAL}		70		Ω
C_W (Note 11)	Wiper Capacitance			25		pF
VOLTAGE DIVIDER MODE (measured at R_Wi, unloaded; i = 0, 1, 2, or 3)						
INL (Note 8)	Integral Non-linearity	Monotonic over all tap positions	-1		1	LSB (Note 4)
DNL (Note 7)	Differential Non-linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 4)
ZSerror (Note 5)	Zero-scale Error	W option	0	1	5	LSB (Note 4)
		U option	0	0.5	2	
FSerror (Note 6)	Full-scale Error	W option	-5	-1	0	LSB (Note 4)
		U option	-2	-1	0	
V_{MATCH} (Note 9)	DCP to DCP Matching	Any two DCPs at the same tap position	-2		2	LSB (Note 4)
TC_V (Note 10)	Ratiometric Temperature Coefficient	DCP register set to 40 hex		±4		ppm/°C

ISL22349

Operating Specifications Over the recommended operating conditions unless otherwise specified.

| SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 13)	TYP (Note 3)	MAX (Note 13)	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	V_{CC} = +3.6V, 10k DCP, f_{SCL} = 400kHz; (for I^{2}C active, read and write states)			2.5	mA
	V_{CC} Supply Current (volatile write/read, non-volatile read)	V_{CC} = +3.6V, 50k DCP, f_{SCL} = 400kHz; (for I^{2}C active, read and write states)			0.65	mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	V_{CC} = +5.5V, 10k DCP, f_{SCL} = 400kHz; (for I^{2}C active, read and write states)			4.0	mA
	V_{CC} Supply Current (non-volatile write/read)	V_{CC} = +5.5V, 50k DCP, f_{SCL} = 400kHz; (for I^{2}C active, read and write states)			3.0	mA
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V, 10k DCP, I^{2}C interface in standby state			2.4	mA
		V_{CC} = +3.6V, 10k DCP, I^{2}C interface in standby state			525	µA
		V_{CC} = +5.5V, 50k DCP, I^{2}C interface in standby state			1.6	mA
		V_{CC} = +3.6V, 50k DCP, I^{2}C interface in standby state			350	µA
I_{SD}	V_{CC} Current (shutdown)	V_{CC} = +5.5V @ +85°C, I^{2}C interface in standby state			5	µA
		V_{CC} = +5.5V @ +125°C, I^{2}C interface in standby state			6.5	µA
		V_{CC} = +3.6V @ +85°C, I^{2}C interface in standby state			4	µA
		V_{CC} = +3.6V @ +125°C, I^{2}C interface in standby state			5.5	µA
I_{LkgDig}	Leakage Current, at Pins A0, A1, A2, SHDN, SDA, and SCL	Voltage at pin from GND to V_{CC}	-1		1	µA
t_{WRT} (Note 11)	DCP Wiper Response Time	SCL falling edge of last bit of DCP data byte to wiper new position		1.5		µs
$t_{ShdnRec}$ (Note 11)	DCP Recall Time from Shutdown Mode	From rising edge of SHDN signal to wiper stored position and RH connection		1.5		µs
		SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection		1.5		µs
Vpor	Power-on Recall Voltage	Minimum V_{CC} at which memory recall occurs	2.0		2.6	V
VccRamp	V_{CC} Ramp Rate		0.2			V/ms
t_D	Power-up Delay	Vcc above Vpor, to DCP Initial Value Register recall completed, and I^{2}C Interface in standby state			3	ms
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ +55°C	50			Years
t_{WC} (Note 12)	Non-volatile Write Cycle Time			12	20	ms

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 13)	TYP (Note 3)	MAX (Note 13)	UNIT
SERIAL INTERFACE SPECS						
V_{IL}	A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Input Buffer LOW Voltage		-0.3		$0.3 \cdot V_{CC}$	V
V_{IH}	A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Input Buffer HIGH Voltage		$0.7 \cdot V_{CC}$		$V_{CC} + 0.3$	V
Hysteresis	SDA and SCL Input Buffer Hysteresis		$0.05 \cdot V_{CC}$			V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin (Note 11)	A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Pin Capacitance			10		pF
f_{SCL}	SCL Frequency				400	kHz
t_{sp}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	$20 + 0.1 \cdot Cb$		250	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	$20 + 0.1 \cdot Cb$		250	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2~2.5kΩ For Cb = 40pF, max is about 15~20kΩ	1			kΩ

Operating Specifications   Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 13)	TYP (Note 3)	MAX (Note 13)	UNIT
$t_{SU:A}$	A2, A1 and A0 Setup Time	Before START condition	600			ns
$t_{HD:A}$	A2, A1 and A0 Hold Time	After STOP condition	600			ns

NOTES:

3. Typical values are for T_A = +25°C and 3.3V supply voltage.

4. LSB: $[V(R_W)_{127} - V(R_W)_0]$/127. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.

5. ZS error = $V(RW)_0$/LSB.

6. FS error = $[V(RW)_{127} - V_{CC}]$/LSB.

7. DNL = $[V(RW)_i - V(RW)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.

8. INL = $[V(RW)_i - i \cdot LSB - V(RW)_0]$/LSB for i = 1 to 127.

9. V_{MATCH} = $[V(RWx)_i - V(RWy)_i]$/LSB, for i = 1 to 127, x = 0 to 3 and y = 0 to 3.

10. $TC_V = \dfrac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \dfrac{10^6}{165°C}$ for i = 16 to 112 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper minimum value of the resistance over the temperature range.

11. This parameter is not 100% tested.

12. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of I2C serial interface, to the end of the self-timed internal non-volatile write cycle.

13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SDA vs SCL Timing
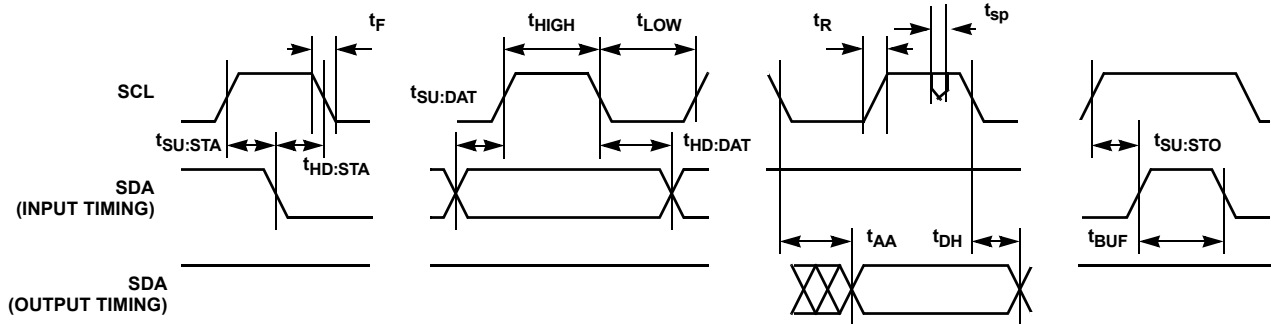
A0, A1, and A2 Pin Timing
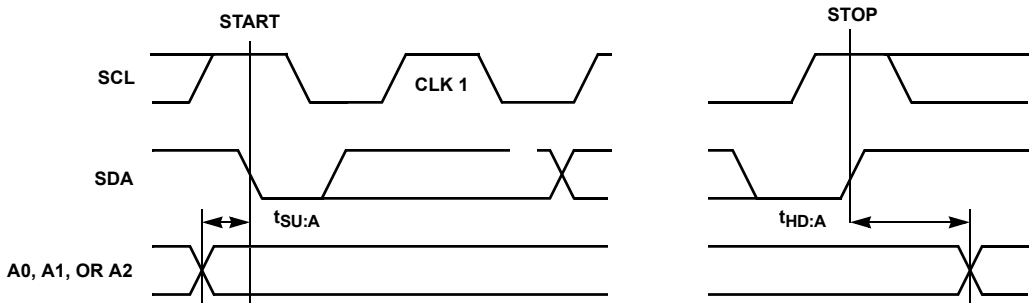
Typical Performance Curves
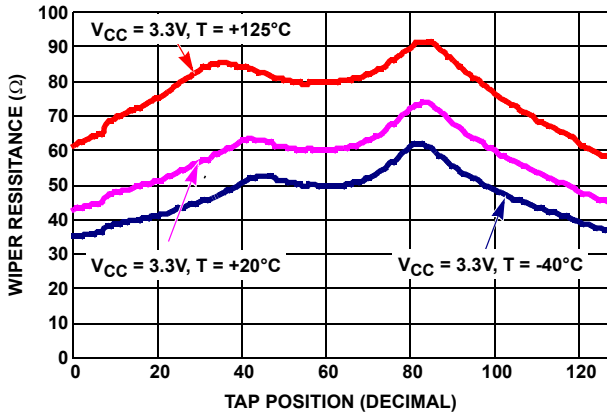
FIGURE 1. WIPER RESISTANCE vs TAP POSITION
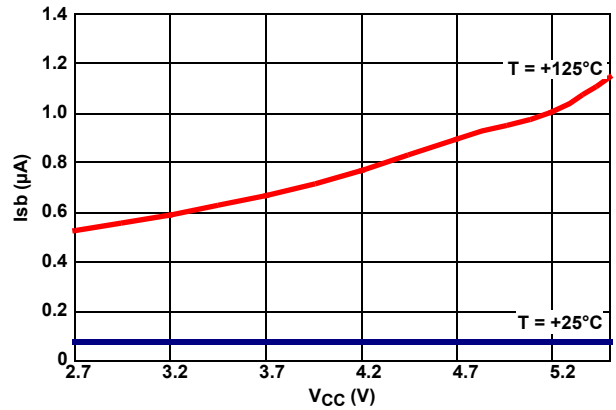[I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

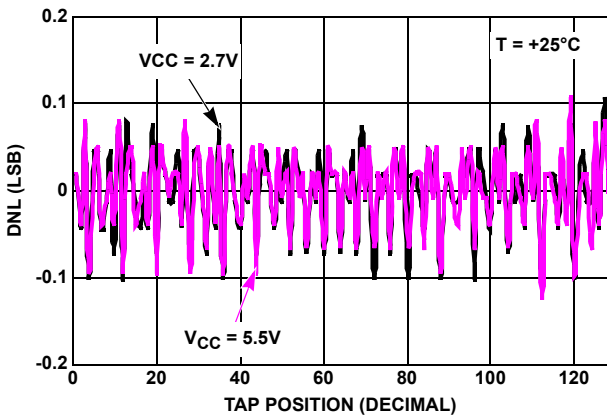FIGURE 2. STANDBY I_{CC} vs V_{CC}

FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER
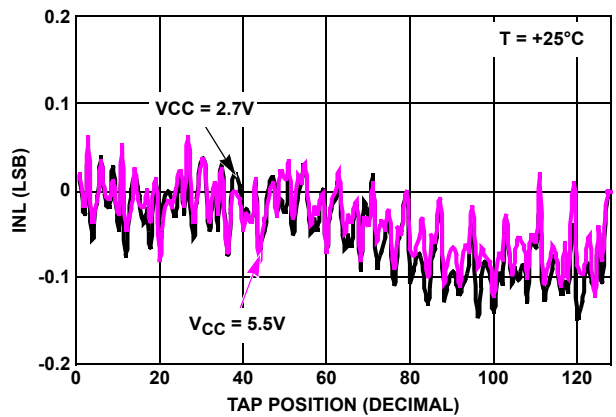MODE FOR 10kΩ (W)

FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER
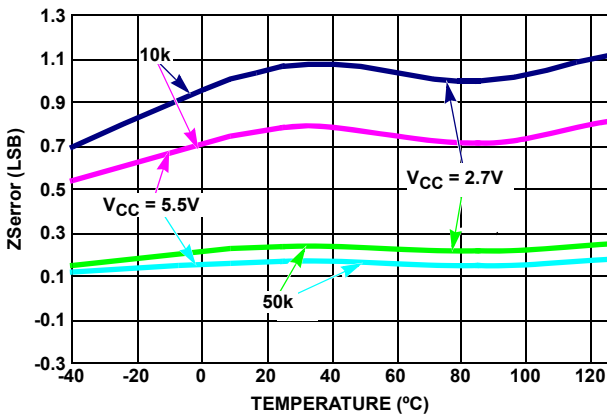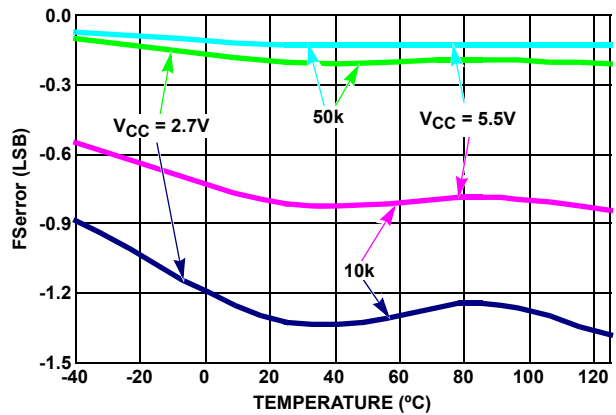MODE FOR 10kΩ (W)

FIGURE 5. ZSerror vs TEMPERATURE

FIGURE 6. FSerror vs TEMPERATURE

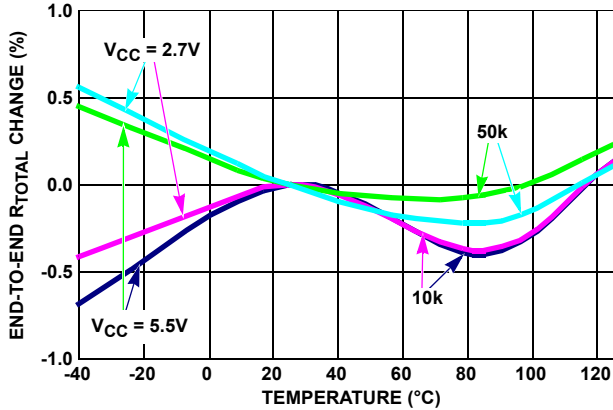## *Typical Performance Curves* (Continued)
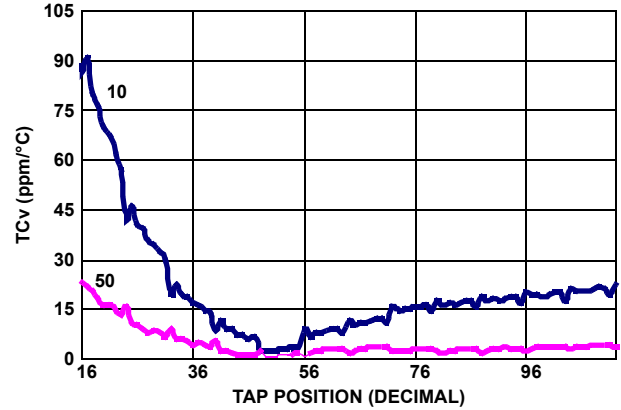

FIGURE 7. END-TO-END R_{TOTAL} % CHANGE vs TEMPERATURE
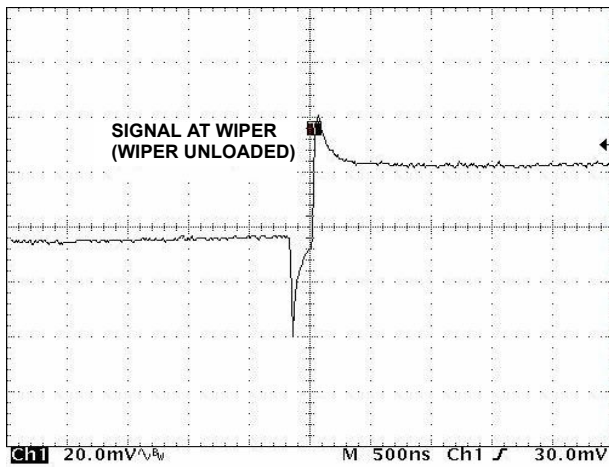

FIGURE 8. TC FOR VOLTAGE DIVIDER MODE IN ppm
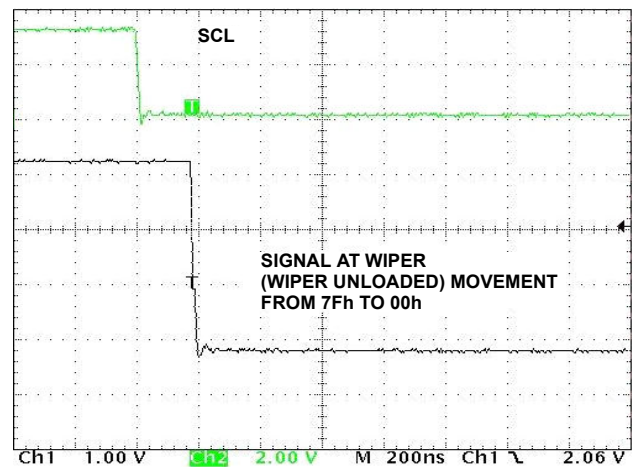

FIGURE 9. MIDSCALE GLITCH, CODE 3Fh TO 40h

FIGURE 10. LARGE SIGNAL SETTLING TIME

Pin Descriptions

Potentiometers Pins

RWI (I = 0, 1, 2 OR 3)

RWi is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

$\overline{SHDN}$

The $\overline{SHDN}$ pin forces the resistor to end-to-end open circuit condition and shorts all RWi to GND. When $\overline{SHDN}$ is returned to logic high, the previous latch settings put RWi at the same resistance setting prior to shutdown. This pin is logically AND with SHDN bit in ACR register. I^{2}C interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation.
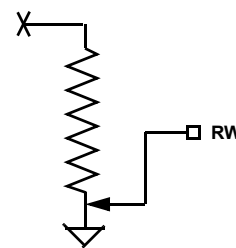

FIGURE 11. DCP CONNECTION IN SHUTDOWN MODE

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for I^{2}C interface. It receives device address, operation code, wiper address and data from an I^{2}C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

SERIAL CLOCK (SCL)

This is the serial clock input of the I^{2}C serial interface. SCL requires an external pull-up resistor, since it is an open drain input.

DEVICE ADDRESS (A2 - A0)

The address inputs are used to set the least significant 3 bits of the 7-bit I^{2}C interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL22349. A maximum of 8 ISL22349 devices may occupy the I^{2}C serial bus.

Principles of Operation

The ISL22349 is an integrated circuit incorporating four DCPs with their associated registers, non-volatile memory and an I^{2}C serial interface providing direct communication between a host and the potentiometers and memory. The resistor arrays are comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a "make before break" mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVRi will be maintained in the non-volatile memory. When power is restored, the contents of the IVRi are recalled and loaded into the corresponding WRi to set the wipers to the initial value.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer and internally connected to Vcc and GND. The RW pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR[6:0] = 00h), its wiper terminal (RW) is closest to GND. When the WR register of a DCP contains all ones (WR[6:0] = 7Fh), its wiper terminal (RW) is closest to V$_{CC}$. As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to GND to the closest to V$_{CC}$.

While the ISL22349 is being powered up, all four WRs are reset to 40h (64 decimal), which locates RW roughly at the center between GND and V$_{CC}$. After the power supply voltage becomes large enough for reliable non-volatile memory reading, all WRs will be reload with the value stored in corresponding non-volatile Initial Value Registers (IVRs).

The WRs can be read or written to directly using the I^{2}C serial interface as described in the following sections. The I^{2}C interface Address Byte has to be set to 00h, 01h, 02h or 03h to access the WR of DCP0, DCP1, DCP2 or DCP3 respectively.

Memory Description

The ISL22349 contains seven non-volatile and five volatile 8-bit registers. The memory map of ISL22349 is on Table 1. The four non-volatile registers (IVRi) at address 0, 1, 2 and 3, contain initial wiper value and volatile registers (WRi) contain current wiper position. In addition, three non-volatile General Purpose registers from address 4 to address 6 are available.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
8	—	ACR
7	Reserved	
6	General Purpose	Not Available
5	General Purpose	Not Available
4	General Purpose	Not Available
3	IVR3	WR3
2	IVR2	WR2
1	IVR1	WR1
0	IVR0	WR0

The non-volatile IVRi and volatile WRi registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2. The VOL bit at access control register (ACR[7]) determines whether the access is to wiper registers WRi or initial value registers IVRi.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

VOL	SHDN	WIP	0	0	0	0	0

If VOL bit is 0, the non-volatile IVRi registers are accessible. If VOL bit is 1, only the volatile WRi are accessible. Note, value is written to IVRi register also is written to the corresponding WRi. The default value of this bit is 0.

The SHDN bit (ACR[6]) disables or enables Shutdown mode. This bit is logically AND with $\overline{\text{SHDN}}$ pin. When this bit is 0, DCPs are in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR[5]) is read only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the WRi or ACR while WIP bit is 1.

Shutdown Mode

The device can be put in Shutdown mode either by pulling the $\overline{\text{SHDN}}$ pin to GND or setting the SHDN bit in the ACR register to 0. The truth table for Shutdown mode is in Table 3.

TABLE 3.

$\overline{\text{SHDN}}$ pin	SHDN bit	Mode
High	1	Normal operation
Low	1	Shutdown
High	0	Shutdown
Low	0	Shutdown

RENESAS

I^2C Serial Interface

The ISL22349 supports an I^2C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22349 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 12). On power-up of the ISL22349 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22349 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met. A START condition is ignored during the power-up of the device.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 12). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 13).

The ISL22349 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22349 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 1010b as the four MSBs, and the following three bits matching the logic values present at pins A2, A1, and A0. The LSB is the Read/Write bit. Its value is "1" for a Read operation, and "0" for a Write operation (see Table 4).

TABLE 4. IDENTIFICATION BYTE FORMAT

Logic values at pins A2, A1, and A0 respectively

1	0	1	0	A2	A1	A0	R/$\overline{W}$

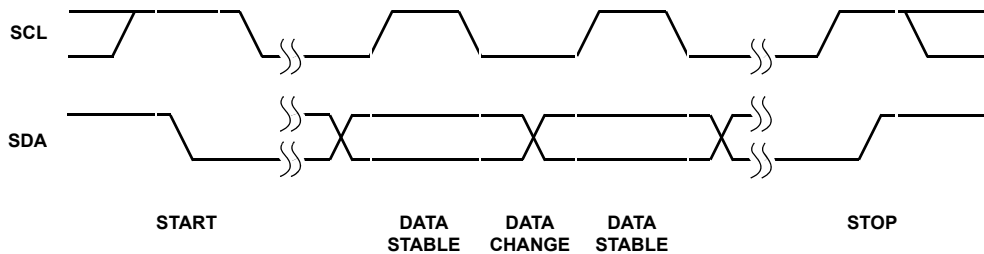(MSB)   (LSB)

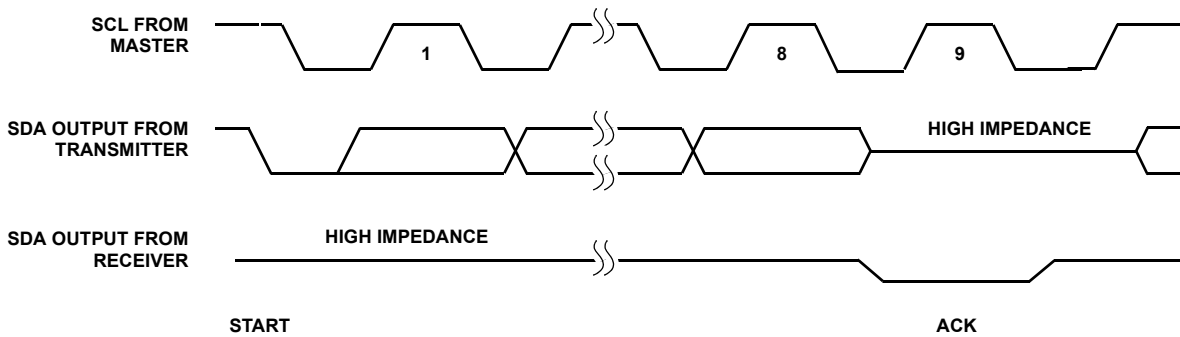FIGURE 12. VALID DATA CHANGES, START AND STOP CONDITIONS

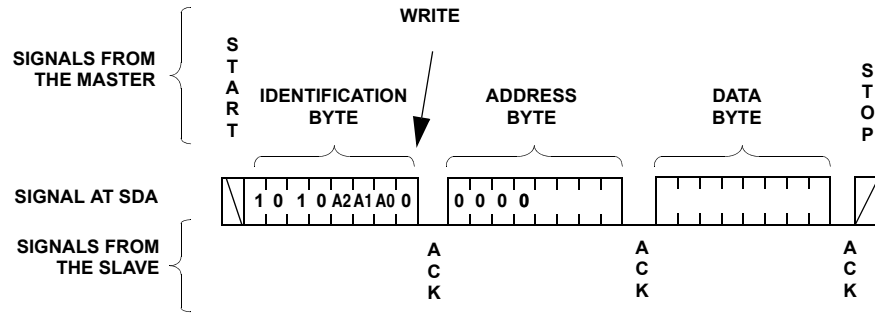FIGURE 13. ACKNOWLEDGE RESPONSE FROM RECEIVER
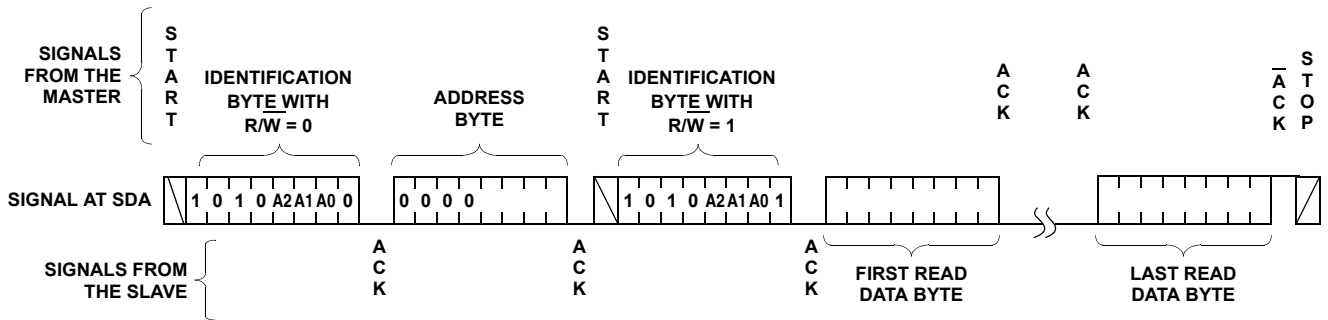
FIGURE 14. BYTE WRITE SEQUENCE

FIGURE 15. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22349 responds with an ACK. At this time, the device enters its standby state (see Figure 14). Device can receive more than one byte of data by auto incrementing the address after each received byte. Note after reaching the address 08h, the internal pointer "rolls over" to address 00h.

The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write. Thus, non-volatile registers must be written individually.

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 15). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the ISL22349 responds with an ACK. Then the ISL22349 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a $\overline{ACK}$ and a STOP condition) following the last bit of the last Data Byte (see Figure 15).

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 08h, the pointer "rolls over" to 00h, and the device continues to output data for each ACK received.

In order to read back the non-volatile IVR, it is recommended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

Thin Shrink Small Outline Plastic Packages (TSSOP)
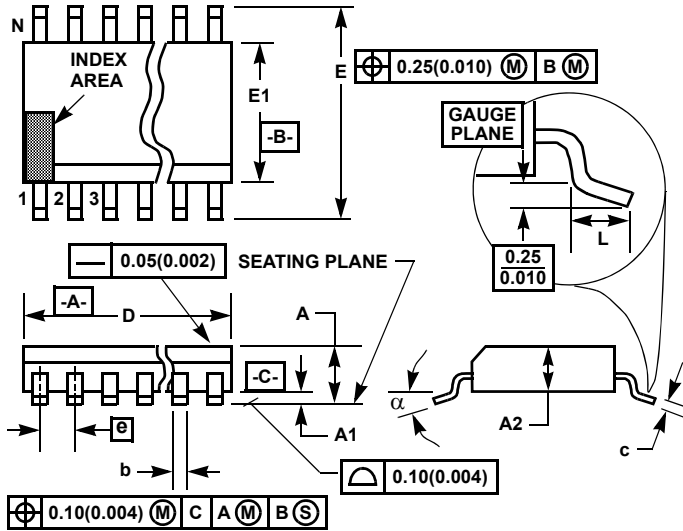
M14.173
14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0°	8°	0°	8°	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

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