

X9315

Low Noise, Low Power, 32 Taps Digitally Controlled Potentiometer (XDCP™)

FN8179
Rev.2.00
December 21, 2009

The Intersil X9315 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the \overline{CS} , $\overline{U/D}$, and \overline{INC} inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

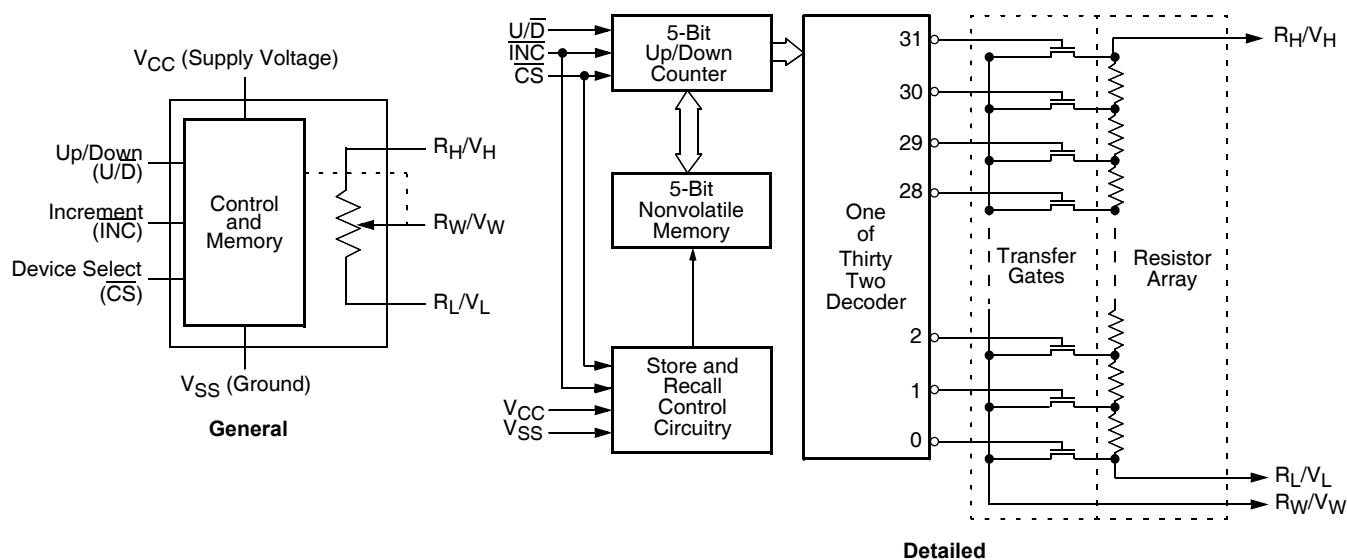
The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Control
- Parameter Adjustments
- Signal Processing

Features

- Solid-state potentiometer
- 3-wire serial interface
- 32 wiper tap points
 - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements
 - Temperature compensated
 - End to end resistance range $\pm 20\%$
 - Terminal voltage, 0 to V_{CC}
- Low power CMOS
 - $V_{CC} = 2.7V$ or $5V$
 - Active current, $80/400\mu A$ max.
 - Standby current, $5\mu A$ max.
- High reliability
 - Endurance, 100,000 data changes per bit
 - Register data retention, 100 years
- R_{TOTAL} values = $10k\Omega$, $50k\Omega$, $100k\Omega$
- Packages
 - 8 Ld SOIC, MSOP and PDIP
- Pb-free available (RoHS compliant)

Block Diagram



Ordering Information

| PART NUMBER | PART MARKING | V _{CC} LIMITS (V) | R _{TOTAL} (kΩ) | TEMP RANGE (°C) | PACKAGE | PKG. DWG. # | | |
|------------------------------|--------------|----------------------------|-------------------------|-----------------|---------------------|-------------|---------------------|--------|
| X9315WMZ (Note 2) | DDT | 5 ±10% | 10 | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 | | |
| X9315WMZT1 (Notes 1, 2) | DDT | | | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 | | |
| X9315WMIT2 (Note 1) | AAX | | | -40 to 85 | 8 Ld MSOP | M8.118 | | |
| X9315WMIZ (Note 2) | AKW | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 | | |
| X9315WMIZT1 (Notes 1, 2) | AKW | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 | | |
| X9315WP | X9315WP | | | 0 to 70 | 8 Ld PDIP | MDP0031 | | |
| X9315WST1 (Note 1) | X9315W | | | 0 to 70 | 8 Ld SOIC | M8.15E | | |
| X9315WSZ (Note 2) | X9315W Z | | | 0 to 70 | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315WSZT1 (Notes 1, 2) | X9315W Z | | | 0 to 70 | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315WSI | X9315W I | | | -40 to 85 | 8 Ld SOIC | M8.15E | | |
| X9315WSIT1 (Note 1) | X9315W I | | | -40 to 85 | 8 Ld SOIC | M8.15E | | |
| X9315WSIZ (Note 2) | X9315W ZI | | | -40 to 85 | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315WSIZT1 (Notes 1, 2) | X9315W ZI | | | -40 to 85 | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315UMZ (Note 2) | DDS | | | 50 | 100 | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 |
| X9315UMZT1 (Notes 1, 2) | DDS | | | | | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 |
| X9315UMI | AEB | | | | | -40 to 85 | 8 Ld MSOP | M8.118 |
| X9315UMIT1 (Notes 1, 2) | AEB | | | | | -40 to 85 | 8 Ld MSOP | M8.118 |
| X9315UMIZ (Note 2) | DDR | | | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 |
| X9315UMIZT1 (Notes 1, 2) | DDR | | | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 |
| X9315UST2 (Note 1) | X9315U | | 0 to 70 | | | 8 Ld SOIC | M8.15E | |
| X9315USZ (Note 2) | X9315U Z | 0 to 70 | 8 Ld SOIC (Pb-free) | | | M8.15 | | |
| X9315USZT1 (Notes 1, 2) | X9315U Z | 0 to 70 | 8 Ld SOIC (Pb-free) | | | M8.15 | | |
| X9315USIZ (Note 2) | X9315U ZI | -40 to 85 | 8 Ld SOIC (Pb-free) | | | M8.15 | | |
| X9315USIZT1 (Notes 1, 2) | X9315U ZI | -40 to 85 | 8 Ld SOIC (Pb-free) | | | M8.15 | | |
| X9315TMZ (Note 2) | DDN | 0 to 70 | 8 Ld MSOP (Pb-free) | | | M8.118 | | |
| X9315TMZT1 (Notes 1, 2) | DDN | 0 to 70 | 8 Ld MSOP (Pb-free) | | | M8.118 | | |
| X9315TMIZ (Note 2) | DDL | -40 to 85 | 8 Ld MSOP (Pb-free) | | | M8.118 | | |
| X9315TMIZT1 (Notes 1, 2) | DDL | -40 to 85 | 8 Ld MSOP (Pb-free) | | | M8.118 | | |
| X9315TSZ (Note 2) | X9315T Z | 0 to 70 | 8 Ld SOIC (Pb-free) | | | M8.15 | | |
| X9315TSZT1 (Notes 1, 2) | X9315T Z | 0 to 70 | 8 Ld SOIC (Pb-free) | | | M8.15 | | |
| X9315TSIZ (Note 2) | X9315T ZI | -40 to 85 | 8 Ld SOIC (Pb-free) | | | M8.15 | | |
| X9315TSIZT1 (Notes 1, 2) | X9315T ZI | -40 to 85 | 8 Ld SOIC (Pb-free) | | | M8.15 | | |
| X9315WMZ-2.7 (Note 2) | AOI | 2.7 to 5.5 | 10 | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 | | |
| X9315WMZ-2.7T1 (Notes 1, 2) | AOI | | | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 | | |
| X9315WMI-2.7T2 (Note 1) | AAV | | | -40 to 85 | 8 Ld MSOP | M8.118 | | |
| X9315WMIZ-2.7 (Note 2) | AKX | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 | | |
| X9315WMIZ-2.7T1 (Notes 1, 2) | AKX | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 | | |
| X9315WS-2.7 | X9315W F | | | 0 to 70 | 8 Ld SOIC | M8.15E | | |

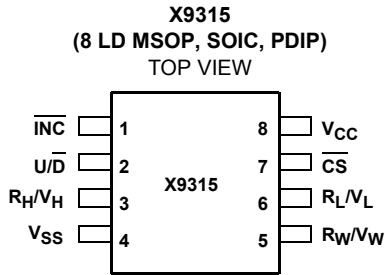
Ordering Information (Continued)

| PART NUMBER | PART MARKING | V _{CC} LIMITS (V) | R _{TOTAL} (kΩ) | TEMP RANGE (°C) | PACKAGE | PKG. DWG. # | |
|------------------------------|--------------|----------------------------|-------------------------|---------------------|---------------------|---------------------|--------|
| X9315WS-2.7T1 (Note 1) | X9315W F | 2.7 to 5.5 | 10 | 0 to 70 | 8 Ld SOIC | M8.15E | |
| X9315WSZ-2.7 (Note 2) | X9315W ZF | | | 0 to 70 | 8 Ld SOIC (Pb-free) | M8.15 | |
| X9315WSZ-2.7T1 (Notes 1, 2) | X9315W ZF | | | 0 to 70 | 8 Ld SOIC (Pb-free) | M8.15 | |
| X9315WSI-2.7T1 (Note 1) | X9315W G | | | -40 to 85 | 8 Ld SOIC | M8.15E | |
| X9315WSIZ-2.7 (Note 2) | X9315W ZG | | | -40 to 85 | 8 Ld SOIC (Pb-free) | M8.15 | |
| X9315WSIZ-2.7T1 (Notes 1, 2) | X9315W ZG | | | -40 to 85 | 8 Ld SOIC (Pb-free) | M8.15 | |
| X9315UMZ-2.7 (Note 2) | AKU | 2.7 to 5.5 | 50 | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 | |
| X9315UMZ-2.7T1 (Notes 1, 2) | AKU | | | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 | |
| X9315UMIZ-2.7 (Note 2) | AJG | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 | |
| X9315UMIZ-2.7T1 (Notes 1, 2) | AJG | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 | |
| X9315US-2.7T2 (Note 1) | X9315U F | | | 0 to 70 | 8 Ld SOIC | M8.15E | |
| X9315USZ-2.7 (Note 2) | X9315U ZF | | | 0 to 70 | 8 Ld SOIC (Pb-free) | M8.15 | |
| X9315USZ-2.7T1 (Notes 1, 2) | X9315U ZF | | 0 to 70 | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315USI-2.7 | X9315U G | | -40 to 85 | 8 Ld SOIC | M8.15E | | |
| X9315USIZ-2.7 (Note 2) | X9315U ZG | | -40 to 85 | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315USIZ-2.7T1 (Notes 1, 2) | X9315U ZG | | -40 to 85 | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315TMZ-2.7 (Note 2) | DDP | | 2.7 to 5.5 | 100 | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 |
| X9315TMZ-2.7T1 (Notes 1, 2) | DDP | | | | 0 to 70 | 8 Ld MSOP (Pb-free) | M8.118 |
| X9315TMI-2.7T1 (Note 1) | ADY | | | | -40 to 85 | 8 Ld MSOP | M8.118 |
| X9315TMIZ-2.7 (Note 2) | DDM | | | | -40 to 85 | 8 Ld MSOP (Pb-free) | M8.118 |
| X9315TMIZ-2.7T1 (Notes 1, 2) | DDM | -40 to 85 | | | 8 Ld MSOP (Pb-free) | M8.118 | |
| X9315TSZ-2.7 (Note 2) | X9315T ZF | 0 to 70 | | | 8 Ld SOIC (Pb-free) | M8.15 | |
| X9315TSZ-2.7T1 (Notes 1, 2) | X9315T ZF | 0 to 70 | | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315TSIZ-2.7 (Note 2) | X9315T ZG | -40 to 85 | | 8 Ld SOIC (Pb-free) | M8.15 | | |
| X9315TSIZ-2.7T1 (Notes 1, 2) | X9315T ZG | -40 to 85 | | 8 Ld SOIC (Pb-free) | M8.15 | | |

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration



Pin Names

| SYMBOL | DESCRIPTION |
|------------------|---------------------------|
| R_H/V_H | High terminal |
| R_W/V_W | Wiper terminal |
| R_L/V_L | Low terminal |
| V_{SS} | Ground |
| V_{CC} | Supply voltage |
| $\overline{U/D}$ | Up/Down control input |
| \overline{INC} | Increment control input |
| \overline{CS} | Chip Select control input |

Pin Description

R_H/V_H and R_L/V_L

The high (R_H/V_H) and low (R_L/V_L) terminals of the X9315 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC} . The terminology of R_L/V_L and R_H/V_H references the relative position of the terminal in relation to wiper movement direction selected by the $\overline{U/D}$ input, and not the voltage potential on the terminal.

R_W/V_W

R_W/V_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200 Ω at $V_{CC} = 5V$.

Up/Down ($\overline{U/D}$)

The $\overline{U/D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment (\overline{INC})

The \overline{INC} input is negative-edge triggered. Toggling \overline{INC} will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the $\overline{U/D}$ input.

Chip Select (\overline{CS})

The device is selected when the \overline{CS} input is LOW. The current counter value is stored in nonvolatile memory when \overline{CS} is returned HIGH while the \overline{INC} input is also HIGH. After the store

operation is complete the X9315 will be placed in the low power standby mode until the device is selected once again.

Principles of Operation

There are three sections of the X9315: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{1W} (\overline{INC} to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The \overline{INC} , $\overline{U/D}$ and \overline{CS} inputs control the movement of the wiper along the resistor array. With \overline{CS} set LOW the device is selected and enabled to respond to the $\overline{U/D}$ and \overline{INC} inputs. HIGH to LOW transitions on \overline{INC} will increment or decrement (depending on the state of the $\overline{U/D}$ input) a five bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever \overline{CS} transitions HIGH while the \overline{INC} input is also HIGH.

The system may select the X9315, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep \overline{INC} LOW while taking \overline{CS} HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments

might be based on user preference, system parameter changes due to temperature drift, etc...

The state of $\overline{U/D}$ may be changed while \overline{CS} remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

| \overline{CS} | \overline{INC} | $\overline{U/D}$ | MODE |
|---|---|------------------|--|
| L |  | H | Wiper up |
| L |  | L | Wiper down |
|  | H | X | Store wiper position to nonvolatile memory |
| H | X | X | Standby |
|  | L | X | No store, return to standby |
|  | L | H | Wiper Up (not recommended) |
|  | L | L | Wiper Down (not recommended) |

Power-up and Down Requirements

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H , V_L , and V_W , i.e., $V_{CC} \geq V_H, V_L, V_W$. The V_{CC} ramp rate spec is always in effect.

Absolute Maximum Ratings

| | |
|--|-----------------|
| Temperature under bias | -65°C to +135°C |
| Storage temperature | -65°C to +150°C |
| Voltage on \overline{CS} , \overline{INC} , U/D, V_H , V_L and V_{CC} with respect to V_{SS} | -1V to +7V |
| $\Delta V = V_H - V_L $ | .5V |
| I_W (10 seconds) | ± 7.5 mA |

Thermal Information

| | | |
|--|---|----------------------|
| Thermal Resistance (Typical, Notes 3, 4) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 8 Ld SOIC | 105 | 68 |
| 8 Ld MSOP | 154 | 58 |
| 8 Ld PDIP | 85 | 57 |
| Pb-Free Reflow Profile | see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp | |

Recommended Operating Conditions

| | |
|---|----------------|
| Temperature (Commercial) | 0°C to +70°C |
| Temperature (Industrial) | -40°C to +85°C |
| Supply Voltage (V_{CC}) (Note 8) Limits | |
| X9315 | 5V \pm 10% |
| X9315-2.7 | 2.7V to 5.5V |
| Max Wiper Current, I_W | ± 3.75 mA |
| Max Power Rating | 10mW |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- For θ_{JC} , the "case temp" location is taken at the package top center.

Potentiometer Characteristics (Over recommended operating conditions unless otherwise stated.)

| SYMBOL | PARAMETER | TEST CONDITIONS/NOTES | LIMITS | | | |
|---------------|-------------------------------------|---|--------------|--------------|--------------|-------------|
| | | | MIN (Note 9) | TYP (Note 8) | MAX (Note 9) | UNIT |
| | End to end resistance tolerance | | -20 | | +20 | % |
| V_{VH} | V_H terminal voltage | | 0 | | V_{CC} | V |
| V_{VL} | V_L terminal voltage | | 0 | | V_{CC} | V |
| R_W | Wiper resistance | $I_W = [V(R_H) - V(R_L)] / R_{TOTAL}$, $V_{CC} = 5V$ | | 200 | 400 | Ω |
| R_W | Wiper resistance | $I_W = [V(R_H) - V(R_L)] / R_{TOTAL}$, $V_{CC} = 2.7V$ | | 400 | 1000 | Ω |
| | Noise | Ref: 1kHz | | -120 | | dBV |
| | Resolution | | | 3 | | % |
| | Absolute linearity (Note 5) | $V_{w(n)(actual)} - V_{w(n)(expected)}$ | | | ± 1 | MI (Note 7) |
| | Relative linearity (Note 6) | $V_{w(n+1)} - [V_{w(n)} + MI]$ | | | ± 0.2 | MI (Note 7) |
| | R_{TOTAL} temperature coefficient | | | ± 300 | | ppm/°C |
| | Ratiometric temperature coefficient | | | ± 20 | | ppm/°C |
| $C_H/C_L/C_W$ | Potentiometer capacitances | See circuit #3 on page 7 | | 10/10/25 | | pF |

NOTES:

- Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $(V_{w(n)(actual)} - V_{w(n)(expected)}) = \pm 1$ MI Maximum.
- Relative linearity is a measure of the error in step size between taps = $R_{W(n+1)} - [R_{W(n)} + MI] = \pm 0.2$ MI.
- 1 MI = Minimum Increment = $R_{TOT}/31$.
- Typical values are for $T_A = +25^\circ\text{C}$ and nominal supply voltage.
- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

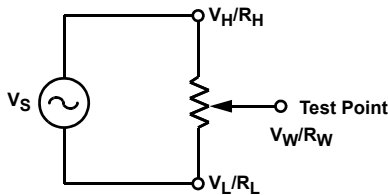
DC Electrical Specifications (Over recommended operating conditions unless otherwise specified.)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|------------------|---|---|-----------------------|--------------|-----------------------|------|
| | | | MIN (Note 9) | TYP (Note 8) | MAX (Note 9) | |
| V _{CC} | Supply Voltage | X9315 | 4.5 | | 5.5 | V |
| | | X9315-2.7 | 2.7 | | 5.5 | V |
| I _{CC1} | V _{CC} active current (Increment) | $\overline{CS} = V_{IL}$, $U/\overline{D} = V_{IL}$ or V_{IH} and $\overline{INC} = 0.4V$ @ max. t _{CYC} | | | 80 | μA |
| I _{CC2} | V _{CC} active current (Store) (EEPROM Store) | $\overline{CS} = V_{IH}$, $U/\overline{D} = V_{IL}$ or V_{IH} and $\overline{INC} = V_{IH}$ @ max. t _{WR} | | | 400 | μA |
| I _{SB} | Standby supply current | $\overline{CS} = V_{CC} - 0.3V$, U/\overline{D} and $\overline{INC} = V_{SS}$ or $V_{CC} - 0.3V$ | | | 5 | μA |
| I _{LI} | \overline{CS} , \overline{INC} , U/\overline{D} input leakage current | V _{IN} = V _{SS} to V _{CC} | -10 | | +10 | μA |
| V _{IH} | \overline{CS} , \overline{INC} , U/\overline{D} input HIGH voltage | | V _{CC} × 0.7 | | V _{CC} + 0.5 | V |
| V _{IL} | \overline{CS} , \overline{INC} , U/\overline{D} input LOW voltage | | -0.5 | | V _{CC} × 0.1 | V |
| C _{IN} | \overline{CS} , \overline{INC} , U/\overline{D} input capacitance | V _{CC} = 5V, V _{IN} = V _{SS} , T _A = +25°C, f = 1MHz | | 10 | | pF |

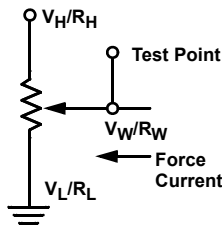
Endurance and Data Retention

| PARAMETER | MIN | UNIT |
|-------------------|---------|----------------------|
| Minimum endurance | 100,000 | Data changes per bit |
| Data retention | 100 | Years |

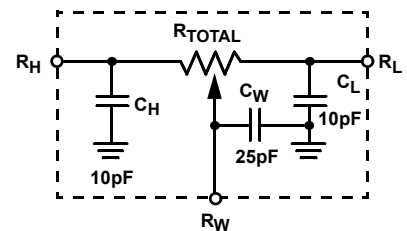
Test Circuit #1



Test Circuit #2



Circuit #3 SPICE Macro Model



AC Conditions of Test

| | |
|---------------------------|----------|
| Input pulse levels | 0V to 3V |
| Input rise and fall times | 10ns |
| Input reference levels | 1.5V |

AC Electrical Specifications (Over recommended operating conditions unless otherwise specified)

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------------|--|--------------|--------------|--------------|------|
| | | MIN (Note 9) | TYP (Note 8) | MAX (Note 9) | |
| t _{CI} | \overline{CS} to \overline{INC} setup | 100 | | | ns |
| t _{DI} | \overline{INC} HIGH to U/\overline{D} change | 100 | | | ns |
| t _{DI} | U/\overline{D} to \overline{INC} setup | 2.9 | | | μs |
| t _{IL} | \overline{INC} LOW period | 1 | | | μs |
| t _{IH} | \overline{INC} HIGH period | 1 | | | μs |

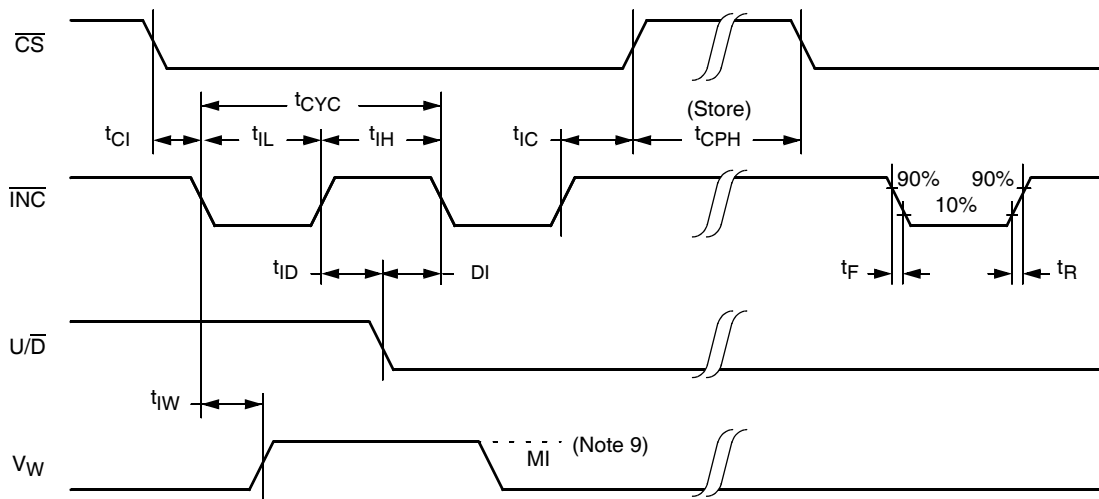
AC Electrical Specifications (Over recommended operating conditions unless otherwise specified) **(Continued)**

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---------------------------|---|--------------|--------------|--------------|---------|
| | | MIN (Note 9) | TYP (Note 8) | MAX (Note 9) | |
| t_{IC} | \overline{INC} Inactive to \overline{CS} inactive | 1 | | | μs |
| t_{CPH} | \overline{CS} Deselect time (NO STORE) | 100 | | | ns |
| t_{CPH} | \overline{CS} Deselect time (STORE) | 10 | | | ms |
| t_{IW} | \overline{INC} to V_W change | | 1 | 5 | μs |
| t_{CYC} | \overline{INC} cycle time | 4 | | | μs |
| t_R, t_F (Note 10) | \overline{INC} input rise and fall time | | | 500 | μs |
| t_{PU} (Note 10) | Power-up to wiper stable | | | 5 | μs |
| $t_R V_{CC}$ (Note 10) | V_{CC} power-up rate | 0.2 | | 50 | V/ms |
| t_{WR} | Store cycle | | 5 | 10 | ms |

NOTE:

10. This parameter is not 100% tested.

AC Timing



NOTE:

11. MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

Symbol Table

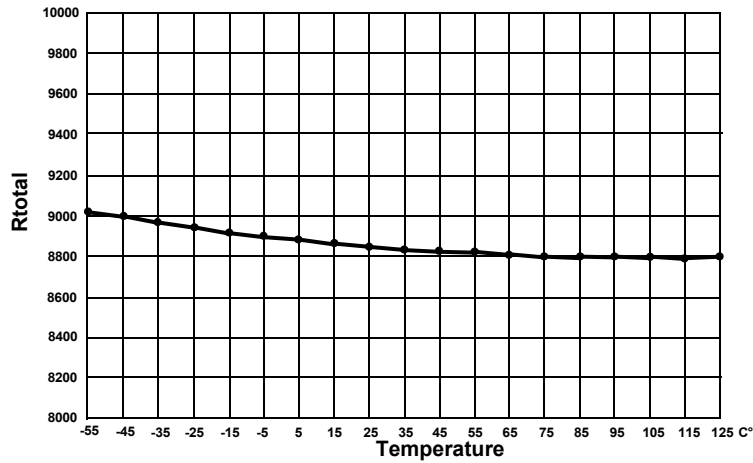
| WAVEFORM | INPUTS | OUTPUTS |
|---|-----------------------------|-------------------------------|
|  | Must be steady | Will be steady |
|  | May change from Low to High | Will change from Low to High |
|  | May change from High to Low | Will change from High to Low |
|  | Don't Care: Changes Allowed | Changing: State Not Known |
|  | N/A | Center Line is High Impedance |

Performance Characteristics (Typical)

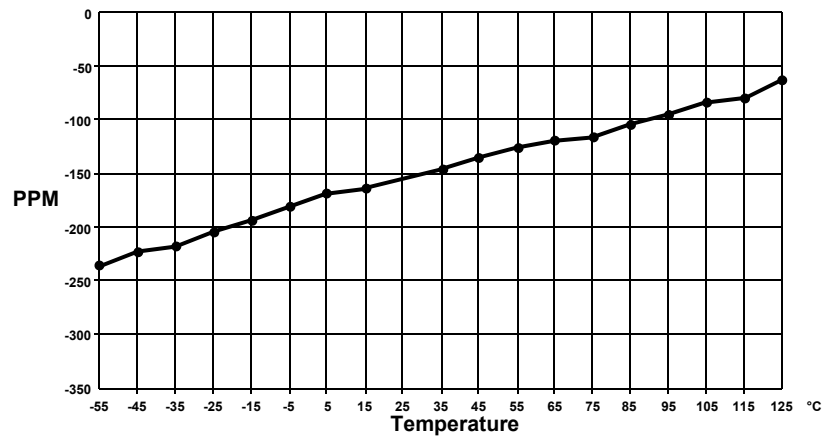
Typical Noise



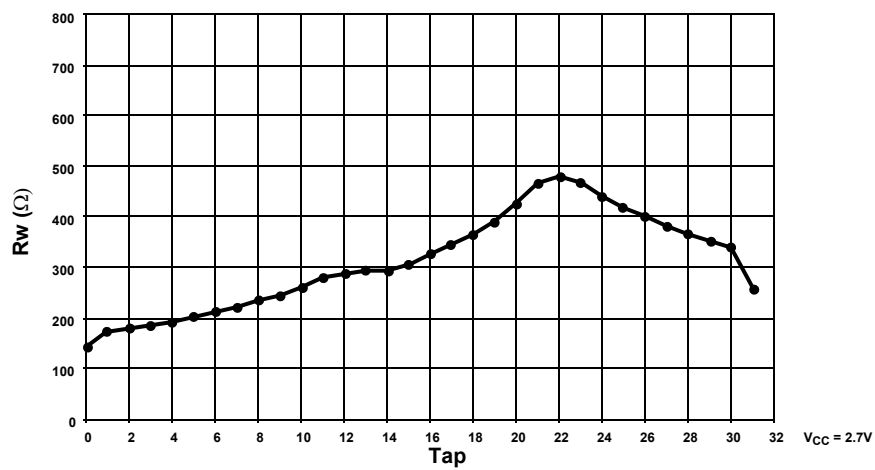
Typical R_{total} vs. Temperature



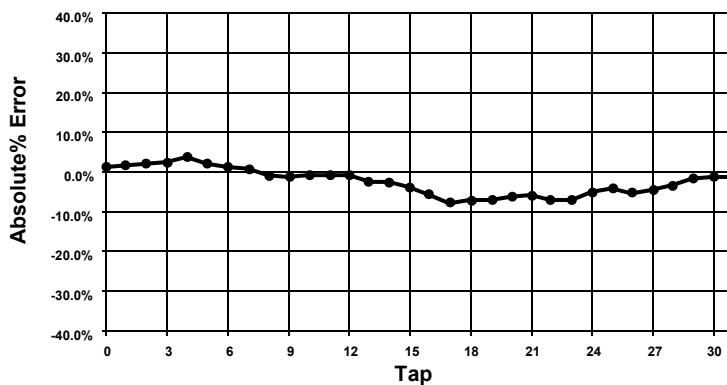
Typical Total Resistance Temperature Coefficient



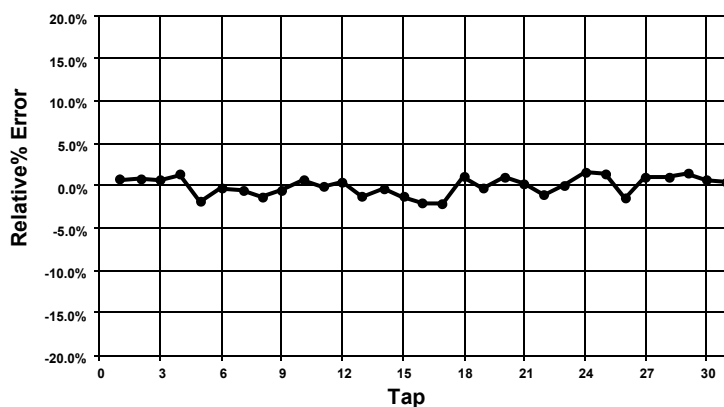
Typical Wiper Resistance



Typical Absolute% Error per Tap Position



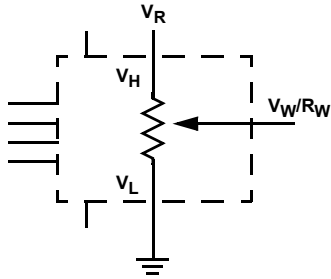
Typical Relative% Error per Tap Position



Applications Information

Electronic digitally controlled (XDCCP) potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers



Three terminal potentiometer; variable voltage divider



Two terminal variable resistor; variable current

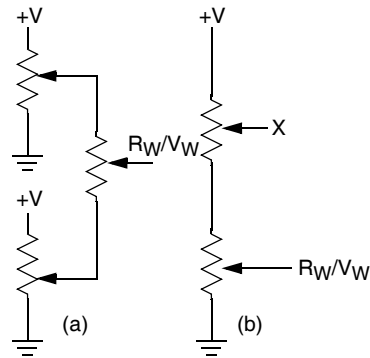
Basic Circuits

Buffered Reference Voltage

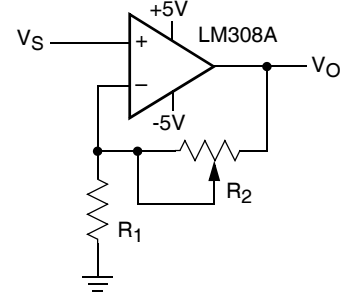


$$V_{OUT} = V_W/R_W$$

Cascading Techniques

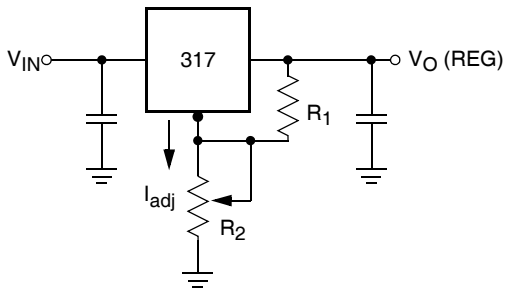


Noninverting Amplifier



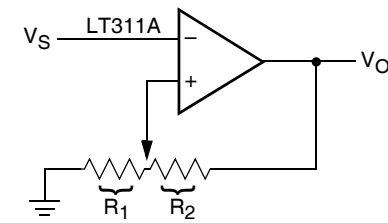
$$V_O = (1 + R_2/R_1)V_S$$

Voltage Regulator



$$V_O (REG) = 1.25V (1 + R_2/R_1) + I_{adj} R_2$$

Comparator with Hysteresis



$$V_{UL} = \{R_1/(R_1 + R_2)\} V_O(max)$$

$$V_{LL} = \{R_1/(R_1 + R_2)\} V_O(min)$$

(for additional circuits see AN115)

Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.037 | 0.043 | 0.94 | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 | - |
| b | 0.010 | 0.014 | 0.25 | 0.36 | 9 |
| c | 0.004 | 0.008 | 0.09 | 0.20 | - |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 3 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.187 | 0.199 | 4.75 | 5.05 | - |
| L | 0.016 | 0.028 | 0.40 | 0.70 | 6 |
| L1 | 0.037 REF | | 0.95 REF | | - |
| N | 8 | | 8 | | 7 |
| R | 0.003 | - | 0.07 | - | - |
| R1 | 0.003 | - | 0.07 | - | - |
| θ | 5° | 15° | 5° | 15° | - |
| α | 0° | 6° | 0° | 6° | - |

Rev. 2 01/03

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. [-H-] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A-] and [-B-] to be determined at Datum plane [-H-].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Package Outline Drawing

M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

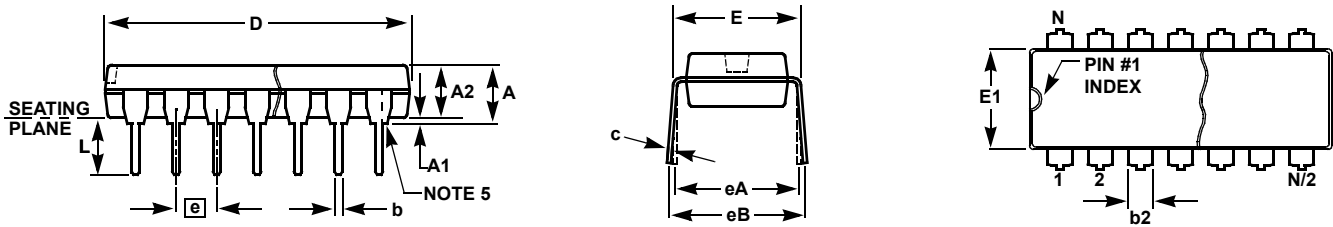
Rev 0, 08/09



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

| SYMBOL | PDIP8 | PDIP14 | PDIP16 | PDIP18 | PDIP20 | TOLERANCE | NOTES |
|--------|-------|--------|--------|--------|--------|---------------|-------|
| A | 0.210 | 0.210 | 0.210 | 0.210 | 0.210 | MAX | |
| A1 | 0.015 | 0.015 | 0.015 | 0.015 | 0.015 | MIN | |
| A2 | 0.130 | 0.130 | 0.130 | 0.130 | 0.130 | ±0.005 | |
| b | 0.018 | 0.018 | 0.018 | 0.018 | 0.018 | ±0.002 | |
| b2 | 0.060 | 0.060 | 0.060 | 0.060 | 0.060 | +0.010/-0.015 | |
| c | 0.010 | 0.010 | 0.010 | 0.010 | 0.010 | +0.004/-0.002 | |
| D | 0.375 | 0.750 | 0.750 | 0.890 | 1.020 | ±0.010 | 1 |
| E | 0.310 | 0.310 | 0.310 | 0.310 | 0.310 | +0.015/-0.010 | |
| E1 | 0.250 | 0.250 | 0.250 | 0.250 | 0.250 | ±0.005 | 2 |
| e | 0.100 | 0.100 | 0.100 | 0.100 | 0.100 | Basic | |
| eA | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | Basic | |
| eB | 0.345 | 0.345 | 0.345 | 0.345 | 0.345 | ±0.025 | |
| L | 0.125 | 0.125 | 0.125 | 0.125 | 0.125 | ±0.010 | |
| N | 8 | 14 | 16 | 18 | 20 | Reference | |

Rev. B 2/99

NOTES:

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

Small Outline Plastic Packages (SOIC)



**M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|-----------|--------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 1 6/05

© Copyright Intersil Americas LLC 2005-2009. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com