X93254

Dual Digitally Controlled Potentiometers (XDCPs™)

FN8186
Rev 1.00
February 4, 2008

The Intersil X93254 is a dual digitally controlled potentiometer (XDCP). The device consists of two resistor arrays, wiper switches, a control section, and nonvolatile memory. The wiper positions are controlled by individual Up/Down interfaces.

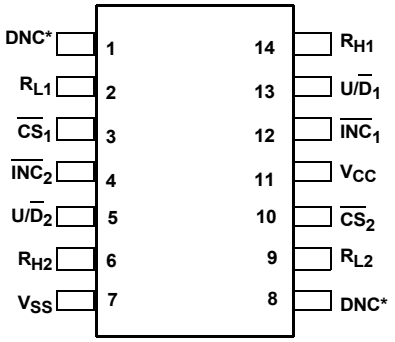
A potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. The position of each wiper element is controlled by a set of independent $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon during a subsequent power-up operation.

Each potentiometer is connected as a two-terminal variable resistor and can be used in a wide variety of applications including:

- Bias and Gain control
- LCD Contrast Adjustment

Pinout

X93254
(14 LD TSSOP)
TOP VIEW



*Do not connect.

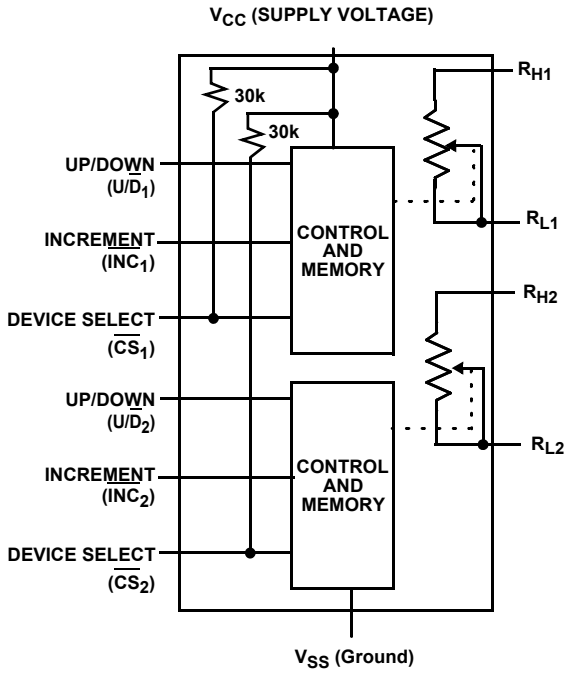
Features

- Dual solid-state potentiometers
- Independent Up/Down interfaces
- 32 wiper tap points per potentiometer
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements per potentiometer
  - Temperature compensated
  - Maximum resistance tolerance of ± 30%
  - Terminal voltage, 0 to V_{CC}
- Low power CMOS
  - V_{CC} = 3V ±10%
  - Active current, 250µA max
  - Standby current, 1µA max
- High reliability
  - Endurance 200,000 data changes per bit
  - Register data retention, 100 years
- R_{TOTAL} value = 50kΩ
- 14 Ld TSSOP package

Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE	PKG DWG. #
X93254UV141-3	X9325 4UVE	3 ±10%	50	-40 to +85	14 Ld TSSOP	M14.173

Block Diagram



Pin Descriptions

TSSOP	SYMBOL	DESCRIPTION
1	DNC	Do Not Connect
2	R_{L1}	**Low Terminal 1**
3	CS_1	**Chip Select 1**
4	$\overline{INC}_2$	**Increment 2**
5	$U/\overline{D}_2$	**Up/Down 2**
6	R_{H2}	**High Terminal 2**
7	V_{SS}	Ground
8	DNC	Do Not Connect
9	R_{L2}	**Low Terminal 2**
10	CS_2	**Chip Select 2**
11	V_{CC}	Supply Voltage
12	$\overline{INC}_1$	**Increment 1**
13	$U/\overline{D}_1$	**Up/Down 1**
14	R_{H1}	**High Terminal 1**

Absolute Maximum Ratings

Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, R_H, R_L and V_{CC}
with respect to V_{SS} . . . . . -1V to +6.5V
Maximum resistor current 2mA

Thermal Information

Temperature under bias. . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Lead temperature (soldering 10s) . . . . . +300°C
Maximum reflow temperature (40s). . . . . +240°C

Recommended Operating Conditions

Temperature Range
Industrial. . . . . -40°C to +85°C
Supply Voltage
V_{CC} . . . . . 3V ±10% (Note 6)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{H(n)}$(actual) - $V_{H(n)}$(expected)) = ±1 MI Maximum. n = 1 .. 29 only
2. Relative linearity is a measure of the error in step size between taps = $V_{H(n+1)}$ - [$V_{H(n)}$ + MI] = ±0.5 MI, n = 1 .. 29 only.
3. 1 MI = Minimum Increment = R_{TOT}/31.
4. Typical values are for T_A = +25°C and nominal supply voltage.
5. Limits established by characterization and are not production tested.
6. When performing multiple write operations, V_{CC} must not decrease by more than 150mV from its initial value.
7. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Potentiometer Specifications

Over recommended operating conditions, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN (Note 7)	TYP (Note 4)	MAX (Note 7)	UNIT
R_{TOT}	End-to-End Resistance		37.5	50	62.5	kΩ
V_R	R_H, R_L Terminal Voltages		0		V_{CC}	V
	Power Rating	R_{TOTAL} = 50kΩ			1	mΩ (Note 5)
	Noise	Ref: 1kHz		-120		dBV (Note 5)
R_W	Wiper Resistance	(Note 5)			1000	Ω
I_W	Wiper Current	(Note 5)			0.6	mA
	Resolution			3		%
	Absolute Linearity (Note 1)	$V_{H(n)(actual)}$ - $V_{H(n)(expected)}$			±1	MI (Note 3)
	Relative Linearity (Note 2)	$V_{H(n+1)}$ - [$V_{H(n)+MI}$			±0.5	MI (Note 3)
	R_{TOTAL} Temperature Coefficient	(Note 5)		±35		ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	See “Circuit #2 SPICE Macro Model” on page 4		10/10/25		pF (Note 5)

DC Operating Specifications

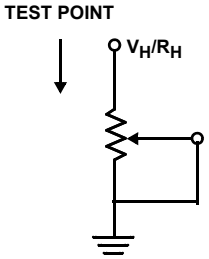
Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN (Note 7)	TYP (Note 4)	MAX (Note 7)	UNIT
I_{CC1}	V_{CC} Active Current (Increment) per DCP	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V @ max. t_{CY}		50	250	µA
I_{CC2}	V_{CC} Active Current (Store) (EEPROM Store) per DCP	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IH} @ max. t_{WR}			600	µA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{CC} - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} - 0.3V			1	µA
I_{LI}	$\overline{CS}_1$ or $\overline{CS}_2$	V_{IN} = V_{CC}			±1	µA
I_{LI}	$\overline{CS}_1$ or $\overline{CS}_2$	V_{CC} = 3V, $\overline{CS}$ = 0	60	100	150	µA
I_{LI}	$\overline{INC}_1$, $\overline{INC}_2$, U/$\overline{D}_1$, U/$\overline{D}_2$ Input Leakage Current	V_{IN} = V_{SS} to V_{CC})			±1	µA
V_{IH}	$\overline{CS}_1$, $\overline{CS}_2$, $\overline{INC}_1$, $\overline{INC}_2$, U/$\overline{D}_1$, U/$\overline{D}_2$ Input HIGH Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	$\overline{CS}_1$, $\overline{CS}_2$, $\overline{INC}_1$, $\overline{INC}_2$, U/$\overline{D}_1$, U/$\overline{D}_2$ Input HIGH Voltage		-0.5		V_{CC} x 0.1	V
C_{IN}	$\overline{CS}_1$, $\overline{CS}_2$, $\overline{INC}_1$, $\overline{INC}_2$, U/$\overline{D}_1$, U/$\overline{D}_2$ Input Capacitance	V_{CC} = 3V, V_{IN} = V_{SS}, T_A = +25°C, f = 1MHz (Note 5)			10	pF

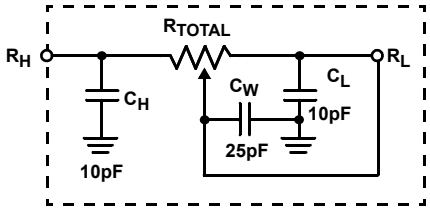
Endurance and Data Retention

PARAMETER	MIN	UNIT
Minimum endurance	200,000	Data changes per bit
Data retention	100	Years

Test Circuit #1



Circuit #2 SPICE Macro Model



AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

AC Operating Specifications

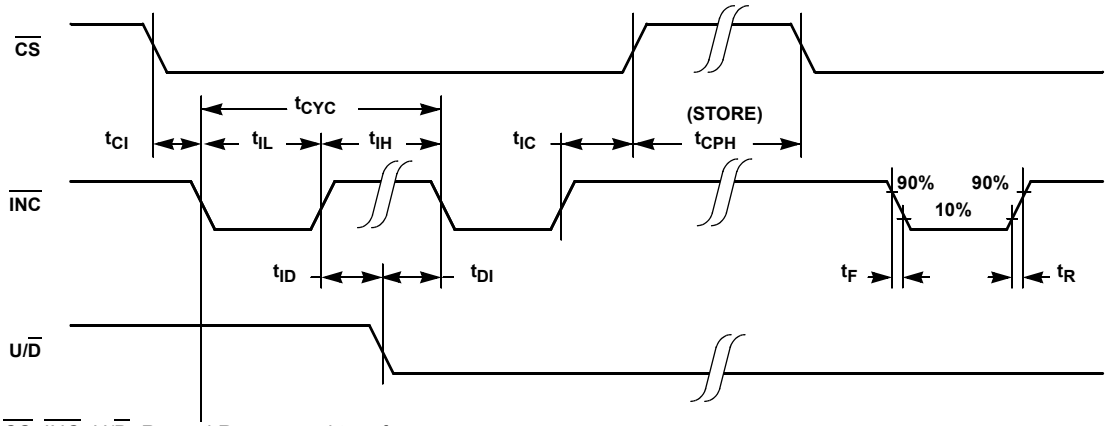
Over recommended operating conditions, unless otherwise stated. $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, R_H and R_L are used to refer to either CS_1 or CS_2, etc.

SYMBOL	PARAMETER	MIN (Note 7)	TYP (Note 4)	MAX (Note 7)	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	100			ns
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect time (No Store)	250			ns
t_{CPH}	$\overline{CS}$ Deselect time (Store)	10			ms

AC Operating Specifications Over recommended operating conditions, unless otherwise stated. $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, R_H and R_L are used to refer to either CS_1 or CS_2, etc. **(Continued)**

SYMBOL	PARAMETER	MIN (Note 7)	TYP (Note 4)	MAX (Note 7)	UNIT
t_{CYC}	$\overline{INC}$ Cycle Time	2			µs
t_R, t_F (Note 5)	$\overline{INC}$ input Rise and Fall Time			500	µs
t_R V_{CC} (Note 5)	V_{CC} Power-up Rate	1		50	V/ms
t_{WR}	Store Cycle		5	10	ms

AC Timing



Note: $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, R_H and R_L are used to refer to either $\overline{CS}_1$ or $\overline{CS}_2$, etc.

Power-up and Power-down Requirements

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H and V_L, i.e., $V_{CC} \geq V_{H,}V_L$. The V_{CC} ramp rate specification is always in effect.

Pin Descriptions

In the text, $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, R_H and R_L are used to refer to either $\overline{CS}_1$ or $\overline{CS}_2$, etc. Note: These signals can be applied independently or at the same time.

R_H and R_L

The R_H and R_L pins of the X93254 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}. The terminology of R_H and R_L references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input per potentiometer.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of a single potentiometer's wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the corresponding potentiometer's counter in the direction indicated by the logic level on the corresponding potentiometer's U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

A potentiometer is selected when the corresponding $\overline{CS}$ input is LOW. Its current counter value is stored in nonvolatile memory when the corresponding $\overline{CS}$ is returned HIGH while the corresponding $\overline{INC}$ input is also HIGH. After the store operation is complete, the affected potentiometer will be placed in the low power standby mode until the potentiometer is selected once again.

Principles of Operation

There are multiple sections for each potentiometer in the X93254: an input control, a counter and decode section; the nonvolatile memory; and a resistor array. Each input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions, the contents of the counter can be stored in nonvolatile memory and retained for future use. Each resistor array is comprised of 31 individual resistors

connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper.

Each wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} (INC to V_W change). The 2-terminal resistance value for the device can temporarily change by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory for each potentiometer. When power is restored, the contents of the memory are recalled and each wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the potentiometer is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a 5-bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever each $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. In order to avoid an accidental store during power-up, each $\overline{CS}$ must go HIGH with V_{CC} during initial power-up. When left open, each $\overline{CS}$ pin is internally pulled up to V_{CC} by an internal 30k resistor.

The system may select the X93254, move any wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data. In order to recall the stored position of the wiper on power-up, the $\overline{CS}$ pin must be held HIGH.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, or other system trim requirements.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move each wiper up and down until the proper trim is attained.

Mode Selection

CS	INC	U/$\overline{D}$	MODE
L	↘	H	Wiper Up
L	↘	L	Wiper Down
↗	H	X	Store Wiper Position
H	X	X	Standby Current
↗	L	X	No Store, Return to Standby
↘	L	H	Wiper Up (not recommended)
↘	L	L	Wiper Down (not recommended)

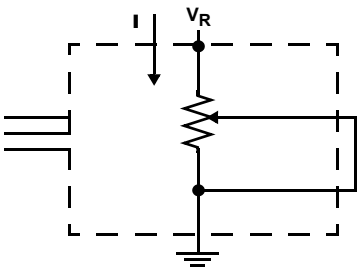
Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Applications Information

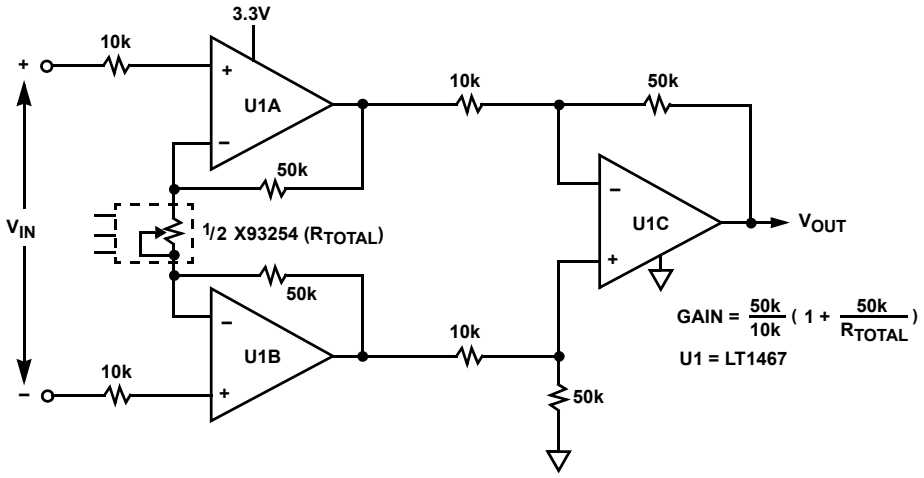
Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages:

1. The variability and reliability of a solid-state potentiometer
2. The flexibility of computer-based digital controls
3. The retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data

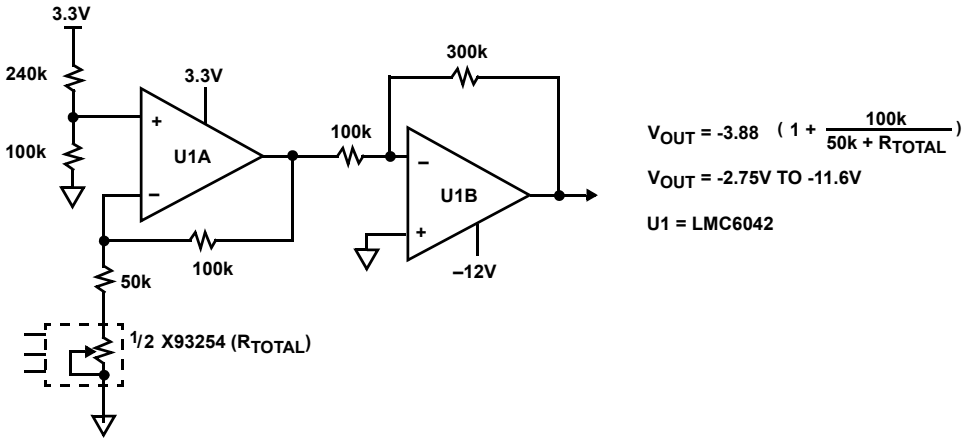


Two terminal variable resistor.
Variable current

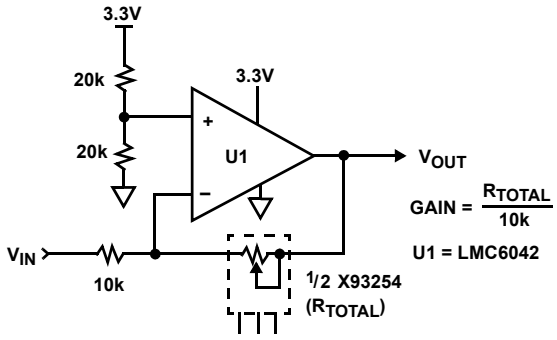
Low Voltage High Impedance Instrumentation Amplifier



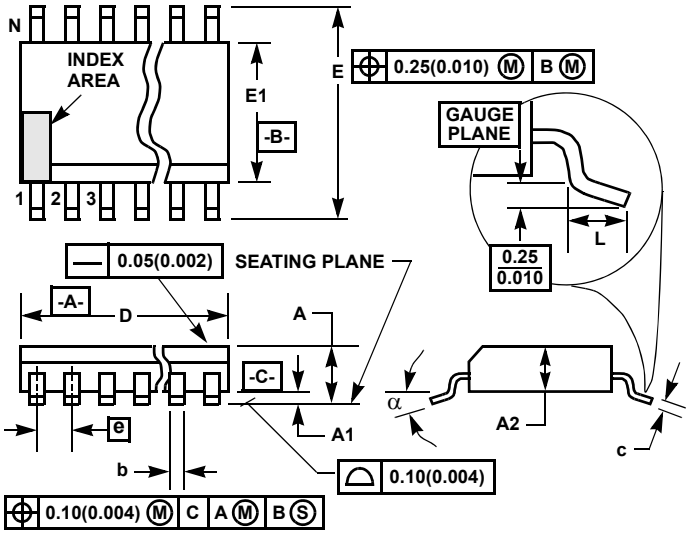
Micro-Power LCD Contrast Control



Single Supply Variable Gain Amplifier



Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0°	8°	0°	8°	-

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