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X9409

Low Noise/Low Power/2-Wire Bus Quad Digitally Controlled Potentiometers (XDCP)

FN8192
Rev.6.00
Sep 3, 2015

The X9409 integrates 4 digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated microcircuit.

The digitally controlled potentiometer is implemented using 63 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and 4 nonvolatile Data Registers (DR0:DR3) that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Power-up recalls the contents of DR0 to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments and signal processing.

Features

- Four potentiometers per package
- 64 resistor taps
- 2-wire serial interface for write, read and transfer operations of the potentiometer
- 50Ω wiper resistance, typical at 5V
- Four nonvolatile data registers for each potentiometer
- Nonvolatile storage of multiple wiper position
- Power-on recall. Loads saved wiper position on power-up standby current < 1µA typical
- System V_{CC}: 2.7V operation
- 10kΩ end-to-end resistance
- 100 year data retention
- Endurance: 100,000 data changes per bit per register
- Low power CMOS
- 24 Ld TSSOP
- Pb-free (RoHS compliant)

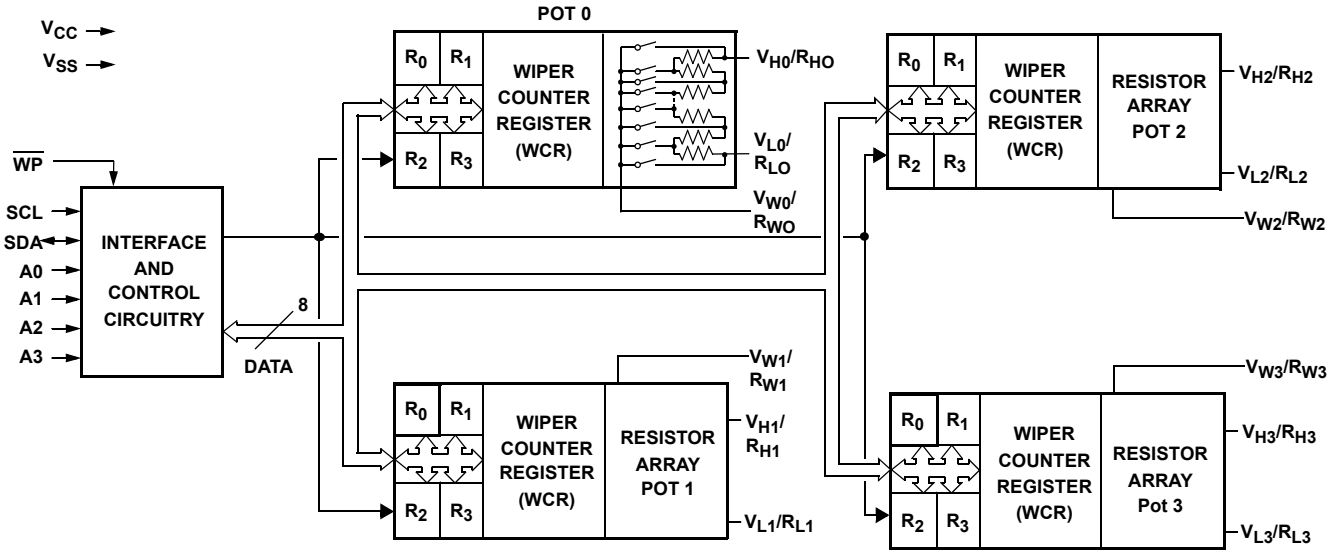


FIGURE 1. BLOCK DIAGRAM

Ordering Information

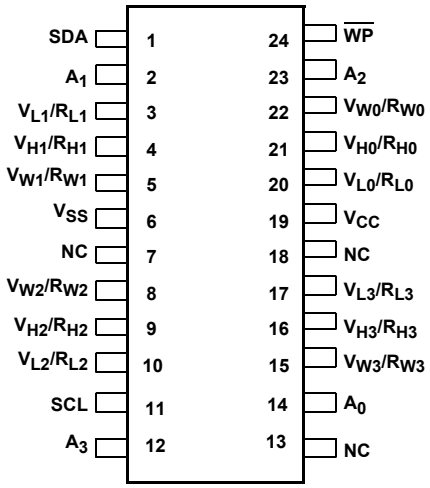
PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
X9409WV24IZ **(No longer available, recommended replacement: X9409WV24IZ-2.7)**	X9409WV ZI	2.7 to 5.5	10	-40 to +85	24 Ld TSSOP (4.4mm)	M24.173
X9409WV24IZ-2.7	X9409WV ZG	2.7 to 5.5	10	-40 to +85	24 Ld TSSOP (4.4mm)	M24.173
X9409WV24Z **(No longer available, recommended replacement: X9409WV24IZ-2.7)**	X9409WV Z	2.7 to 5.5	10	-40 to +85	24 Ld TSSOP (4.4mm)	M24.173
X9409WV24Z-2.7 **(No longer available, recommended replacement: X9409WV24IZ-2.7)**	X9409WV ZF	2.7 to 5.5	10	0 to +70	24 Ld TSSOP (4.4mm)	M24.173

NOTES:

1. Add “T1” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for X9409. For more information on MSL, please see tech brief TB363.

Pin Configuration

X9409
(24 LD TSSOP)
TOP VIEW



Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
11	SCL	Serial Clock
1	SDA	Serial Data
14, 2, 23, 12	A_0, A_1, A_2, A_3	Device Address
21, 4, 9, 16, 20, 3, 10, 17	V_{H0}/R_{H0}, V_{H1}/R_{H1}, V_{H2}/R_{H2}, V_{H3}/R_{H3}, V_{L0}/R_{L0}, V_{L1}/R_{L1}, V_{L2}/R_{L2}, V_{L3}/R_{L3}	Potentiometer Pin (terminal equivalent)
22, 5, 8, 15	V_{W0}/R_{W0}, V_{W1}/R_{W1}, V_{W2}/R_{W2}, V_{W3}/R_{W3}	Potentiometer Pin (wiper equivalent)
24	WP	Hardware Write Protection
19	V_{CC}	System Supply Voltage
6	V_{SS}	System Ground (Digital)
7, 13, 18	NC	No Connection

Host Interface Pins

Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9409.

SERIAL DATA (SDA)

The SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-O Red with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

DEVICE ADDRESS (A_0, A_2, A_3)

The address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9409. A maximum of 16 devices may occupy the 2-wire serial bus.

Potentiometer Pins

V_{H0}/R_{H0} - V_{H3}/R_{H3}, V_{L0}/R_{L0} - V_{L3}/R_{L3}

The V_H/R_H and V_L/R_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_{W0}/R_{W0} - V_{W3}/R_{W3}

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

HARDWARE WRITE PROTECT INPUT ($\overline{WP}$)

The $\overline{WP}$ pin when low prevents nonvolatile writes to the Data Registers.

PRINCIPLES OF OPERATION

The X9409 is a highly integrated microcircuit incorporating four resistor arrays and their associated registers and counters and the serial interface logic providing direct communication between the host and the XDCP potentiometers.

Serial Interface

The X9409 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9409 will be considered a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). The SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

START CONDITION

All commands to the X9409 are preceded by the start condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9409 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

STOP CONDITION

All communications must be terminated by a stop condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH.

ACKNOWLEDGE

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9409 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9409 will respond with a final acknowledge.

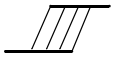
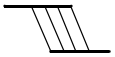
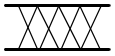
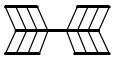
ARRAY DESCRIPTION

The X9409 is comprised of four resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H/R_H and V_L/R_L inputs).

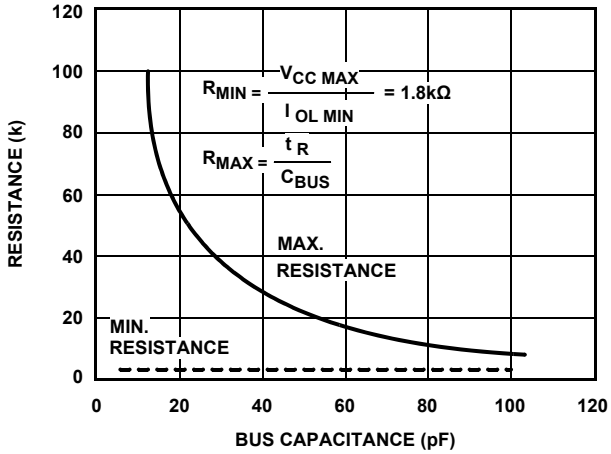
At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (V_W/R_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The 6 bits of the WCR are decoded to select and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated Data Registers into the WCR. These Data Registers and the WCR can be read and written by the host system.

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . 2.7V to 5.5V
Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on SDA, SCL or any address input with respect to V_{SS} . -1V to +7V
$\Delta V = |V_H - V_L|$ 5V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 4kV
Machine Model (Tested per JESD22-A115-A) 300V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld TSSOP (Notes 4, 5)	71	19

Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is taken at the package top center.

Analog Characteristics

Across the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
	End-to-end Resistance Tolerance				±20	%
	Power Rating	+25°C, each pot at 5V, 2.5k			15	mW
I_W	Wiper Current		-3		+3	mA
R_W	Wiper Resistance	I_W = ±3mA, V_{CC} = 3V to 5V		50	150	Ω
V_{TERM}	Voltage On Any V_H/R_H or V_L/R_L pin	V_{SS} = 0V	V_{SS}		V_{CC}	V
	Noise	Ref: 1kHz		-		dBV
	Resolution (Note 10)			1.6		%
	Absolute Linearity (Note 7)	$V_{w(n)(actual)} - V_{w(n)(expected)}$	-1		+1	MI (Note 9)
	Relative Linearity (Note 8)	$V_{w(n+1)} - [V_{w(n)} + MI]$	-0.2		+0.2	MI (Note 9)
	Temperature Coefficient Of R_{TOTAL}			±30		ppm/°C
	Ratiometric Temp. Coefficient				20	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	See macro model		10/		pF
I_{AL}	R_H, R_L, R_W Leakage Current	V_{IN} = V_{SS} to V_{CC}. Device is in stand-by mode.		0.1	10	µA
D.C. OPERATING CHARACTERISTICS						
I_{CC1}	V_{CC} Supply Current (Active)	f_{SCL} = 400kHz, SDA = open, other inputs = V_{SS}			100	µA
I_{CC2}	V_{CC} Supply Current (Nonvolatile Write)	f_{SCL} = 400kHz, SDA = open, other inputs = V_{SS}			1	mA
I_{SB}	V_{CC} Current (Standby)	SCL = SDA = V_{CC}, addr. = V_{SS}			3	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}			10	µA
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		-0.5		V_{CC} x 0.1	V
V_{OL}	Output LOW Voltage	I_{OL} = 3mA			0.4	V
ENDURANCE AND DATA RETENTION						
	Minimum Endurance		100,000			Data changes per bit per register
	Data Retention		100			Years

Analog Characteristics

Across the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CAPACITANCE						
$C_{I/O}$ (Note 10)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V			8	pF
C_{IN} (Note 10)	Input Capacitance (A0, A1, A2, A3 and SCL)	V_{IN} = 0V			6	pF
POWER-UP TIMING						
t_r V_{CC} (Note 11)	V_{CC} Power-Up Rate		0.2		50	V/ms
A.C. TEST CONDITIONS						
	Input Pulse Levels					V_{CC} x 0.1 to V_{CC} x 0.9
	Input Rise and Fall Times					10ns
	Input and Output Timing Level					V_{CC} x 0.5

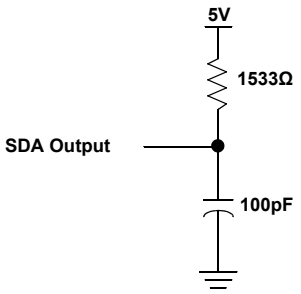


FIGURE 2. EQUIVALENT A.C. LOAD CIRCUIT

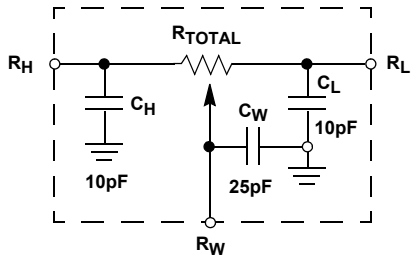


FIGURE 3. CIRCUIT #3 SPICE MACRO MODEL

AC TIMING

Across recommended operating conditions.

SYMBOL	PARAMETER	MIN (Note 6)	MAX (Note 6)	UNITS
f_{SCL}	Clock Frequency		400	kHz
t_{CYC}	Clock Cycle Time	2500		ns
t_{HIGH}	Clock High Time	600		ns
t_{LOW}	Clock Low Time	1300		ns
$t_{SU:STA}$	Start Setup Time	600		ns
$t_{HD:STA}$	Start Hold Time	600		ns
$t_{SU:STO}$	Stop Setup Time	600		ns
$t_{SU:DAT}$	SDA Data Input Setup Time	100		ns
$t_{HD:DAT}$	SDA Data Input Hold Time (Note 12)	30		ns
t_R	SCL and SDA Rise Time		300	ns
t_F	SCL and SDA Fall Time		300	ns
t_{AA}	SCL Low to SDA Data Output Valid Time		900	ns
t_{DH}	SDA Data Output Hold Time	50		ns
T_I	Noise Suppression Time Constant At SCL and SDA Inputs	50		ns
t_{BUF}	Bus Free Time (Prior To Any Transmission)	1300		ns

AC TIMING Across recommended operating conditions. **(Continued)**

SYMBOL	PARAMETER	MIN (Note 6)	MAX (Note 6)	UNITS
$t_{SU:WPA}$	$\overline{WP}$, A0, A1, A2 and A3 Setup Time	0		ns
$t_{HD:WPA}$	$\overline{WP}$, A0, A1, A2 and A3 Hold Time		0	

HIGH-VOLTAGE WRITE CYCLE TIMING

SYMBOL	PARAMETER	TYP	MAX (Note 6)	UNIT
t_{WR}	High-Voltage Write Cycle Time (Store Instructions)	5	10	ms

XDCP TIMING

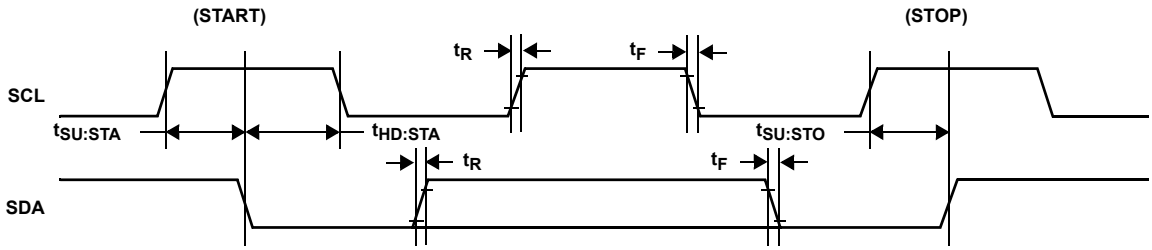
SYMBOL	PARAMETER	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
t_{WRPO}	Wiper Response Time After The Third (Last) Power Supply Is Stable		2	10	µs
t_{WRL}	Wiper Response Time After Instruction Issued (All Load Instructions)		2	10	µs
t_{WRID}	Wiper Response Time From An Active SCL/SCK Edge (Increment/Decrement Instruction)		2	10	µs

NOTES:

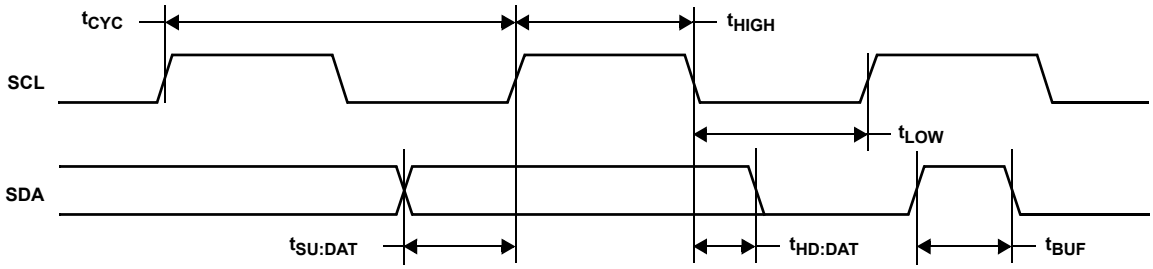
6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
8. Relative Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
9. MI = RTOT/63 or $(V_H - V_L)/63$, single pot.
10. This parameter is periodically sampled and not 100% tested.
11. Sample tested only.
12. A device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

TIMING DIAGRAMS

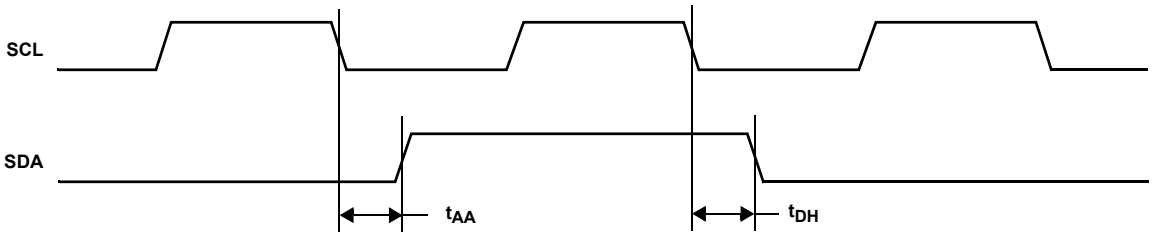
START and STOP Timing



Input Timing



Output Timing



Power-up Requirements

(Power-up sequencing can affect correct recall of the wiper registers)

The preferred power-on sequence is as follows: First V_{CC}, then the potentiometer pins, R_H, R_L and R_W. The V_{CC} ramp rate specification should be met and any glitches or slope changes in the V_{CC} line should be held to <100mV if possible. If V_{CC} powers down, it should be held below 0.1V for more than 1 second before powering up again in order for proper wiper register recall. Also, V_{CC} should not reverse polarity by more than 0.5V. Recall of wiper position will not be complete until V_{CC} reaches its final value.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X9409 this is fixed as 0101[B].

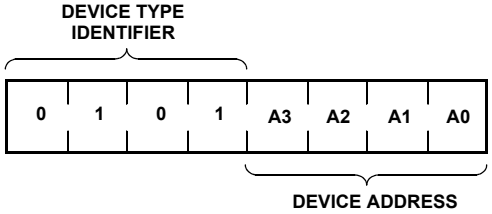


FIGURE 4. SLAVE ADDRESS

The next 4 bits of the slave address are the device address. The physical device address is defined by the state of the A0 through A3 inputs. The X9409 compares the serial data stream with the address input state; a successful compare of all four address bits is required for the X9409 to respond with an acknowledge. The A0 through A3 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

Acknowledge Polling

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical nonvolatile write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9409 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9409 is still busy with the write operation no ACK will be returned. If the X9409 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

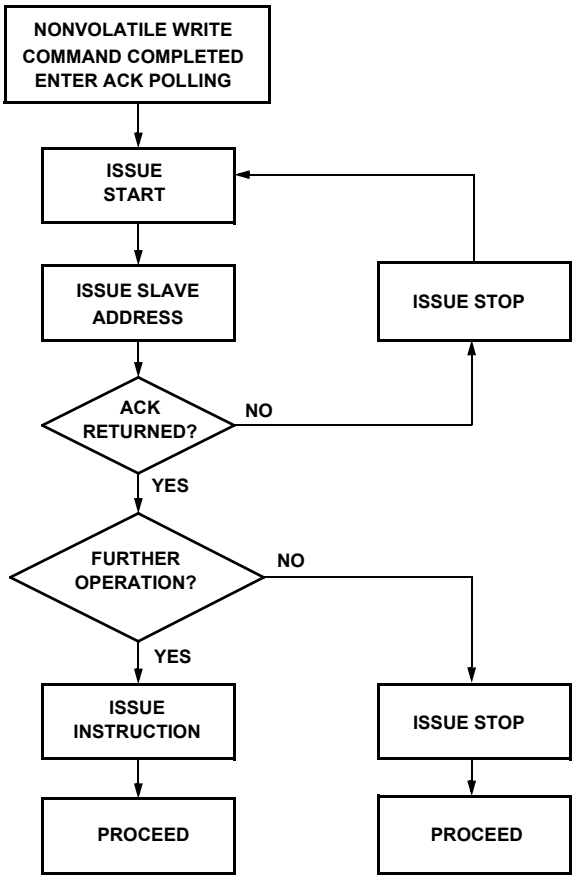


FIGURE 5. ACK POLLING SEQUENCE

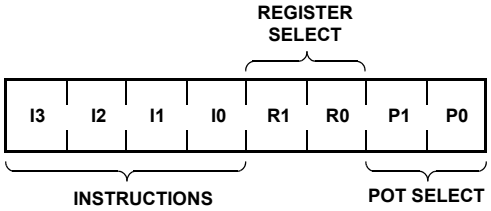


FIGURE 6. INSTRUCTION BYTE FORMAT

Instruction Structure

The next byte sent to the X9409 contains the instruction and register pointer information. The format is shown in Figure 6.

The four high order bits define the instruction. The next 2 bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last bits (P1, P0) select, which one of the four potentiometers is to be affected by the instruction.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 7. These two-byte instructions exchange data between the Wiper Counter Register and one of the data registers. A transfer from a Data Register to a Wiper Counter Register is essentially a write to a static RAM.

The response of the wiper to this action will be delayed t_{WRL}. A transfer from the Wiper Counter Register (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, wherein the transfer occurs between all of the potentiometers and one of their associated registers.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9409; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are: Read Wiper Counter Register (read the current wiper position of the selected pot), Write Wiper Counter Register (change current wiper position of the selected pot), Read Data Register (read the contents of the selected nonvolatile register) and Write Data Register (write a new value to the selected Data Register). The sequence of operations is shown in Table 1.

The Increment/Decrement command is different from the other commands. Once the command is issued and the X9409 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the V_H/R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the V_L/R_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 9 and 10 respectively.

TABLE 1. INSTRUCTION SET

INSTRUCTION	INSTRUCTION SET								OPERATION
	I_3	I_2	I_1	I_0	R_1	R_0	P_1	P_0	
Read Wiper Counter Register	1	0	0	1	0	0	P_1	P_0	Read the contents of the Wiper Counter Register pointed to by P_1 - P_0
Write Wiper Counter Register	1	0	1	0	0	0	P_1	P_0	Write new value to the Wiper Counter Register pointed to by P_1 - P_0
Read Data Register	1	0	1	1	R_1	R_0	P_1	P_0	Read the contents of the Data Register pointed to by P_1 - P_0 and R_1 - R_0
Write Data Register	1	1	0	0	R_1	R_0	P_1	P_0	Write new value to the Data Register pointed to by P_1 - P_0 and R_1 - R_0
XFR Data Register to Wiper Counter Register	1	1	0	1	R_1	R_0	P_1	P_0	Transfer the contents of the Data Register pointed to by P_1 - P_0 and R_1 - R_0 to its associated Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	R_1	R_0	P_1	P_0	Transfer the contents of the Wiper Counter Register pointed to by P_1 - P_0 to the Data Register pointed to by R_1 - R_0
Global XFR Data Registers to Wiper Counter Registers	0	0	0	1	R_1	R_0	0	0	Transfer the contents of the Data Registers pointed to by R_1 - R_0 of all four pots to their respective Wiper Counter Registers
Global XFR Wiper Counter Registers to Data Register	1	0	0	0	R_1	R_0	0	0	Transfer the contents of both Wiper Counter Registers to their respective Data Registers pointed to by R_1 - R_0 of all four pots
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	P_1	P_0	Enable Increment/decrement of the WCR Latch pointed to by P_1 - P_0

NOTE:

13. 1/0 = data is one or zero

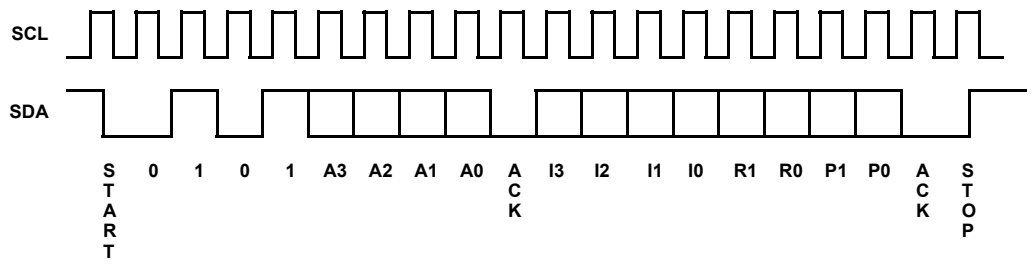


FIGURE 7. 2-BYTE INSTRUCTION SEQUENCE

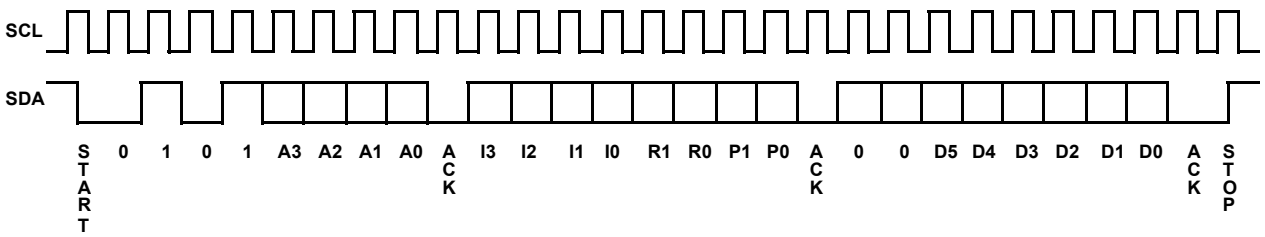


FIGURE 8. 10-BYTE INSTRUCTION SEQUENCE

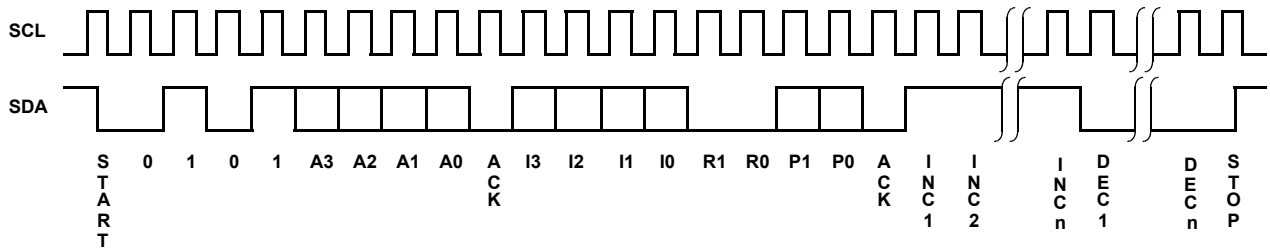


FIGURE 9. INCREMENT/ DECREMENT INSTRUCTION SEQUENCE

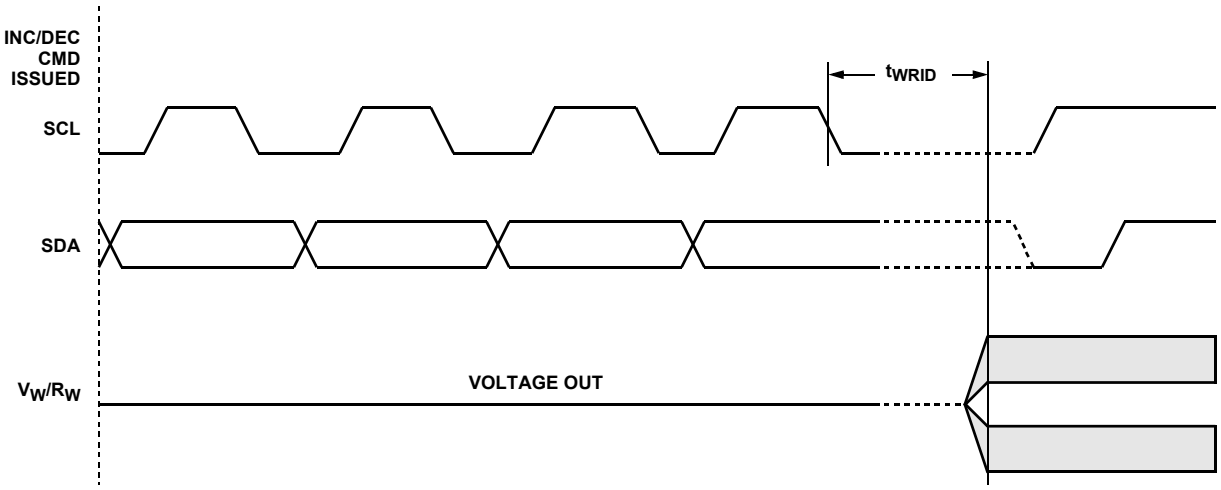


FIGURE 10. INCREMENT/ DECREMENT TIMING LIMITS

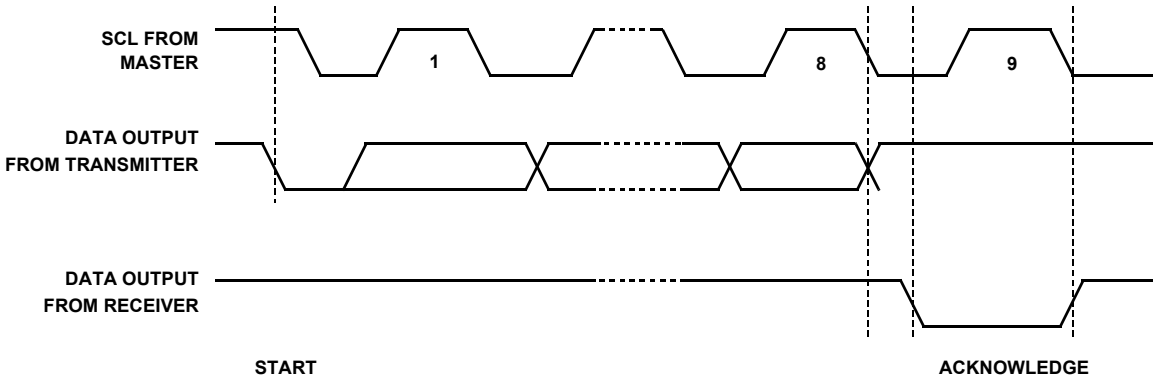


FIGURE 11. ACKNOWLEDGE RESPONSE FROM RECEIVER

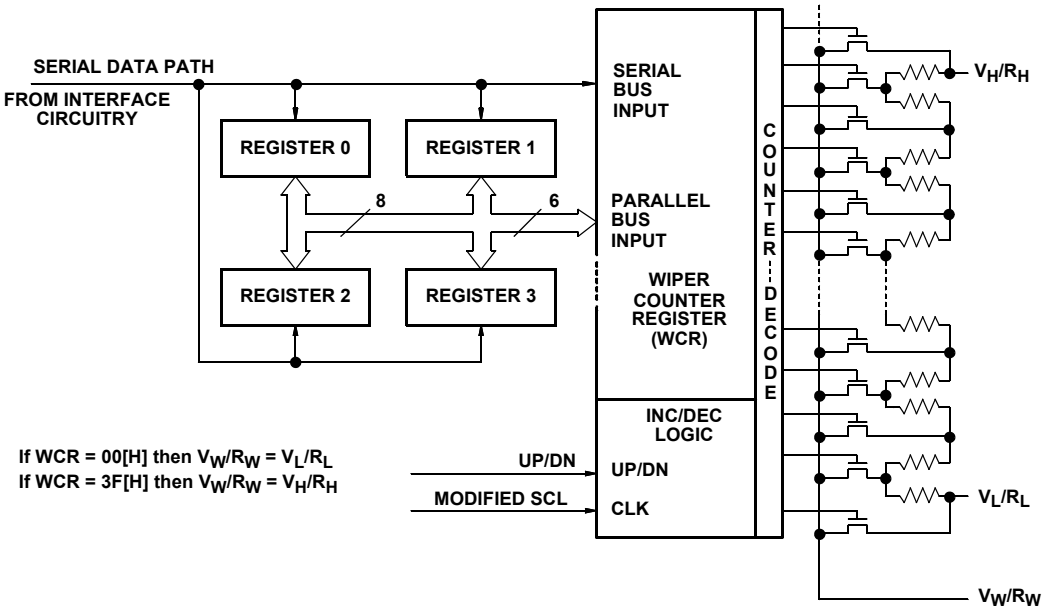


FIGURE 12. DETAILED POTENTIOMETER BLOCK DIAGRAM

Detailed Operation

All XDCP potentiometers share the serial interface and share a common architecture. Each potentiometer has a Wiper Counter Register and 4 Data Registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter Register

The X9409 contains four Wiper Counter Registers, one for each XDCP potentiometer. The Wiper Counter Register can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of the four associated Data Registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/ Decrement instruction. Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9409 is powered down. Although the register is automatically loaded with the value in DR0 upon power-up, it should be noted this may be different from the value present at power-down.

Data Registers

Each potentiometer has four nonvolatile Data Registers. These can be read or written directly by the host and data can be transferred between any of the four Data Registers and the Wiper Counter Register. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

Register Descriptions

TABLE 2. DATA REGISTERS, (6-BIT), NONVOLATILE

D5	D4	D3	D2	D1	D0
NV	NV	NV	NV	NV	NV
(MSB)					(LSB)

Four 6-bit Data Registers for each XDCP. (sixteen 6-bit registers in total).

{D5~D0}: These bits are for general purpose not volatile data storage or for storage of up to four different wiper values. The contents of Data Register 0 are automatically moved to the wiper counter register on power-up.

TABLE 3. WIPER COUNTER REGISTER, (6-BIT), VOLATILE

WP5	WP4	WP3	WP2	WP1	WP0
V	V	V	V	V	V
(MSB)					(LSB)

One 6-bit Wiper Counter Register for each XDCP. (Four 6-bit registers in total).

{D5~D0}: These bits specify the wiper position of the respective XDCP. The Wiper Counter Register is loaded on power-up by the value in Data Register R_0. The contents of the WCR can be loaded from any of the other Data Register or directly by command. The contents of the WCR can be saved in a DR.

Read Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				WCR ADDRESSES				S A C K	WIPER POSITION (SENT BY SLAVE ON SDA)								M A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	0	1	0	0	P1	P0		0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Write Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				WCR ADDRESSES				S A C K	WIPER POSITION (SENT BY MASTER ON SDA)								S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	1	0	0	0	P1	P0		0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Read Data Register (DR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR AND WCR ADDRESSES				S A C K	WIPER POSITION (SENT BY SLAVE ON SDA)								M A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	1	1	R1	R0	P1	P0		0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Write Data Register (DR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR AND WCR ADDRESSES				S A C K	WIPER POSITION (SENT BY MASTER ON SDA)								S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	A1	A0		1	1	0	0	R1	R0	P1	P0		0	0	WP5	WP4	WP3	WP2	WP1	WP0			

Transfer Data Register (DR) to Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR AND WCR ADDRESSES				S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	1	0	1	R1	R0	P1	P0		

Write Wiper Counter Register (WCR) to Data Register (DR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR AND WCR ADDRESSES				S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	A1	A0		1	1	1	0	R1	R0	P1	P0			

Increment/Decrement Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				WCR ADDRESSES				S A C K	INCREMENT/DECREMENT (SENT BY MASTER ON SDA)						S T O P
	0	1	0	1	A3	A2	A1	A0		0	0	1	0	0	0	P1	P0		I/D	I/D	.	.	.	I/D	I/D	

Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR ADDRESSES				S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		0	0	0	1	R1	R0	0	0		

Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR ADDRESSES				S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	A1	A0		1	0	0	0	R1	R0	0	0			

Instruction Format

NOTES:

14. “MACK”/”SACK”: stands for the acknowledge sent by the master/slave.
15. “A3 ~ A0”: stands for the device addresses sent by the master.
16. “X”: indicates that it is a “0” for testing purpose but physically it is a “don’t care” condition.
17. “I”: stands for the increment operation, SDA held high during active SCL phase (high).
18. “D”: stands for the decrement operation, SDA held low during active SCL phase (high).

Applications Information

Basic Configurations of Electronic Potentiometers

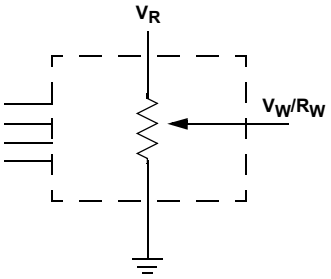


FIGURE 13. THREE TERMINAL POTENTIOMETER; VARIABLE VOLTAGE DIVIDER

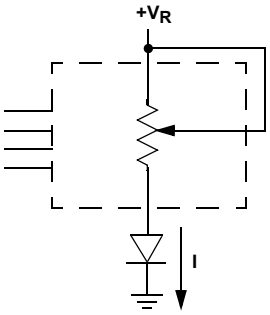
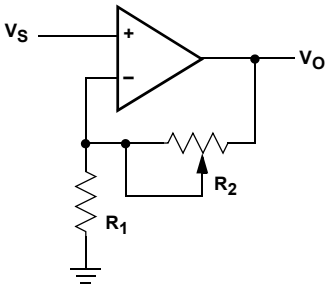


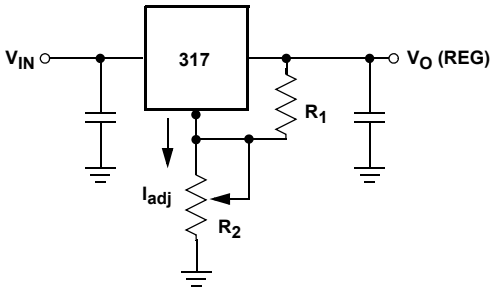
FIGURE 14. TWO TERMINAL VARIABLE RESISTOR; VARIABLE CURRENT

Application Circuits



$V_O = (1+R_2/R_1)V_S$

FIGURE 15. NONINVERTING AMPLIFIER



V_O (REG) = 1.25V $(1+R_2/R_1)+I_{adj}$ R_2

FIGURE 16. VOLTAGE REGULATOR

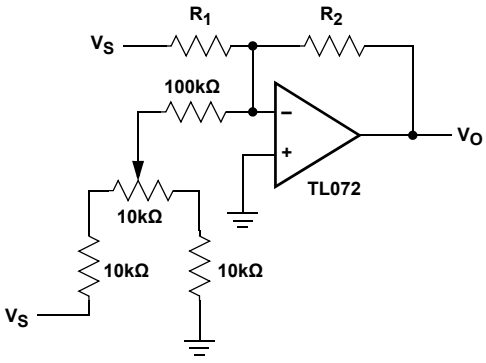
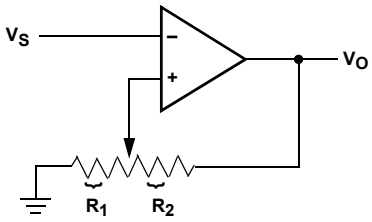


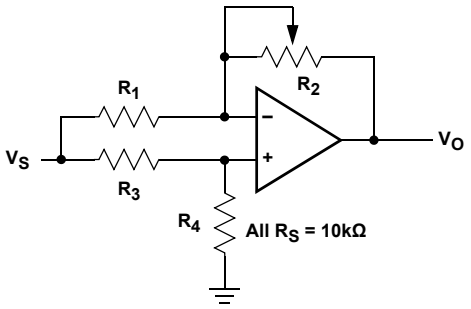
FIGURE 17. OFFSET VOLTAGE ADJUSTMENT



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

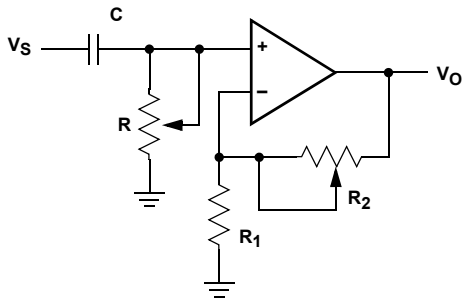
FIGURE 18. COMPARATOR WITH HYSTERESIS

Application Circuits (Continued)



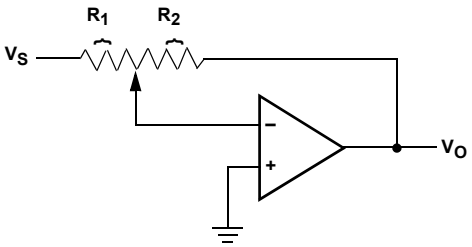
$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

FIGURE 19. ATTENUATOR



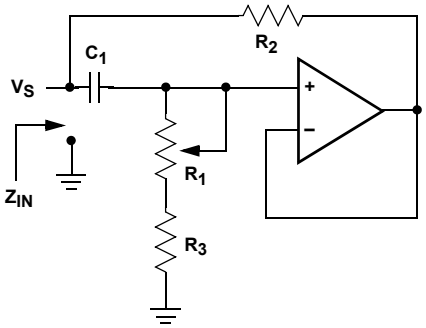
$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

FIGURE 20. FILTER



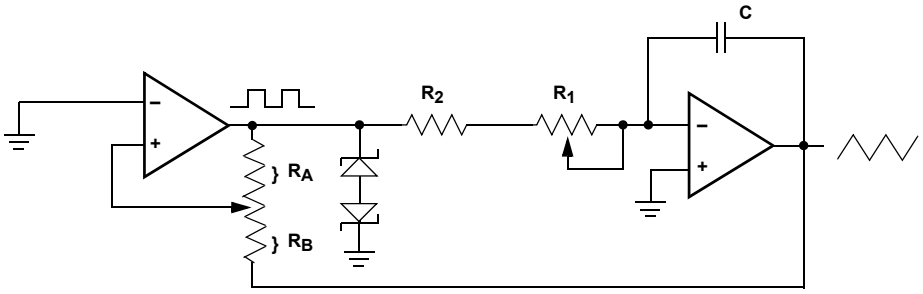
$V_O = G\ V_S$
$G = -\ R_2/R_1$

FIGURE 21. INVERTING AMPLIFIER



$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

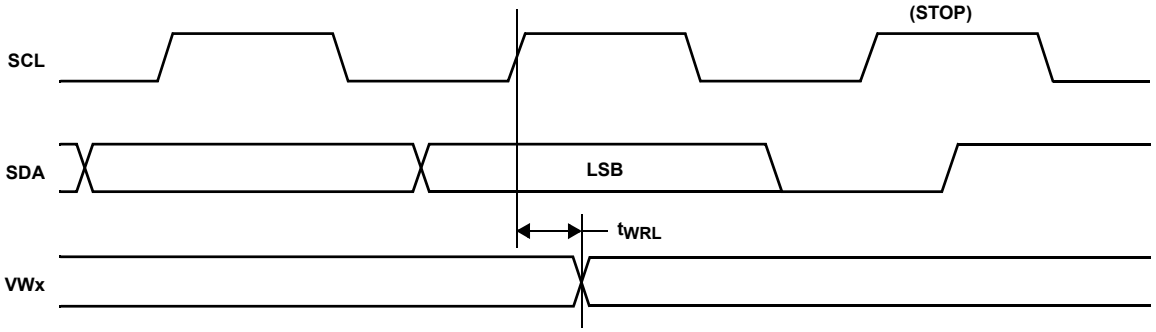
FIGURE 22. EQUIVALENT L-R CIRCUIT



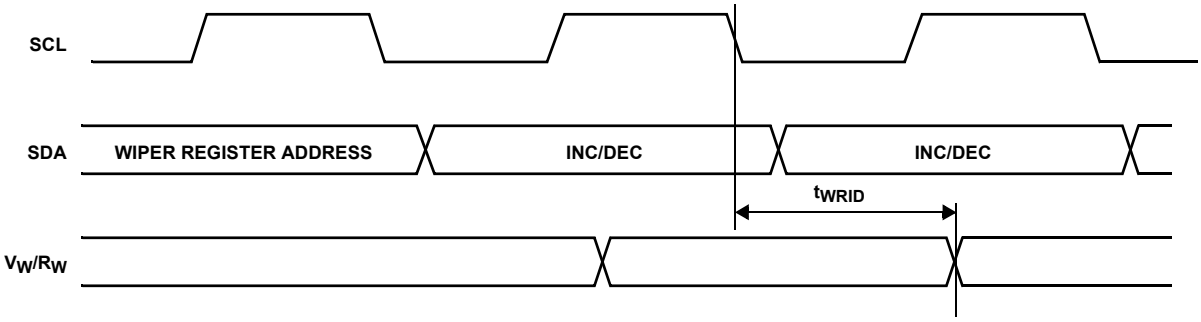
frequency $\propto R_1, R_2, C$
amplitude $\propto R_A, R_B$

FIGURE 23. FUNCTION GENERATOR

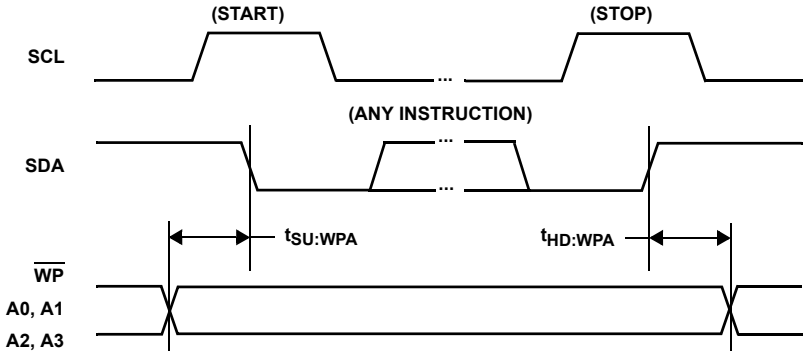
XDCP Timing (for All Load Instructions)



XDCP Timing (for Increment/Decrement Instruction)



Write Protect and Device Address Pins Timing



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 3, 2015	FN8192.6	Updated Ordering Information table on page 2.
April 20, 2015	FN8192.5	Updated Template. Added revision history. Removed part numbers X9409WS24I-2.7 and X9409WS24IZ-2.7 from ordering information table. Analog Characteristics table on page 5, in ISB section: Changed max value from 1µ to 3µ. Removed 24 Ld SOIC throughout the document. Removed POD M24.3.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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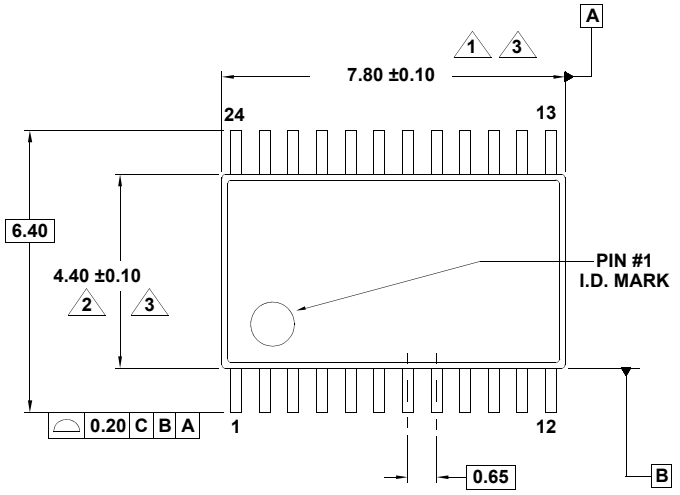
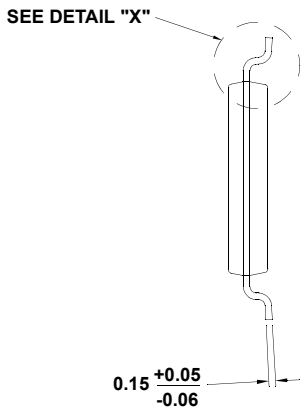
Package Outline Drawing

M24.173

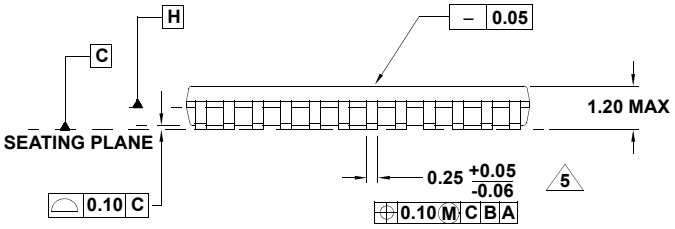
24 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 1, 5/10



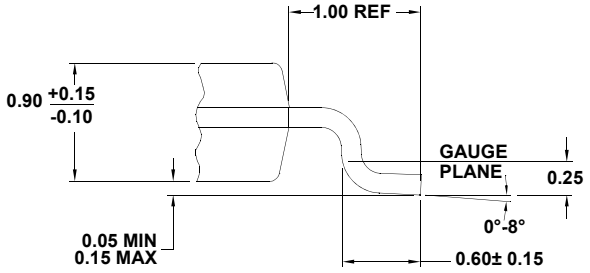
TOP VIEW



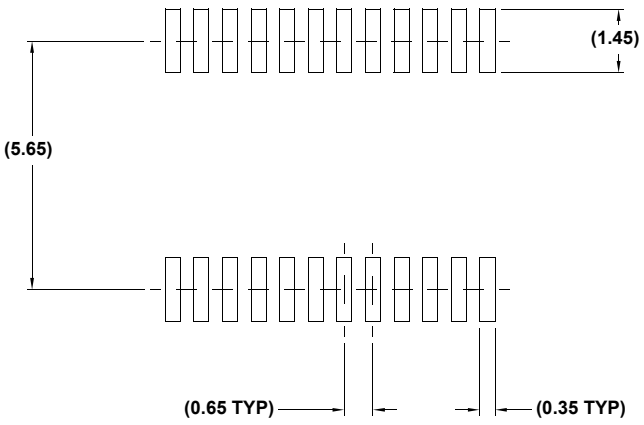
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.