One-time Digital 32-tap Potentiometer (POT)

Description

The CAT5126 is a digital POT. The wiper position is controlled with a simple 2-wire digital interface. This digital potentiometer is unique in that it has an optional one-time programmable feature that either sets the wiper's position upon power-on to a user-defined value, or the wiper can be set and the interface also disabled to prevent further adjustment.

The CAT5126 has an end-to-end resistance of 10 k Ω , 50 k Ω , and 100 k Ω . All CAT5126 devices have 32-wiper positions and operate from a single 2.5 V to 5.5 V supply.

The CAT5126 is available in TDFN 8-pad and MSOP 8-lead packages. Each device is guaranteed over the industrial temperature range of -40° C to $+85^{\circ}$ C.

Features

- Wiper Position Stored after One-time Non-volatile Programming
- User-defined Power-On Wiper Position
- 32-tap Positions
- Wiper Position Programmed through Simple 2-wire Serial Interface
- Low 0.35 μA (typ) Static Supply Current
- 2.5 V to 5.5 V Single-supply Operation
- $10 \text{ k}\Omega$, $50 \text{ k}\Omega$, and $100 \text{ k}\Omega$ End-to-End Resistances
- 50 ppm/°C End-to-End Temperature Coefficient and 5 ppm/°C Ratiometric Temperature Coefficient
- TDFN 8-pad (2 × 3 mm) and MSOP 8-lead Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Mechanical Potentiometer Replacement
- Products using One-time Factory Calibration
- Contrast, Brightness, Volume Controls
- Programmable Analog Functions



ON Semiconductor®

http://onsemi.com

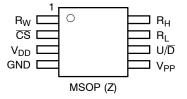


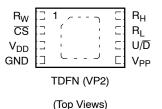
MSOP-8 Z SUFFIX CASE 846AD



TDFN-8 VP2 SUFFIX CASE 511AK

PIN CONFIGURATIONS





ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

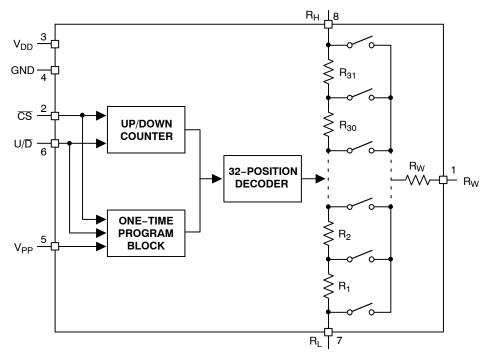


Figure 1. Functional Diagram

Table 1. PIN DESCRIPTION

Pin	Name	Function
1	R_W	Wiper Connection
2	CS	Chip-Select Input. A high-to-low \overline{CS} transition determines the mode: increment if U/ \overline{D} is high, or decrement if U/ \overline{D} is low. \overline{CS} is also used for one-time programming (see the One-Time Programming section).
3	V_{DD}	Power-Supply Voltage
4	GND	Ground
5	V _{PP}	Programming Voltage for One-Time Programming. Connect V _{PP} to 10 V supply when one-time programming the device. For normal operation, connect to ground or let float.
6	U/D	Up/Down Control Input. With CS low, a low-to-high transition increments or decrements the wiper position.
7	R_L	Low Terminal of Resistor
8	R _H	High Terminal of Resistor

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V _{DD} to GND	-0.5 to +7.0	V
V _{PP} to GND	-0.5 to +12.0	V
All other pins to GND	-0.5 to V _{DD} +0.5	V
Maximum Continuous Current into H, L, and W	±1.5	mA
Continuous Power Dissipation (T _A = +70°C) MSOP 8-lead (derate 4.5 mW/°C above +70°C) TDFN 8-pad (derate 24.4 mW/°C above +70°C)	362 1951	mW
Operating Temperature Range	-40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 s)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
DC PERFO	PRMANCE					
RES	Resolution			3.2		%
R _{POT}	End-to-End Resistance	-10 Device	8	10	12	kΩ
		-50 Device	40	50	60	1
		-00 Device	80	100	120	1
TC _{RPOT}	TC of Pot Resistance			±50	±300	ppm/°C
TC _{RATIO}	Ratiometric Resistance TC			±5	±20	ppm/°C
INL	Integral Nonlinearity	Potentiometer configuration, no load		0.5	1	LSB
DNL	Differential Nonlinearity	Potentiometer configuration, no load		0.25	0.5	LSB
R _W	Wiper Resistance	V _{DD} = 5 V		70	100	Ω
		V _{DD} = 2.5 V		150	200	1
DIGITAL IN	IPUTS (CS, U/D)					
V _{IH}	Input High Voltage		0.7 x V _{DD}			V
V _{IL}	Input Low Voltage				0.3 x V _{DD}	V
I _{IN}	Input Leakage Current			±0.1	±1	μА
C _{IN}	Input Capacitance			5		pF
POWER SI	UPPLY	•	•	•	•	•
V_{DD}	Supply Voltage		2.5		5.5	V
I _{DD}	Stand by Current	(Note 2)		0.35	1	μА
I _{DDW}	Programming Current			0.25	1	mA
V _{PP}	Programming Voltage	V _{DD} = 5 V		8.5	10	V
		V _{DD} = 2.5 V		6.0	10	
I _{PP}	V _{PP} Input Current	V _{PP} = 10 V			5	μΑ
TIMING CH	IARACTERISTICS (Note 3)		•	•	•	•
t _{CU}	U/D Mode to CS Setup	Figures 6, 7	50			ns
t _{Cl}	CS Hold to U/D Mode	Figures 6, 7	50			ns
t _{IC}	U/D Step Hold to CS	Figures 6, 7	0			ns
t _{IL}	U/D Step Low Time	Figures 6, 7	100			ns
t _{IH}	U/D Step High Time	Figures 6, 7	100			ns
t _{IW}	Wiper Switching Time	C _L = 0 pF, Figures 6, 7		100		ns
t _{PC}	V _{PP} Rising Edge to CS Falling Edge	Figure 8	1			ms
t _{CP}	CS Falling Edge to V _{PP} Falling Edge	Figure 8	5			ms
t _{CL}	CS Step Low Time	Figure 8	5			ms
t _{CH}	CS Step High Time	Figure 8	5			ms
t _{PH}	V _{PP} Falling Edge to CS Rising Edge	Figure 8	1			ms
f _{U/DMAX}	U/D Frequency			1	5	MHz

- All devices are production tested at T_A = +25°C and are guaranteed by design for T_A = -40°C to +85°C.
 Digital inputs CS and U/D are connected to GND or V_{DD}.
 Digital timing is guaranteed by design, not production tested.
 Power-up time is the period of time from when the power supply is applied until the serial interface is ready for writing.

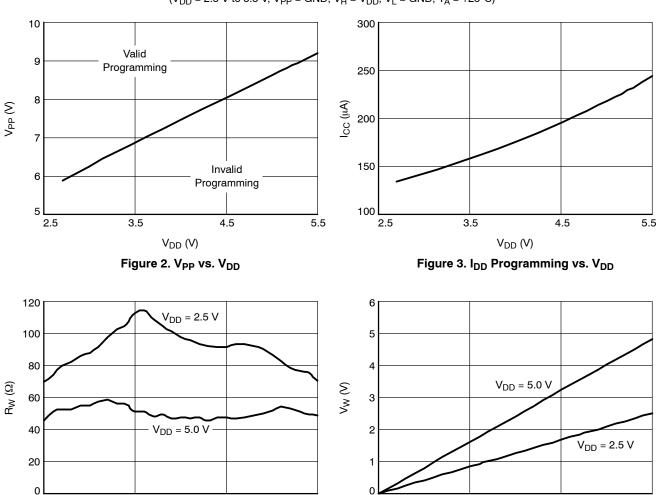
Table 3. ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5 V to 5.5 V, V_{PP} = GND, R_H = V_{DD} , R_L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{DD} = 5.0 \text{ V}$, $T_A = +25 ^{\circ}\text{C}$, unless otherwise noted.) (Note 1) (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
TIMING CHARACTERISTICS (Note 3)						
t _{UP}	Power-up Time	(Note 4)			1	ms
tSETTLE	Output Settling Time	100 k Ω variable resistor configuration, C_L = 10 pF		1		μs
		100 k Ω potentiometer configuration, C_L = 10 pF		0.25		

- 1. All devices are production tested at $T_A = +25^{\circ}C$ and are guaranteed by design for $T_A = -40^{\circ}C$ to $+85^{\circ}C$. 2. Digital inputs \overline{CS} and U/\overline{D} are connected to GND or V_{DD} .
- 3. Digital timing is guaranteed by design, not production tested.
- 4. Power-up time is the period of time from when the power supply is applied until the serial interface is ready for writing.

TYPICAL OPERATING CHARACTERISTICS

(V_{DD} = 2.5 V to 5.5 V, V_{PP} = GND, V_H = V_{DD}, V_L = GND, T_A = +25°C)



TAP POSITION Figure 4. Wiper Resistance vs. Tap Position @ 25°C

20

10

0

TAP Figure 5. Wiper Voltage vs. Tap Position

20

30

30

Detailed Description

The CAT5126 devices are $10~k\Omega/50~k\Omega/100~k\Omega$ (end-to-end resistance) digitally controlled potentiometers. They have 32-tap positions that are accessible to the wiper along the resistor array between R_H and R_L .

The wiper (R_W) position is adjusted sequentially through the tap positions using a simple I^2C interface. These digital potentiometers have an optional one-time programmable feature that sets the POR position of the wiper. The I^2C interface can then be disabled, permanently preventing unwanted adjustment.

Digital Interface Operation

The CAT5126 devices have two modes of operation when the serial interface is active: increment mode and decrement mode. The serial interface is only active when \overline{CS} is low.

The \overline{CS} and U/\overline{D} inputs control the position of the wiper along the resistor array. When \overline{CS} transitions from high to low, the part goes into increment mode if U/\overline{D} is high (Figure 6), and into decrement mode if U/\overline{D} is low (Figure 7). Once the mode is set, the device remains in that mode until \overline{CS} goes high. A low-to-high transition at the U/\overline{D} increments or decrements the wiper position depending on the current mode.

The value of the counter is then stored and the wiper position is maintained till the device is Powered down.

The wiper performs a make-before-break transition, ensuring that there is never an open circuit during a transition from one resistor tap to another. When the wiper is at either end (max/min) of the resistor array, additional transitions in the direction of the endpoint do not change the counter value (the counter does not wrap around).

One-Time Programming

The factory-set default position of the wiper on power-up is tap 16. However, the power-up position can be changed once using the one-time programming feature. After the wiper is moved to the desired position, the programming sequence is initiated by setting U/\overline{D} high, applying 10 V to V_{PB} and then taking \overline{CS} low. Five pulses on \overline{CS} (consisting of \overline{CS} starting from low and going high for t_{CH} and then low for t_{CL}) program the device (Figure 8). The programming voltage should then be taken to zero. After the device is programmed, V_{PP} can be set to zero or be allowed to float. The wiper position is still adjustable, but always returns to this programmed position on power–up.

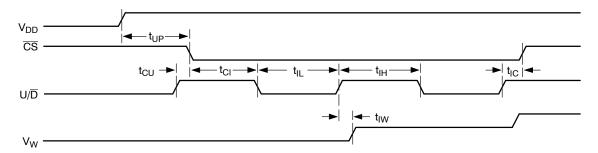


Figure 6. Increment Mode Serial Interface Timing Diagram

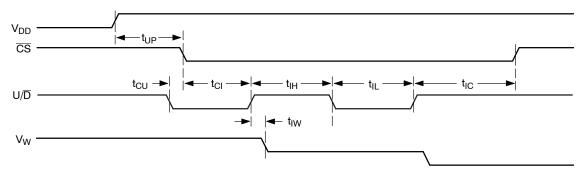


Figure 7. Decrement Mode Serial Interface Timing Diagram

If the intent is to program the device to a specific wiper position and not to allow further adjustments, then six programming pulses are required (as opposed to five), as shown in Figure 8. The sixth pulse locks the wiper position and disables the serial interface. This also allows U/\overline{D} and \overline{CS} to float without any increase in supply current. Once the lockout bit is set, no further adjustment to the potentiometer is possible, effectively changing the potentiometer into a fixed resistor-divider (Table 4).

It is recommended that the user either use six $\overline{\text{CS}}$ pulses (convert to a fixed voltage-divider) or five pulses (program the initial power-up value of the device, but still be able to adjust the wiper). If the device is programmed with five pulses and later it is desired to disable the interface (convert to a fixed voltage-divider), then care must be taken to ensure that the wiper is in the same position as it was originally set to (when programmed with five pulses). The full six programming pulses must be applied. Note that once the six-pulse program occurs, no further programming is possible.

Table 4. ONE-TIME PROGRAMMING MODE

Mode	Power Up Position	Interface	Operation
Factory Default	At midscale	Active	Programming allowed
Programming with 5 pulses at the midscale position	At midscale	Active	Programming allowed
Programming with 5 pulses different from midscale position – only once	At the new programmed position	Active	No further change in power-up position allowed
Programming with 5 pulses if the power up position was changed before	At the previous programmed position	Active	None
Programming with 6 pulses if the tap position is at midscale	Midscale position forever	I ² C interface active till power down	I ² C interface disable after next power-up
Programming ONLY with 6 pulses if the tap position is different from midscale position	At the new programmed position	I ² C interface active till power down	I ² C interface disable after next power-up

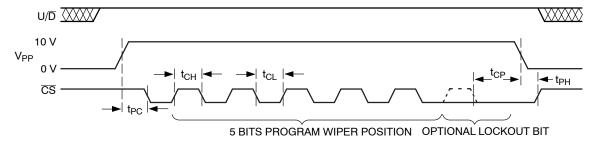
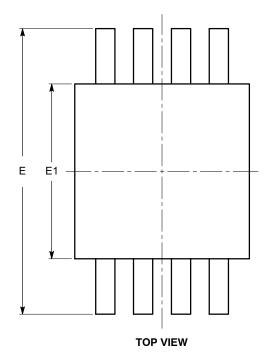


Figure 8. One Time Program Mode Serial Interface Timing Diagram

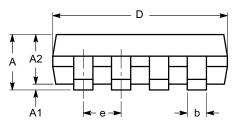
- 5. If CAT5126 is Programmed with less than 5 pulses, it does not change the Power-up recall position.
- 6. During internal power-up the wiper is forced to miscale; thereafter the wiper is set at the stored position.

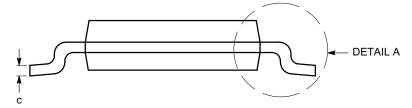
PACKAGE DIMENSIONS

MSOP 8, 3x3 CASE 846AD ISSUE O



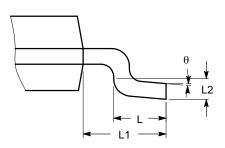
SYMBOL	MIN	NOM	MAX	
Α			1.10	
A1	0.05	0.10	0.15	
A2	0.75	0.85	0.95	
b	0.22		0.38	
С	0.13		0.23	
D	2.90	3.00	3.10	
E	4.80	4.90	5.00	
E1	2.90	3.00	3.10	
е		0.65 BSC		
L	0.40	0.60	0.80	
L1	0.95 REF			
L2	0.25 BSC			
θ	0°		6°	





SIDE VIEW

END VIEW



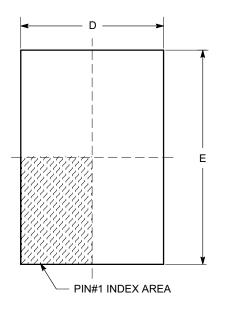
Notes:

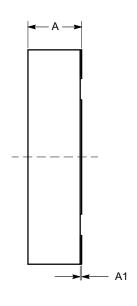
- (1) All dimensions are in millimeters. Angles in degrees.(2) Complies with JEDEC MO-187.

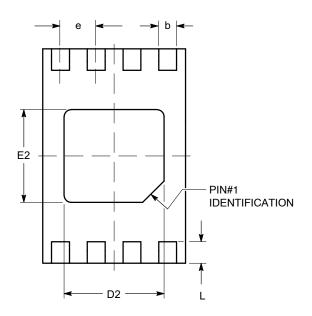
DETAIL A

PACKAGE DIMENSIONS

TDFN8, 2x3 CASE 511AK ISSUE A





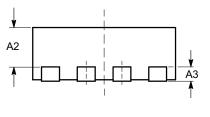


TOP VIEW

SIDE VIEW

BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
Α	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
Е	2.90	3.00	3.10
E2	1.20	1.30	1.40
е	0.50 TYP		
L	0.20	0.30	0.40



FRONT VIEW

Notes:

- (1) All dimensions are in millimeters.(2) Complies with JEDEC MO-229.

Table 5. ORDERING INFORMATION

Orderable Part Numbers	Resistor (kΩ)	Package-Pin	Shipping [†]
CAT5126VP2I10GT3	10	TDFN-8	3000 / Tape & Ree
CAT5126ZI-10-G	10	MSOP-8	96 / Tube
CAT5126ZI-10-GT3	10	MSOP-8	3000 / Tape & Ree
CAT5126ZI-50-GT3 (Note 10)	50	MSOP-8	3000 / Tape & Ree
CAT5126ZI-00-GT3 (Note 10)	100	MSOP-8	3000 / Tape & Ree

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor and III are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implications to be below or other applications to the case of the science of the scie surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA **Phone**: 303–675–2175 or 800–344–3860 Toll Free USA/Canada **Fax**: 303–675–2176 or 800–344–3867 Toll Free USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

^{7.} For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.

^{8.} All packages are RoHS-compliant (Lead-free, Halogen-free).

^{9.} The standard lead finish is NiPdAu.

^{10.} For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.