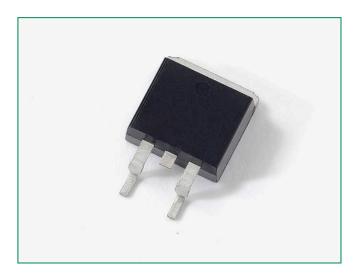


# NGB8204AN - 18 A, 400 V, N-Channel Ignition IGBT, D2PAK





18 Amps, 400 Volts  $V_{cr}(on) \le 2.0 \text{ V } @$  $I_{c} = 10A$ ,  $V_{GE} \ge 4.5 \text{ V}$ 

# Maximum Ratings (T<sub>1</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CES</sub>	430	V <sub>DC</sub>
Collector-Gate Voltage	V <sub>CER</sub>	430	V <sub>DC</sub>
Gate-Emitter Voltage	V <sub>GE</sub>	18	V <sub>DC</sub>
Collector Current–Continuous @T <sub>c</sub> = 25°C – Pulsed	I <sub>c</sub>	18 50	A <sub>DC</sub>
ESD (Human Body Model) R = 1500 $\Omega$ , C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	800	V
Total Power Dissipation @T <sub>c</sub> = 25°C Derate above 25°C	P <sub>D</sub>	115 0.77	Watts W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

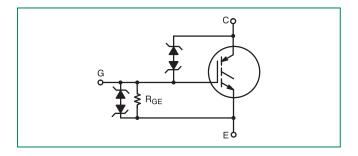
#### **Description**

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

#### **Features**

- Ideal for Coil-on-Plug Applications
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Integrated Gate-Emitter Resistor (Rgs)
- Emitter Ballasting for Short-Circuit Capability
- These are Pb-Free Devices

#### **Functional Diagram**



## **Additional Information**







Resources



Samples



Unc	lamped Co	ollector–To–Em	itter Avalar	nche Ch	naracteristics (	(–55°≤T <sub>J</sub> ≤175°C)
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Rating	Symbol	Value	Unit	
Single Pulse Collector-to-Emitter Avalanche Energy				
$V_{CC} = 50 \text{ V}, V_{GE} = 5.0 \text{ V}, P_k I_L = 21.1 \text{ A}, L = 1.8 \text{ mH}, \text{ Starting T}_J = 25^{\circ}\text{C}$	_	400		
$V_{CC} = 50 \text{ V}, V_{GE} = 5.0 \text{ V}, P_k I_L = 18.3 \text{ A}, L = 1.8 \text{ mH}, Starting T_J = 125^{\circ}\text{C}$	- E <sub>AS</sub>	400	mJ	
Reverse Avalanche Energy				
$V_{CC} = 100 \text{ V}, V_{GE} = 20 \text{ V}, P_k I_L = 25.8 \text{ A}, L = 6.0 \text{ mH}, \text{ Starting T}_J = 25^{\circ}\text{C}$	E <sub>AS(R)</sub>	2000	mJ	

# Maximum Short-Circuit Times (-55°C ≤ TJ ≤ 150°C)

	Symbol	Value	Unit
Short Circuit Withstand Time 1 (See Figure 17, 3 Pulses with 10 ms Period)	t <sub>sc</sub> 1	750	μs
Short Circuit Withstand Time 2 (See Figure 18, 3 Pulses with 10 ms Period)	t <sub>sc</sub> 2	5.0	ms

# **Thermal Characteristics**

Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Case	R <sub>euc</sub>	1.3	°C/W
Thermal Resistance, Junction to Ambient D <sup>2</sup> PAK (Note 1)	$R_{\theta_{JA}}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T <sub>L</sub>	275	°C

<sup>1.</sup> When surface mounted to an FR4 board using the minimum recommended pad size.



# **Electrical Characteristics - OFF**

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
Collector-Emitter	DV/	I <sub>C</sub> = 2.0 mA	$T_J = -40^{\circ}\text{C to}$ 150°C	370	395	420	\/
Clamp Voltage	BV <sub>CES</sub>	$I_c = 10 \text{ mA}$	$T_J = -40^{\circ}\text{C to}$ 150°C	390	415	440	V <sub>DC</sub>
			T <sub>J</sub> = 25°C	_	2.0	10	
Zero Gate Voltage Collector Current	I <sub>CES</sub>	$V_{CE} = 200V$ $V_{GE} = 0 V$	T <sub>J</sub> = 150°C	_	10	40*	μA <sub>DC</sub>
			T <sub>J</sub> = -40°C	-	1.0	10	
			T <sub>J</sub> = 25°C	27	33	37	
Reverse Collector–Emitter Clamp Voltage	B <sub>VCES(R</sub>	$I_{c} = -75 \text{ mA}$	T <sub>J</sub> = 150°C	30	36	40	V <sub>DC</sub>
			T <sub>J</sub> = -40°C	25	32	35	
			T <sub>J</sub> = 25°C	_	0.7	1.0	
Reverse Collector–Emitter Leakage Current	I <sub>CES(R)</sub>	$V_{CE} = -24 V$	T <sub>J</sub> = 150°C	_	12	25*	mA
			T <sub>J</sub> = -40°C	_	0.1	1.0	
Gate–Emitter Clamp Voltage	BV <sub>GES</sub>	I <sub>G</sub> = 5.0 mA	T <sub>J</sub> = -40°C to 150°C	11	13	15	V <sub>DC</sub>
Gate–Emitter Leakage Current	I <sub>GES</sub>	V <sub>GE</sub> = 10 V	T <sub>J</sub> = -40°C to 150°C	384	640	700	μA <sub>DC</sub>
Gate Emitter Resistor	R <sub>GE</sub>	-	T <sub>J</sub> = -40°C to 150°C	10	16	26	kΩ



ctrical Characteristics - ON (	Note 3)						
Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
			T <sub>J</sub> = 25°C	1.1	1.4	1.9	
Gate Threshold Voltage	V <sub>GE(th)</sub>	$I_{c} = 1.0 \text{ mA},$ $V_{GE} = V_{CE}$	T <sub>J</sub> = 150°C	0.75	1.0	1.4	V <sub>DC</sub>
		GE CE	T <sub>J</sub> = -40°C	1.2	1.6	2.1*	
Threshold Temperature Coefficient (Negative)	-	-	-	-	3.4	-	mV/°
			T <sub>J</sub> = 25°C	1.0	1.4	1.6	
		$I_{c} = 6.0 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	T <sub>J</sub> = 150°C	0.9	1.3	1.6	
			T <sub>J</sub> = -40°C	1.1	1.45	1.7*	
		$I_{c} = 8.0 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	T <sub>J</sub> = 25°C	1.3	1.6	1.9*	
			T <sub>J</sub> = 150°C	1.2	1.55	1.8	
			V <sub>GE</sub> — 4.0 V	T <sub>J</sub> = -40°C	1.4	1.6	1.9*
			T <sub>J</sub> = 25°C	1.4	1.8	2.0	
Collector-to-Emitter On-Voltage	V <sub>CE (on)</sub>	$I_C = 10 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	T <sub>J</sub> = 150°C	1.5	1.8	2.0	V <sub>DC</sub>
J		GE TIS	T <sub>J</sub> = -40°C	1.4	1.8	2.1*	
		45.4	T <sub>J</sub> = 25°C	1.8	2.2	2.5	
		$I_{c} = 15 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	T <sub>J</sub> = 150°C	2.0	2.4	2.6*	
		$V_{GE} = 4.0 \text{ V}$ $I_{C} = 10 \text{ A},$ $V_{GE} = 4.5 \text{ V}$	T <sub>J</sub> = -40°C	1.7	2.1	2.5	
			T <sub>J</sub> = 25°C	1.3	1.8	2.0*	
			T <sub>J</sub> = 150°C	1.3	1.75	2.0*	
			T <sub>J</sub> = -40°C	1.4	1.8	2.0*	
Forward Transconductance	gfs	$V_{CE} = 5.0 \text{ V},$ $I_{C} = 6.0 \text{ A}$	T <sub>J</sub> = -40°C to 150°C	8.0	14	25	Mho

 $<sup>{\</sup>rm *Maximum\,Value\,\,of\,\,Characteristic\,\,across\,Temperature\,\,Range}.$ 

#### **Dynamic Characteristics**

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
Input Capacitance	C <sub>ISS</sub>	V <sub>cc</sub> = 25 V		400	800	1000	
Output Capacitance	C <sub>oss</sub>	$V_{GE} = 0 V$	$T_{J} = -40^{\circ}\text{C} \text{ to}$ 150°C	50	75	100	pF
Transfer Capacitance	C <sub>RSS</sub>	f = 1.0 MHz		4.0	7.0	10	

<sup>3.</sup> Pulse Test: Pulse Width  $\leq 300~\mu\text{S},~\text{Duty Cycle} \leq 2\,\%$  .



### **Switching Characteristics**

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
Turn-Off Delay Time (Resistive)	t <sub>d (off)</sub>	$V_{cc} = 300 \text{ V},$ $I_{c} = 6.5 \text{ A}$	T <sub>J</sub> = 25°C	_	4.0	10	
Fall Time (Resistive)	t <sub>f</sub>	$R_{G} = 1.0 \text{ k}\Omega,$ $R_{L} = 46 \Omega$	T <sub>J</sub> = 25°C	-	9.0	15	u <sup>2</sup> 00
Turn-On Delay Time	t <sub>d (on)</sub>	$V_{CC} = 10 \text{ V},$ $I_{C} = 6.5 \text{ A}$	T <sub>J</sub> = 25°C	_	0.7	4.0	μSec
Rise Time	t <sub>r</sub>	$R_{G} = 1.0 \text{ k}\Omega,$ $R_{L} = 1.5 \Omega,$	T <sub>J</sub> = 25°C	_	4.5	7.0	

## **Ratings and Characteristic Curves**

**Figure 1. Output Characteristics** 

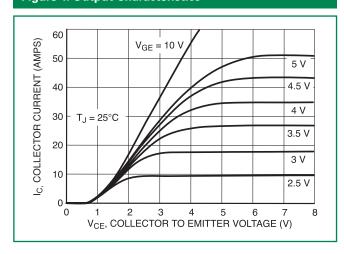
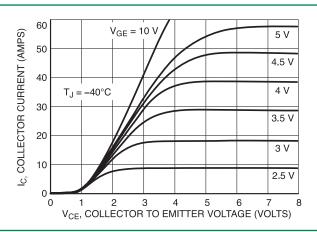
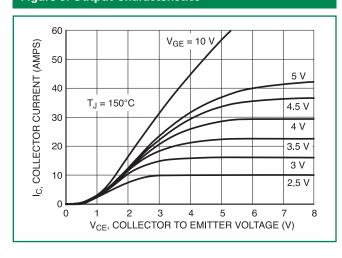


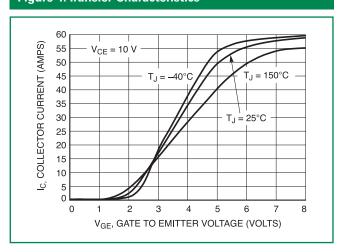
Figure 2. Output Characteristics



**Figure 3. Output Characteristics** 



**Figure 4. Transfer Characteristics** 





#### **Ratings and Characteristic Curves**

Figure 5. Collector-to-Emitter Saturation Voltage vs Junction Temperature

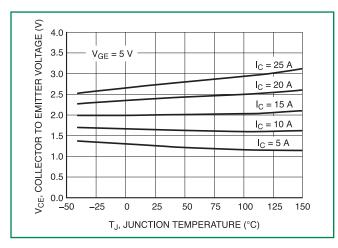


Figure 7. Collector-to-Emitter Voltage vs Gate-to-Emitter Voltage

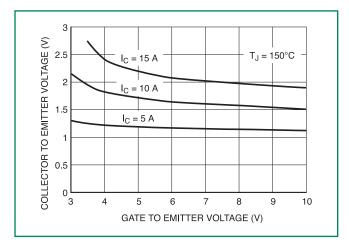


Figure 9. Gate Threshold Voltage versus Temperature

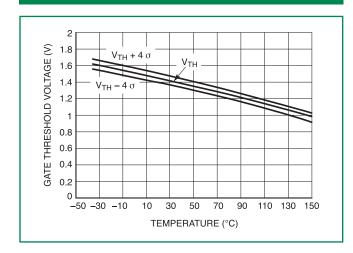


Figure 6. Collector-to-Emitter Voltage vs Gate-to-Emitter Voltage

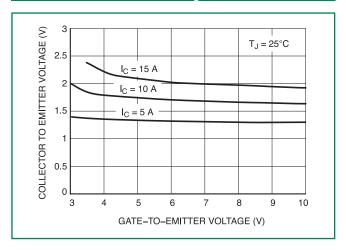


Figure 8. Capacitance Variation

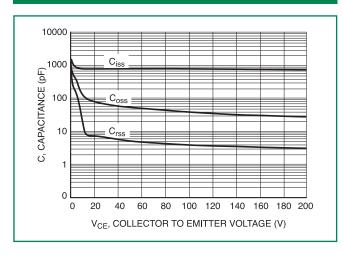


Figure 10. Minimum Open Secondary Latch Current vs. Temperature

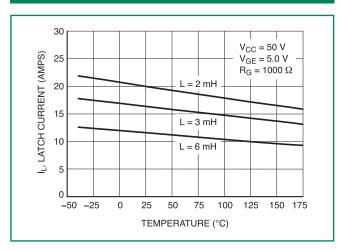




Figure 11. Typical Open Secondary Latch Current vs. Temperature

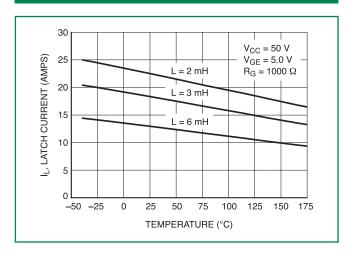


Figure 13. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at T<sub>A</sub> = \( \mathbb{N} \)\)

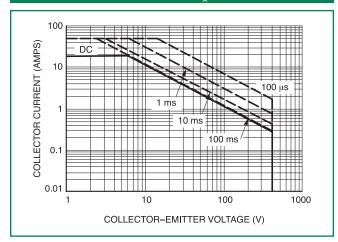


Figure 15. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at  $T_c = 25^{\circ}$ C)

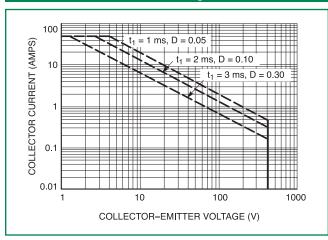


Figure 12. Inductive Switching Fall Time vs. Temperature

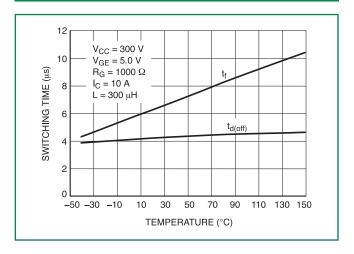


Figure 14. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at  $T_a = 125$ °C)

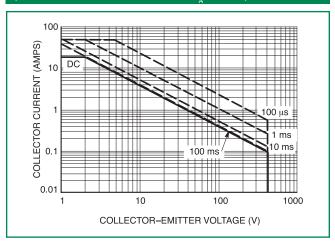
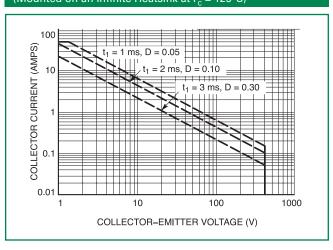


Figure 15. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at  $T_c = 125$ °C)





# Figure 17. Circuit Configuration for Short Circuit Test #1

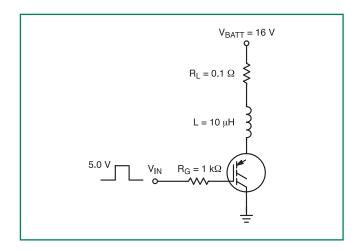


Figure 18. Circuit Configuration for Short Circuit Test #2

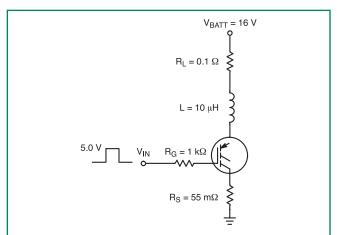
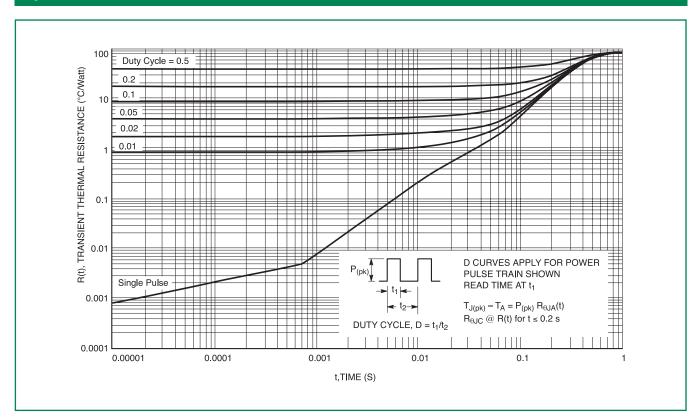
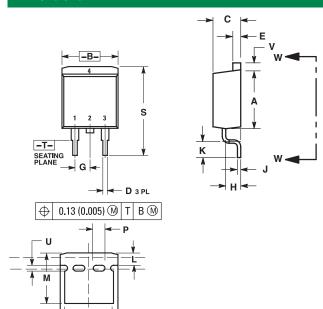


Figure 19. Transient Thermal Resistance (Non-normalized Junction-to-Ambient mounted on minimum pad area)





#### **Dimensions**



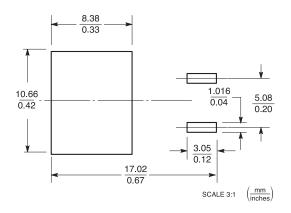
VIEW W-W 10.66

0.42					
Dise	Inc	hes	Millim	neters	
Dim	Min	Max	Min	Max	
А	0.340	0.380	8.64	9.65	
В	0.380	0.405	9.65	10.29	
С	0.160	0.190	4.06	4.83	
D	0.020	0.035	0.51	0.89	
Е	0.045	0.055	1.14	1.40	
F	0.310	0.350	7.87	8.89	
G	0.100	BSC	2.54 BSC		
Н	0.080	0.110	2.03	2.79	
J	0.018	0.025	0.46	0.64	
K	0.090	0.110	2.29	2.79	
L	0.052	0.072	1.32	1.83	
М	0.280	0.320	7.11	8.13	
N	0.197	7 REF	5.00 REF		
Р	0.079 REF		2.00 REF		
R	0.039 REF		0.99	REF	
S	0.575	0.625	14.60	15.88	
V	0.045	0.055	1.14	1.40	

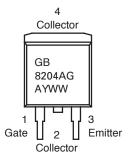
#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.
- 3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

#### **Soldering Footrpint**



## **Part Marking System**



GB8204x= Device Code

A= Assembly Location
Y= Year
Walk

WW = Work Week
G= Pb-Free Package

## **ORDERING INFORMATION**

Device	Package	Shipping†
NGB8204ANT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

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