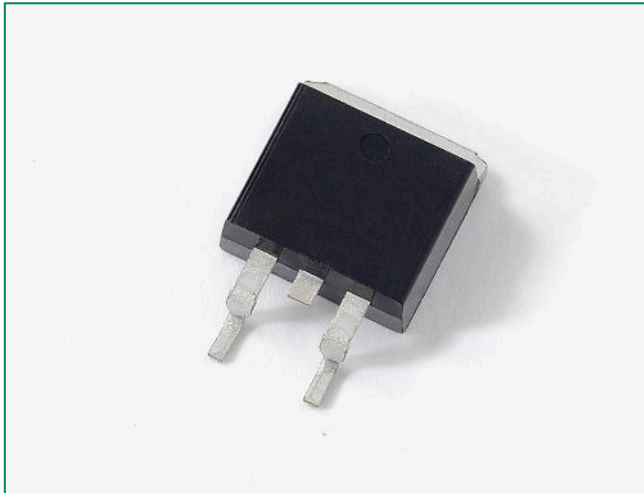


# NGD18N40ACLB - 18 A, 400 V, N-Channel Ignition IGBT, DPAK



18 Amps, 400 Volts  
 $V_{CE(on)} \leq 2.0 \text{ V @}$   
 $I_C = 10 \text{ A, } V_{GE} \geq 4.5 \text{ V}$

### Maximum Ratings (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V <sub>CES</sub>	430	V <sub>DC</sub>
Collector–Gate Voltage	V <sub>CER</sub>	430	V <sub>DC</sub>
Gate–Emitter Voltage	V <sub>GE</sub>	18	V <sub>DC</sub>
Collector Current–Continuous @ TC = 25°C – Pulsed	I <sub>C</sub>	15 50	A <sub>DC</sub> A <sub>AC</sub>
ESD (Human Body Model) R = 1500 Ω, C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	800	V
Total Power Dissipation @ TC = 25°C Derate above 25°C	PD	115 0.77	W W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

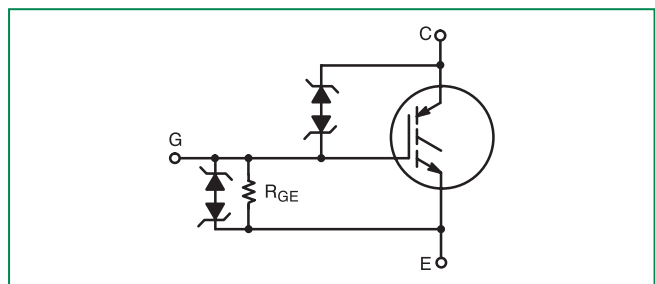
### Description

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

### Features

- Ideal for Coil–on–Plug Applications
- DPAK Package Offers Smaller Footprint for Increased Board Space
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage Interfaces Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Optional Gate Resistor (R<sub>G</sub>) and Gate–Emitter Resistor (R<sub>GE</sub>)
- Emitter Ballasting for Short–Circuit Capability
- These are Pb–Free Devices

### Functional Diagram



### Additional Information



Datasheet



Resources



Samples

**Unclamped Collector–to–Emitter Avalanche Characteristics ( $-55^{\circ}\leq T_J \leq 150^{\circ}\text{C}$ )**

Rating	Symbol	Value	Unit
Single Pulse Collector–to–Emitter Avalanche Energy			
$V_{CC} = 50\text{ V}, V_{GE} = 5.0\text{ V}, P_k I_L = 21.1\text{ A}, L = 1.8\text{ mH}, \text{Starting } T_J = 25^{\circ}\text{C}$	$E_{AS}$	400	mJ
$V_{CC} = 50\text{ V}, V_{GE} = 5.0\text{ V}, P_k I_L = 16.2\text{ A}, L = 3.0\text{ mH}, \text{Starting } T_J = 25^{\circ}\text{C}$		400	
$V_{CC} = 50\text{ V}, V_{GE} = 5.0\text{ V}, P_k I_L = 18.3\text{ A}, L = 1.8\text{ mH}, \text{Starting } T_J = 125^{\circ}\text{C}$		300	
Reverse Avalanche Energy			
$V_{CC} = 100\text{ V}, V_{GE} = 20\text{ V}, P_k I_L = 25.8\text{ A}, L = 6.0\text{ mH}, \text{Starting } T_J = 25^{\circ}\text{C}$	$E_{AS(R)}$	2000	mJ

**Maximum Short-Circuit Times ( $-55^{\circ}\leq T_J \leq 150^{\circ}\text{C}$ )**

Rating	Symbol	Value	Unit
Short Circuit Withstand Time 1 (See Figure 17, 3 Pulses with 10 ms Period)	$t_{sc1}$	750	$\mu\text{s}$
Short Circuit Withstand Time 2 (See Figure 18, 3 Pulses with 10 ms Period)	$t_{sc2}$	5.0	ms

**Thermal Characteristics**

Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient DPAK (Note 1)	$R_{\theta JA}$	95	$^{\circ}\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	$T_L$	275	$^{\circ}\text{C}$

**Electrical Characteristics - OFF**

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Collector–Emitter Clamp Voltage	$BV_{CES}$	$I_C = 2.0 \text{ mA}$	$T_J = -40^\circ\text{C to } 150^\circ\text{C}$	380	395	420	$V_{DC}$
		$I_C = 10 \text{ mA}$	$T_J = -40^\circ\text{C to } 150^\circ\text{C}$	390	405	430	
Zero Gate Voltage Collector Current	$I_{CES}$	$V_{CE} = 350 \text{ V}, V_{GE} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$	–	2.0	20	$\mu\text{A}_{DC}$
			$T_J = 150^\circ\text{C}$	–	10	40*	
			$T_J = -40^\circ\text{C}$	–	1.0	10	
		$V_{CE} = 15 \text{ V}, V_{GE} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$	–	–	2.0	
Reverse Collector–Emitter Leakage Current	$I_{ECS}$	$V_{CE} = -24 \text{ V}$	$T_J = 25^\circ\text{C}$	–	0.7	1.0	mA
			$T_J = 150^\circ\text{C}$	–	12	25*	
			$T_J = -40^\circ\text{C}$	–	0.1	1.0	
Reverse Collector–Emitter Clamp Voltage	$B_{V_{CES(R)}}$	$I_C = -75 \text{ mA}$	$T_J = 25^\circ\text{C}$	27	33	37	$V_{DC}$
			$T_J = 150^\circ\text{C}$	30	36	40	
			$T_J = -40^\circ\text{C}$	25	32	35	
Gate–Emitter Clamp Voltage	$BV_{GES}$	$I_G = 5.0 \text{ mA}$	$T_J = -40^\circ\text{C to } 150^\circ\text{C}$	11	13	15	$V_{DC}$
Gate–Emitter Leakage Current	$I_{GES}$	$V_{GE} = 10 \text{ V}$	$T_J = -40^\circ\text{C to } 150^\circ\text{C}$	384	640	700	$\mu\text{A}_{DC}$
Gate Emitter Resistor	$R_{GE}$	–	$T_J = -40^\circ\text{C to } 150^\circ\text{C}$	10	16	26	k $\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted.

Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. When surface mounted to an FR4 board using the minimum recommended pad size.

\*Maximum Value of Characteristic across Temperature Range.

**Electrical Characteristics - ON (Note 2)**

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Gate Threshold Voltage	$V_{GE(th)}$	$I_C = 1.0 \text{ mA}$ , $V_{GE} = V_{CE}$	$T_J = 25^\circ\text{C}$	1.1	1.4	1.9	$V_{DC}$
			$T_J = 150^\circ\text{C}$	0.75	1.0	1.4	
			$T_J = -40^\circ\text{C}$	1.2	1.6	2.1*	
Threshold Temperature Coefficient (Negative)	-	-	-	-	3.4	-	mV/°C
Collector-to-Emitter On-Voltage	$V_{CE(on)}$	$I_C = 6.0 \text{ A}$ , $V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.0	1.4	1.6	$V_{DC}$
			$T_J = 150^\circ\text{C}$	0.9	1.3	1.6	
			$T_J = -40^\circ\text{C}$	1.1	1.45	1.7*	
		$I_C = 8.0 \text{ A}$ , $V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.3	1.6	1.9*	
			$T_J = 150^\circ\text{C}$	1.2	1.55	1.8	
			$T_J = -40^\circ\text{C}$	1.4	1.6	1.9*	
		$I_C = 10 \text{ A}$ , $V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.4	1.8	2.05	
			$T_J = 150^\circ\text{C}$	1.4	1.8	2.0	
			$T_J = -40^\circ\text{C}$	1.4	1.8	2.1*	
		$I_C = 15 \text{ A}$ , $V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.8	2.2	2.5	
			$T_J = 150^\circ\text{C}$	2.0	2.4	2.6*	
			$T_J = -40^\circ\text{C}$	1.7	2.1	2.5	
		$I_C = 10 \text{ A}$ , $V_{GE} = 4.5 \text{ V}$	$T_J = 25^\circ\text{C}$	1.3	1.8	2.0*	
			$T_J = 150^\circ\text{C}$	1.3	1.75	2.0*	
			$T_J = -40^\circ\text{C}$	1.4	1.8	2.0*	
$I_C = 6.5 \text{ A}$ , $V_{GE} = 3.7 \text{ V}$	$T_J = 25^\circ\text{C}$	-	-	1.65			
Forward Transconductance	gfs	$V_{CE} = 5.0 \text{ V}$ , $I_C = 6.0 \text{ A}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	8.0	14	25	Mhos

**Dynamic Characteristics**

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Input Capacitance	$C_{ISS}$	$V_{CC} = 25 \text{ V}$ , $V_{GE} = 0 \text{ V}$ $f = 1.0 \text{ MHz}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	400	800	1000	pF
Output Capacitance	$C_{OSS}$			50	75	100	
Transfer Capacitance	$C_{RSS}$			4.0	7.0	10	

**Switching Characteristics**

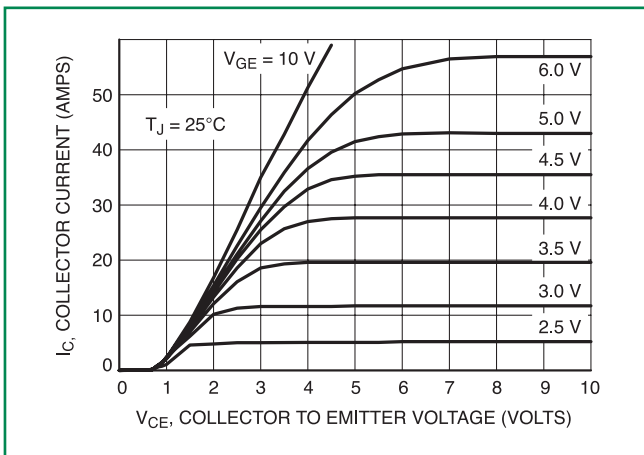
Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Turn-Off Delay Time (Resistive)	$t_{d(off)}$	$V_{CC} = 300\text{ V},$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega,$ $R_L = 46\ \Omega,$	$T_J = 25^\circ\text{C}$	-	4.0	10	$\mu\text{S}$
Fall Time (Resistive)	$t_f$	$V_{CC} = 300\text{ V},$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega,$ $R_L = 46\ \Omega,$	$T_J = 25^\circ\text{C}$	-	9.0	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{CC} = 10\text{ V},$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega,$ $R_L = 1.5\ \Omega,$	$T_J = 25^\circ\text{C}$	-	0.7	4.0	$\mu\text{S}$
Rise Time	$t_r$	$V_{CC} = 10\text{ V},$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega,$ $R_L = 1.5\ \Omega,$	$T_J = 25^\circ\text{C}$	-	4.5	7.0	

\*Maximum Value of Characteristic across Temperature Range.

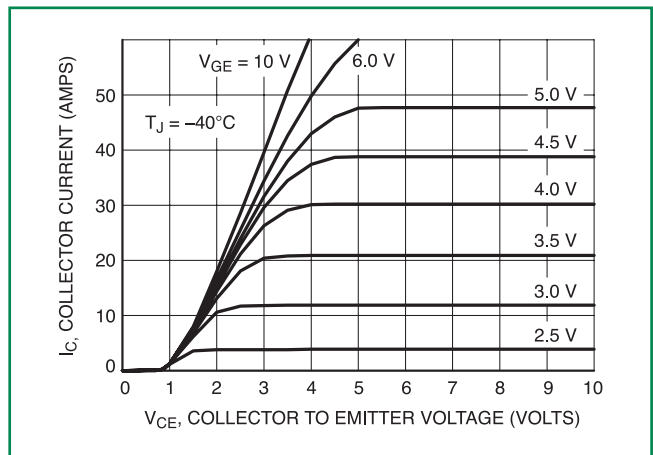
1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{S}$ , Duty Cycle  $\leq 2\%$ .

**Ratings and Characteristic Curves**

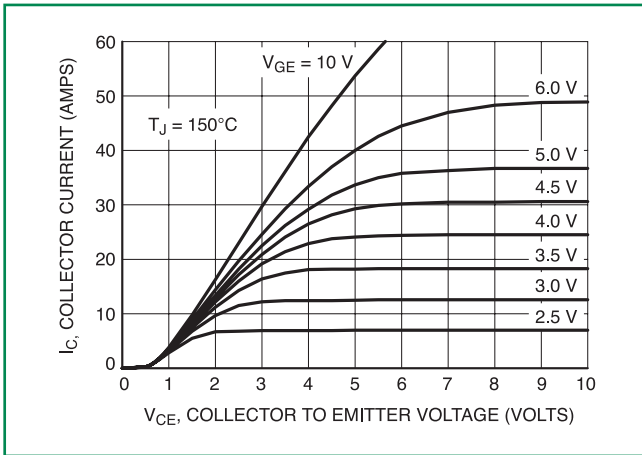
**Figure 1. Output Characteristics**



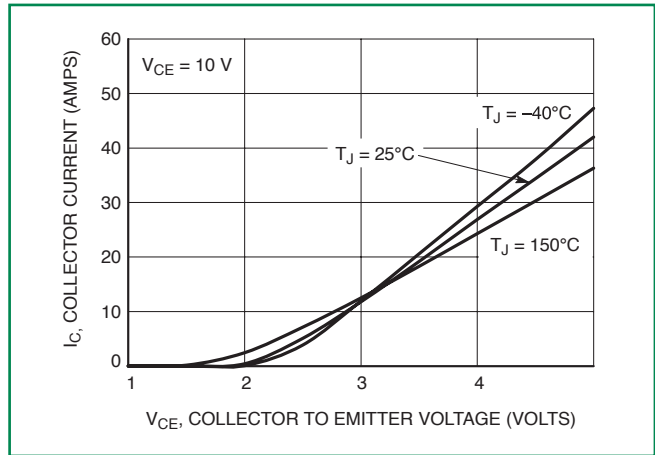
**Figure 2. Output Characteristics**



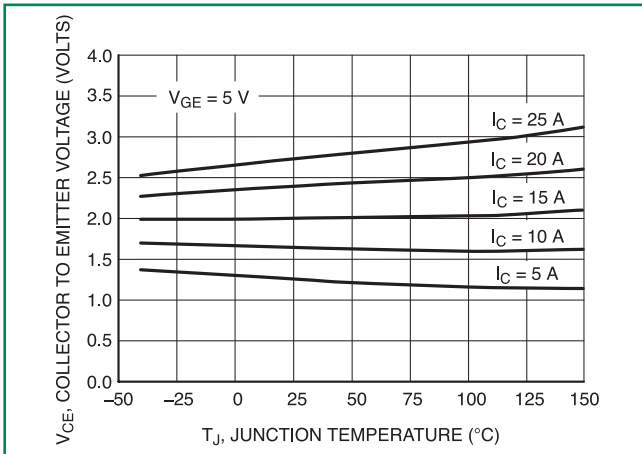
**Figure 3. Output Characteristics**



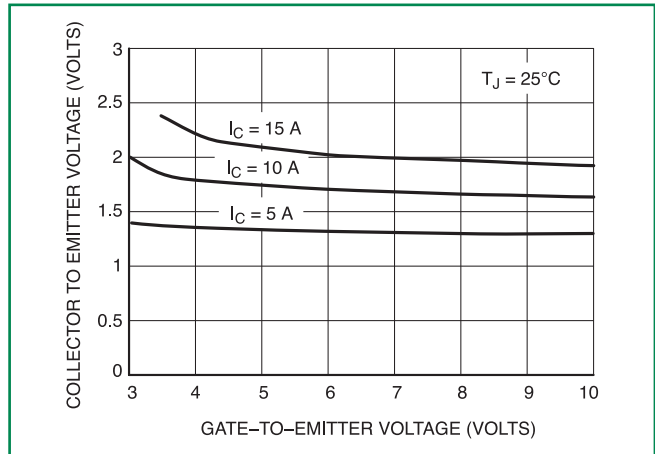
**Figure 4. Transfer Characteristics**



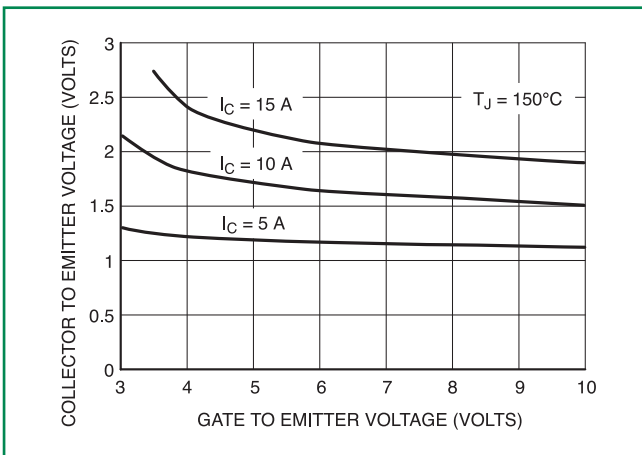
**Figure 5. Collector-to-Emitter Saturation Voltage vs Junction Temperature**



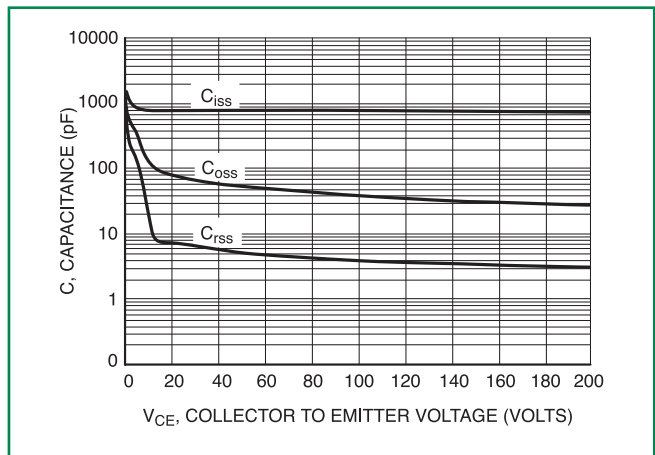
**Figure 6. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage**



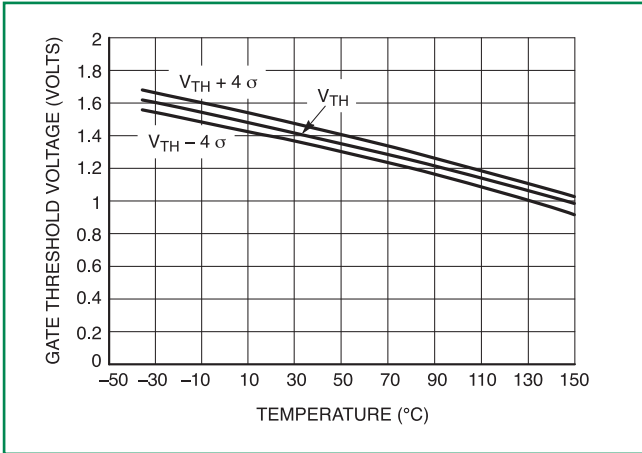
**Figure 7. Collector-to-Emitter Voltage vs Gate-to-Emitter Voltage**



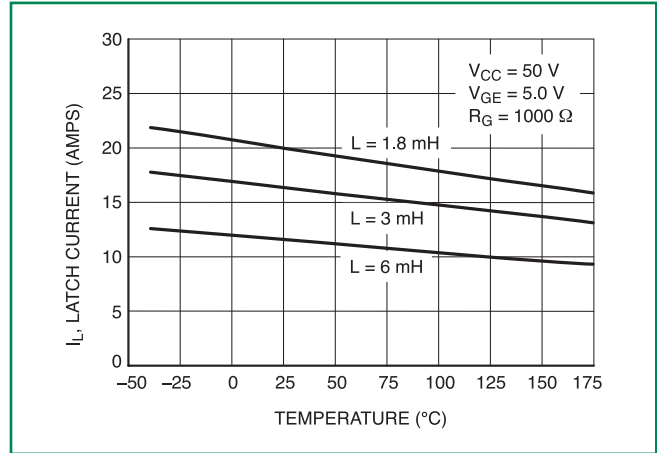
**Figure 8. Capacitance Variation**



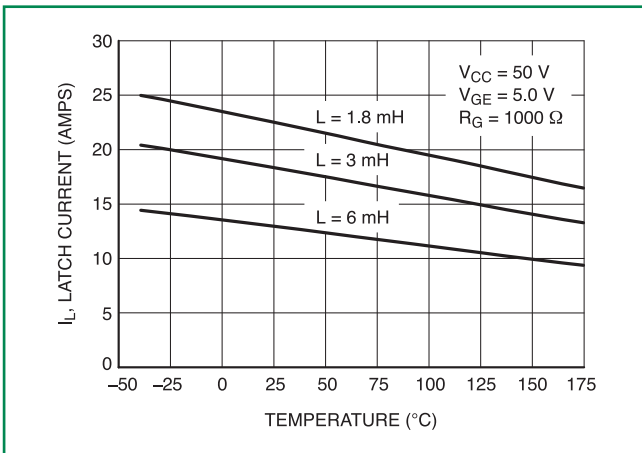
**Figure 9. Gate Threshold Voltage vs Temperature**



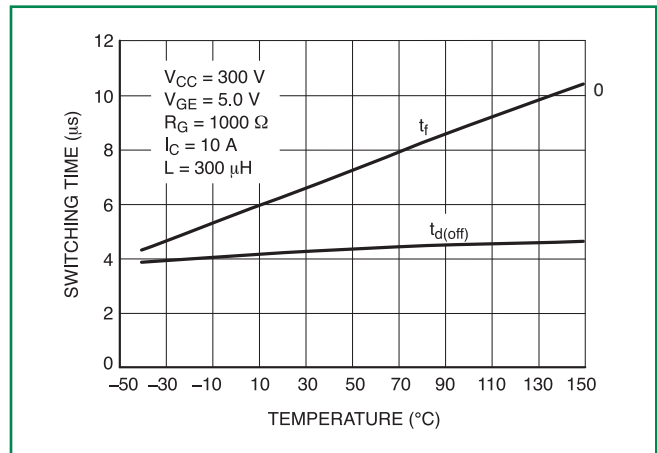
**Figure 10. Minimum Open Secondary Latch Current vs Temperature**



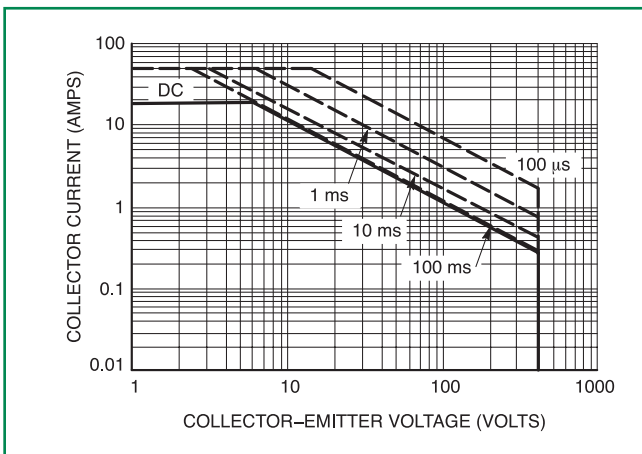
**Figure 11. Typical Open Secondary Latch Current vs Temperature**



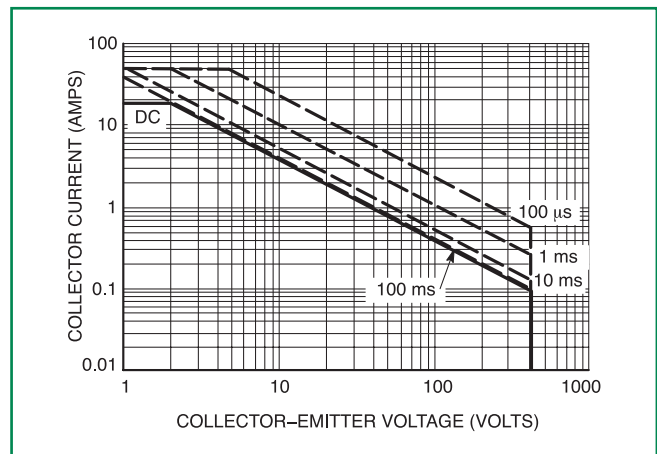
**Figure 12. Inductive Switching Fall Time vs Temperature**



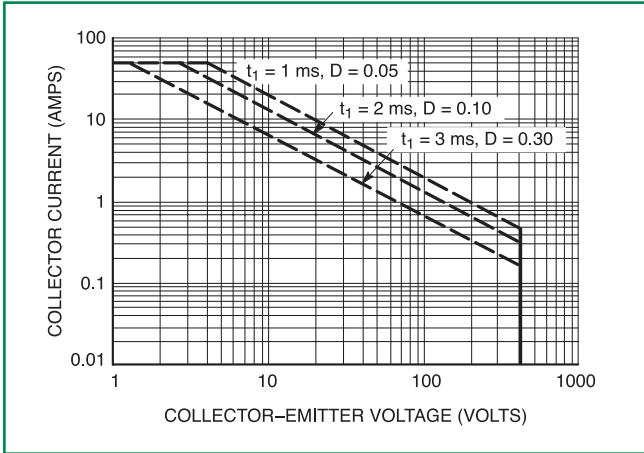
**Figure 13. Single Pulse Safe Operating Area**  
(Mounted on an Infinite Heatsink at  $T_A = 25^\circ\text{C}$ )



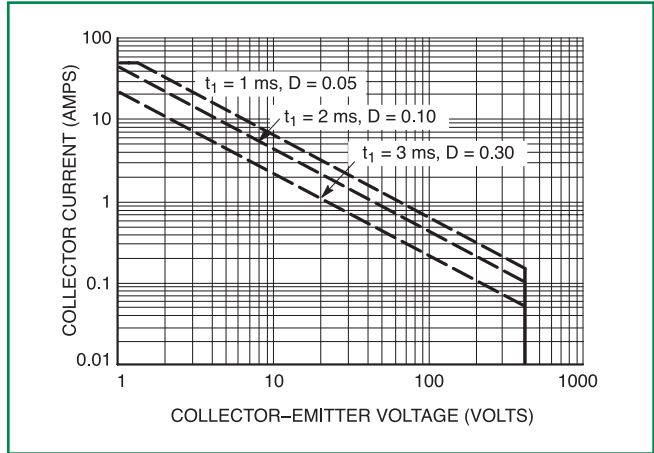
**Figure 14. Single Pulse Safe Operating Area**  
(Mounted on an Infinite Heatsink at  $T_A = 125^\circ\text{C}$ )



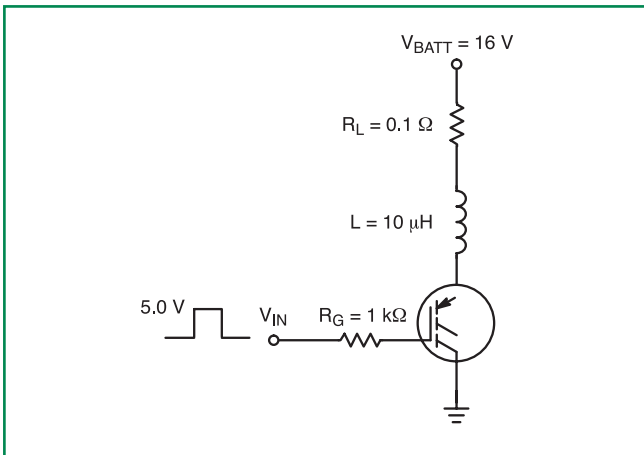
**Figure 15. Pulse Train Safe Operating Area**  
 (Mounted on an Infinite Heatsink at  $T_c = 25^\circ\text{C}$ )



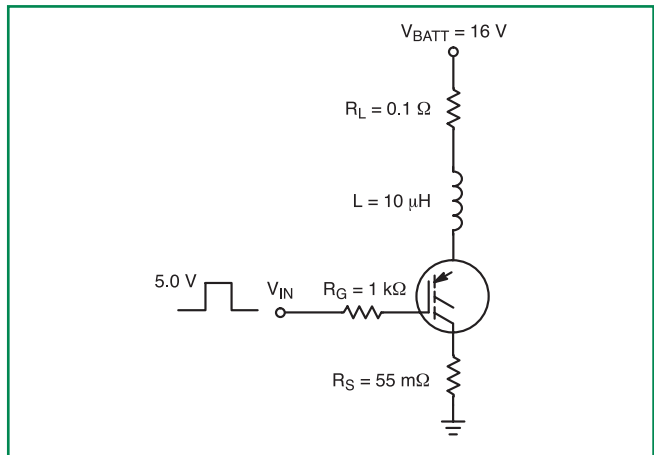
**Figure 15. Pulse Train Safe Operating Area**  
 (Mounted on an Infinite Heatsink at  $T_c = 125^\circ\text{C}$ )



**Figure 17. Circuit Configuration for Short Circuit Test #1**

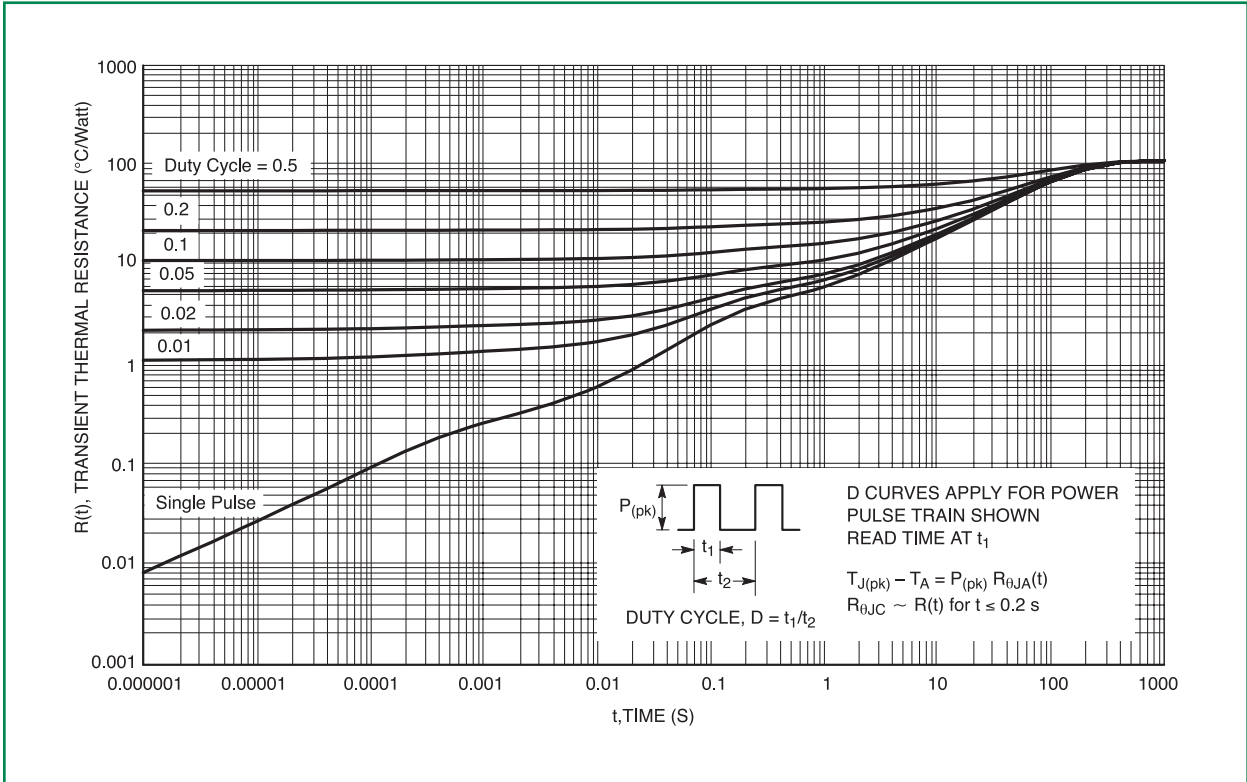


**Figure 18. Circuit Configuration for Short Circuit Test #2**

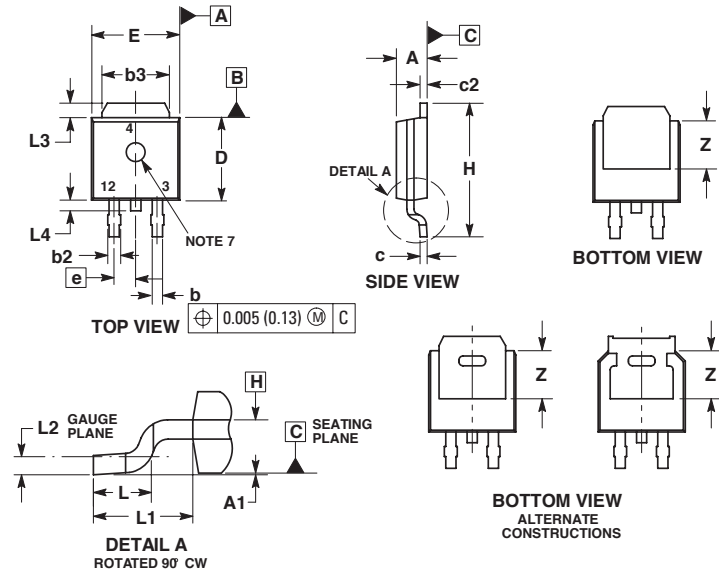




**Figure 19. Transient Thermal Resistance** (Non-normalized Junction-to-Ambient mounted on minimum pad area)



**Dimensions**

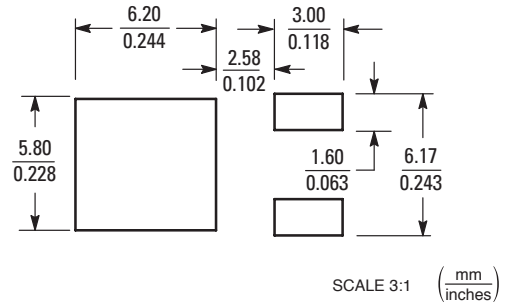


Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

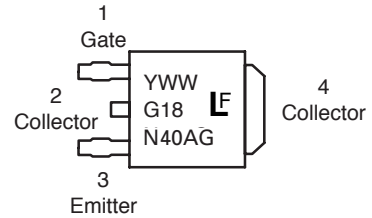
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

**Soldering Footprint**



**Part Marking System**



G18N40x= Device Code

- Y = Year
- WW = Work Week
- G = Pb-Free Device

**ORDERING INFORMATION**

Device	Package	Shipping†
NGD18N40ACLB4G	DPAK (Pb-Free)	2500 / Tape & Reel

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