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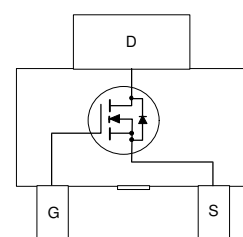
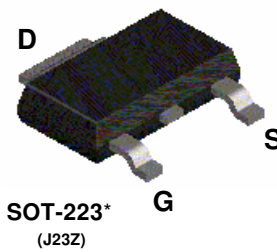
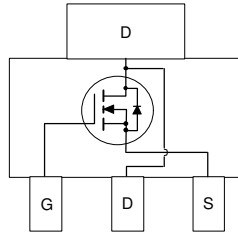
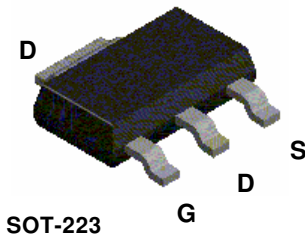
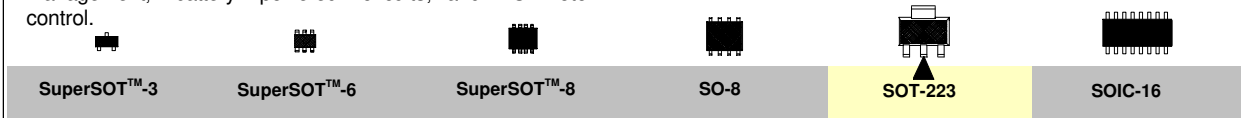
## FDT457N N-Channel Enhancement Mode Field Effect Transistor

### General Description

These N-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance. These products are well suited to low voltage, low current applications such as notebook computer power management, battery powered circuits, and DC motor control.

### Features

- 5 A, 30 V.  $R_{DS(ON)} = 0.06 \Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 0.090 \Omega @ V_{GS} = 4.5 \text{ V}$ .
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDT457N	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage - Continuous	$\pm 20$	V
$I_D$	Maximum Drain Current - Continuous (Note 1a)	5	A
	- Pulsed	16	
$P_D$	Maximum Power Dissipation (Note 1a)	3	W
	(Note 1b)	1.3	
	(Note 1c)	1.1	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C}/\text{W}$

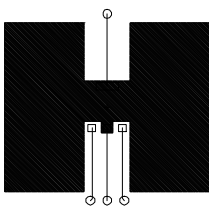
\* Order option J23Z for cropped center drain lead.

### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		35		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$T_J = 55^\circ\text{C}$			10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.6	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4.2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		0.043	0.06	$\Omega$
		$T_J = 125^\circ\text{C}$		0.065	0.1	
		$V_{GS} = 4.5\text{ V}, I_D = 3.8\text{ A}$		0.071	0.09	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 5\text{ A}$		5		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		235		$\mu\text{F}$
$C_{oss}$	Output Capacitance			145		
$C_{rss}$	Reverse Transfer Capacitance			50		
<b>SWITCHING CHARACTERISTICS (Note 2)</b>						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		5	10	ns
$t_r$	Turn - On Rise Time			12	22	
$t_{D(off)}$	Turn - Off Delay Time			12	22	
$t_f$	Turn - Off Fall Time			3	8	
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 5\text{ V}$		4.2	5.9	nC
$Q_{gs}$	Gate-Source Charge			1.3		
$Q_{gd}$	Gate-Drain Charge			1.7		
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				2.5	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.5\text{ A}$ (Note 2)		0.85	1.2	V

Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $42^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2oz Cu.



b.  $95^\circ\text{C/W}$  when mounted on a  $0.066\text{ in}^2$  pad of 2oz Cu.



c.  $110^\circ\text{C/W}$  when mounted on a  $0.00123\text{ in}^2$  pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Electrical Characteristics

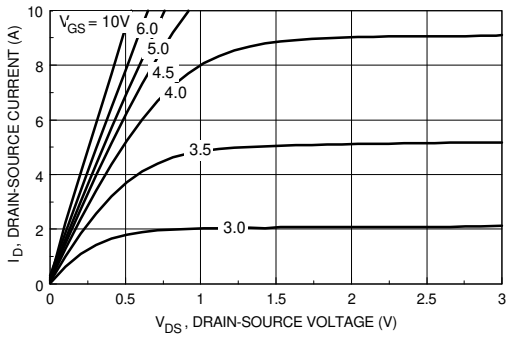


Figure 1. On-Region Characteristics.

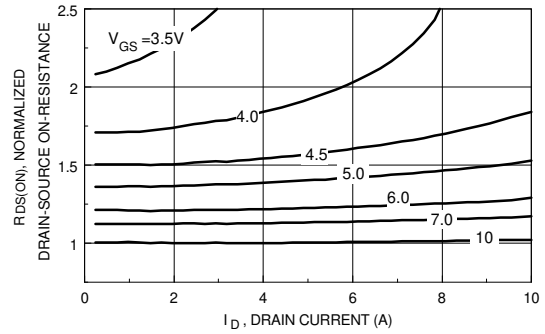


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

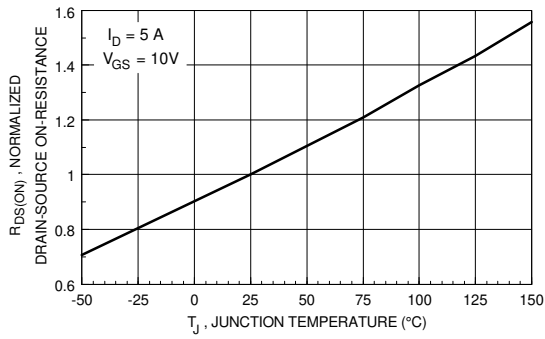


Figure 3. On-Resistance Variation with Temperature.

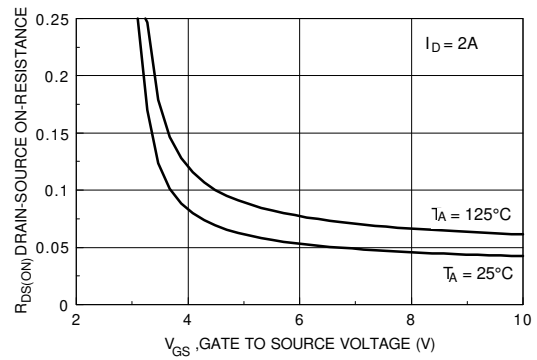


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

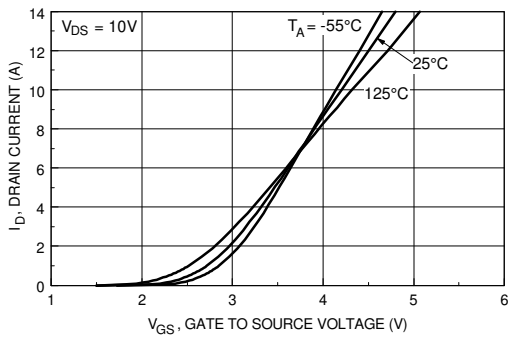


Figure 5. Transfer Characteristics.

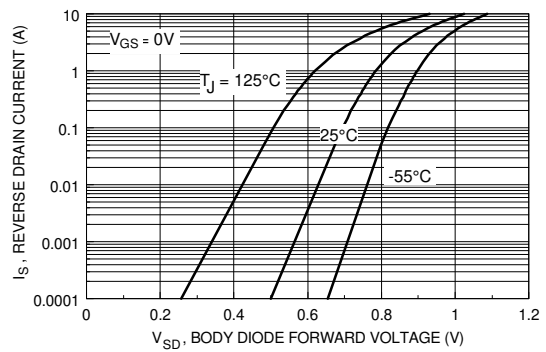


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics

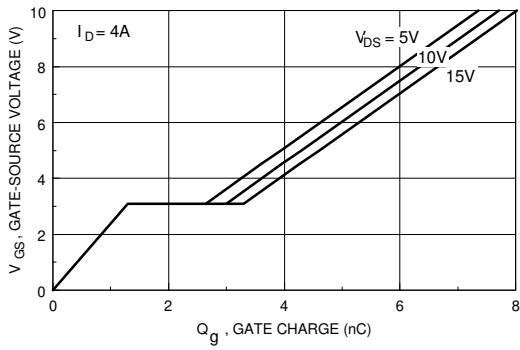


Figure 7. Gate Charge Characteristics.

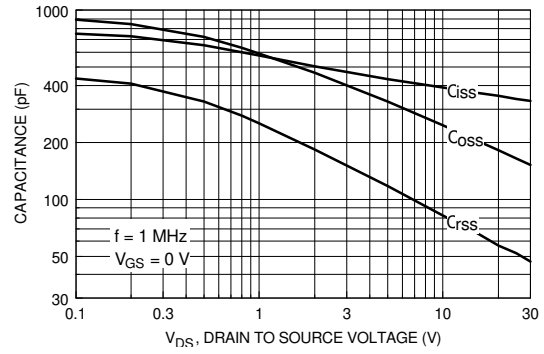


Figure 8. Capacitance Characteristics.

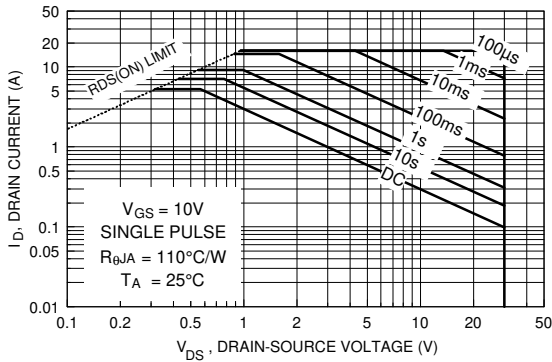


Figure 9. Maximum Safe Operating Area.

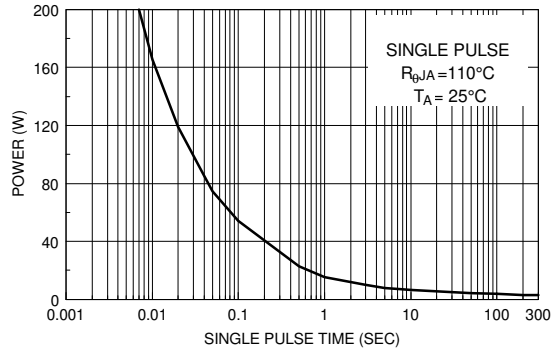


Figure 10. Single Pulse Maximum Power Dissipation.

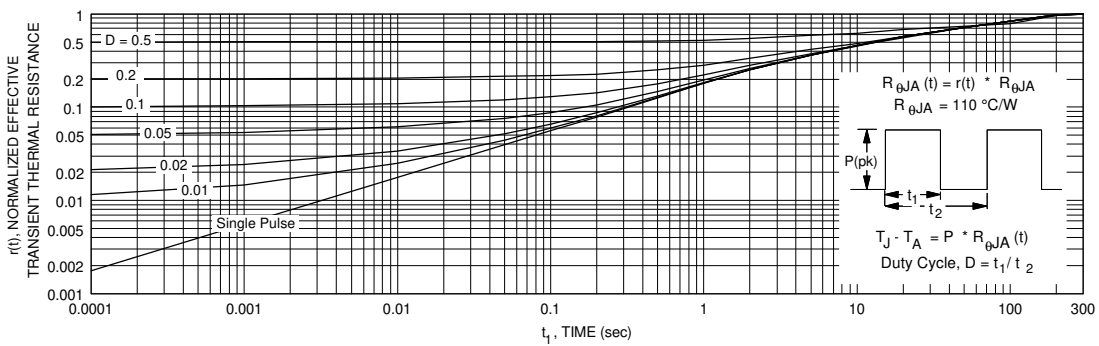



Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1c.  
Transient thermal response will change depending on the circuit board design.

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