

N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary (Typ. @ V_{GS} = 3.3V, T_A = +25°C)

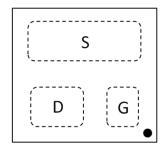
V _{DSS}	R _{DS(ON)}	Qg	Q _{gd}	I _D
12V	14.1mΩ	10.5nC	4.1nC	7.5A

Description

This new generation MOSFET is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high efficiency power transfer. Using Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal R_{DS(ON)} per footprint area.

Applications

- DC-DC Converters
- **Battery Management**
- Load Switch



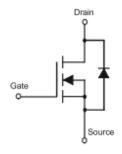
Top-View Pin Configuration

Features

- TR-MOS Technology with the Lowest R_{DS(ON)}: $R_{DS(ON)} = 14.1 m\Omega$ to Minimize On-State Losses
- CSP with Footprint 1.0mm × 1.0mm
- Height = 0.29mm for Low Profile
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

- Case: X3-DSN1010-3
- Terminal Connections: See Diagram Below
- Terminal Finish: Matte Tin Annealed Over Copper Pillar (3)
- Solder Cap Material: SnAg (Ag: 2.0+/-0.5%)



Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN1017UCP3-7	X3-DSN1010-3	3000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.</p>
 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

4B ΥM 4B = Product Type Marking Code YM = Date Code Marking Y or \overline{Y} = Year (ex: E = 2017) M or M = Month (ex: 9 = September)

Date Code Key

Year	201	6	2017		2018	20	19	2020		2021	2	2022
Code	D		E		F	(G	Н				J
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V_{DSS}	12	V	
Gate-Source Voltage	V _{GSS}	±8	V	
Continuous Drain Current @ V _{GS} = 3.3V (Note 5)	I _D	5.4 4.3	Α	
Continuous Drain Current @ V _{GS} = 3.3V (Note 6)	I _D	7.5 6.1	Α	
Pulsed Drain Current (Pulse Duration 10µs, Duty Cycle ≤1%	I _{DM}	15	Α	
Continuous Source-Drain Diode Current (Note 6)	I _S	1.47	Α	
Pulse Diode Forward Current (Note 6)	I _{SM}	15	Α	

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_{D}	0.74	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{ heta JA}$	167	°C/W
Total Power Dissipation (Note 6)	P _D	1.47	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{ heta JA}$	85	°C/W
Operating and Storage Temperature Range	$T_{J_1}T_{STG}$	-55 to +150	°C

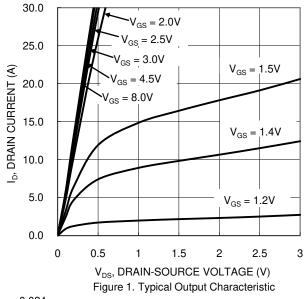
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

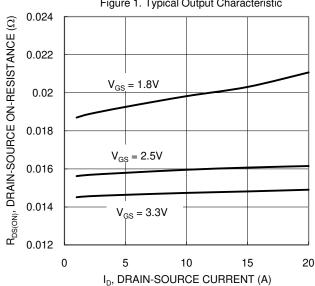
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	12	_	-	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}		_	1.0	μΑ	$V_{DS} = 9.6V, V_{GS} = 0V$	
Gate-Body Leakage	I _{GSS}		_	±100	nA	$V_{GS} = \pm 8V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(TH)}	0.4	0.7	1.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
		_	14.1	17.0		$V_{GS} = 3.3V, I_D = 5.0A$	
		_	14.4	19.0		$V_{GS} = 3.0V, I_D = 5.0A$	
		-	15.5	21.0		$V_{GS} = 2.5V, I_D = 5.0A$	
Static Drain-Source On-Resistance	R _{DS(ON)}		16.0	23.0	mΩ	$V_{GS} = 2.3V, I_D = 5.0A$	
		-	16.8	24.0		$V_{GS} = 2.1V, I_D = 5.0A$	
			21.3	34.0		$V_{GS} = 2.1V$, $I_D = 5.0A$, $+125$ °C (Note 8)	
		1	20.0	30.0		$V_{GS} = 1.8V, I_D = 3.0A$	
Forward Transfer Admittance	Y _{fs}	_	6.6	_	S	$V_{DS} = 6V, I_{S} = 1.0A$	
Body Diode Forward Voltage	V_{SD}	_	0.7	1	V	$V_{GS} = 0V, I_{S} = 1.0A$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	_	1002	1503	pF	.,	
Output Capacitance	Coss	-	312	468	pF	V _{DS} = 6V, V _{GS} = 0V, f = 1.0MHz	
Reverse Transfer Capacitance	C_{rss}	-	259	389	pF	1 - 1.0WH 12	
Gate Resistance	R_g	1	2.2	4.4	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge	Q_g	1	10.5	16	nC	V 2 2V V 6V	
Gate-Source Charge	Q_{gs}		1.0	1.5	nC	$V_{GS} = 3.3V, V_{DS} = 6V,$ $I_{D} = 5.0A$	
Gate-Drain Charge	Q_{gd}		4.1	6.2	nC	ID = 5.0A	
Turn-On Delay Time	t _{D(ON)}	1	3.7	10	ns		
Turn-On Rise Time	t _R		6.3	15	ns	$V_{DD} = 6V, I_D = 5.0A$	
Turn-Off Delay Time	t _{D(OFF)}	_	17.9	35	ns	$V_{GEN} = 4.5V, R_G = 1\Omega, R_L = 1.2\Omega$	
Turn-Off Fall Time	t _F	_	7.5	15	ns]	
Reverse Recovery Charge	Q _{RR}	_	2.7	5	nC	L 54 di/dt 1004/up	
Body Diode Reverse Recovery Time	t _{RR}		14.2	28	ns	I _F = 5A, di/dt = 100A/μs	

 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 7. Short duration pulse test used to minimize self-heating effect.
 8. Guaranteed by design. Not subject to production testing. Notes:









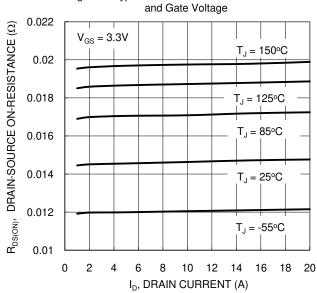
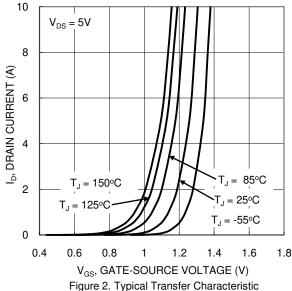


Figure 3. Typical On-Resistance vs. Drain Current

Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature



0.2 $R_{DS(ON)}$, DRAIN-SOURCE ON-RESISTANCE (Ω) 0.18 0.16 0.14 $I_D = 5A$ 0.12 0.1 0.08 0.06 0.04 0.02 0 0 3 4 5 6 8 V_{GS}, GATE-SOURCE VOLTAGE (V) Figure 4. Typical Transfer Characteristic

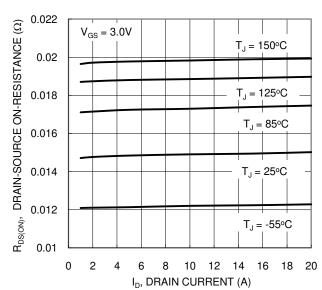


Figure 6. Typical On-Resistance vs. Drain Current and Junction Temperature



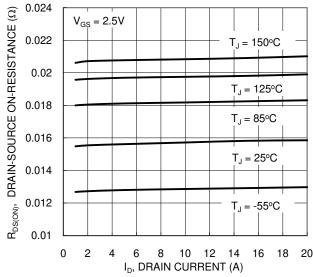


Figure 7. Typical On-Resistance vs. Drain Current and Junction Temperature

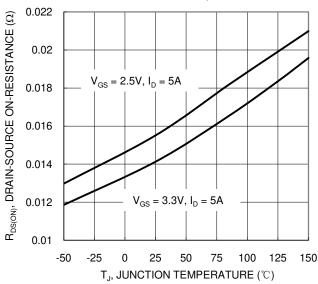


Figure 9. On-Resistance Variation with Junction Temperature

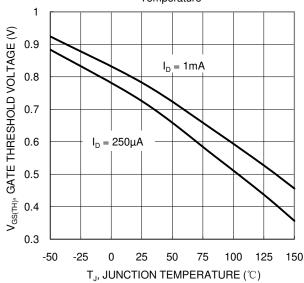


Figure 11. Gate Threshold Variation vs. Junction Temperature

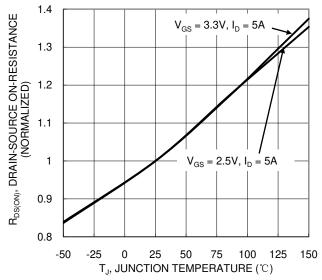


Figure 8. On-Resistance Variation with Junction Temperature

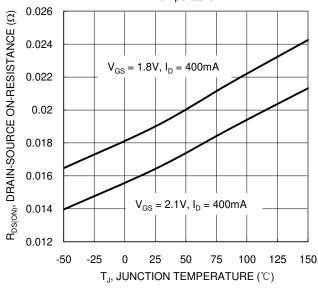


Figure 10. On-Resistance Variation with Junction Temperature

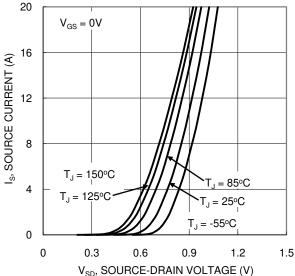
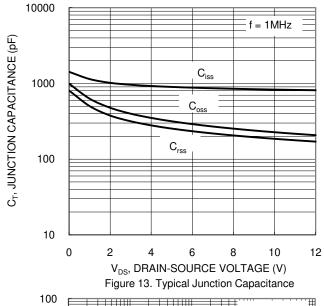
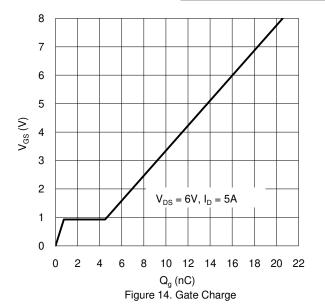


Figure 12. Diode Forward Voltage vs. Current









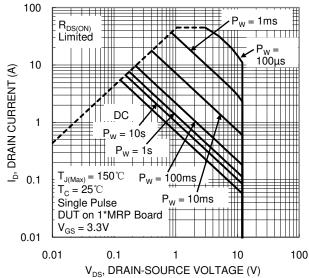


Figure 15. SOA, Safe Operation Area

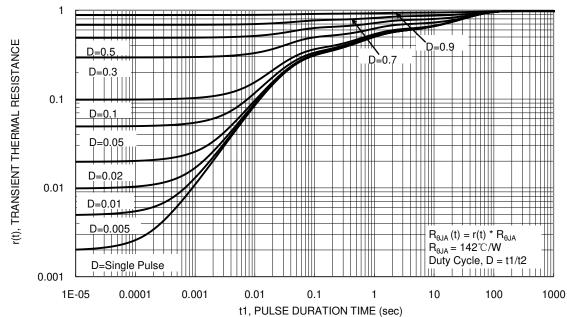


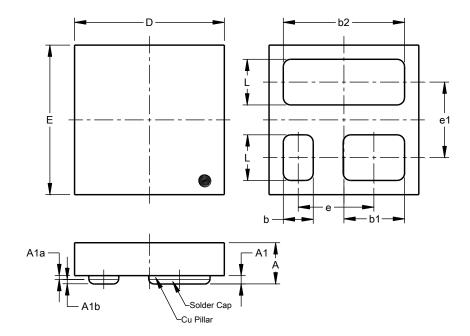
Figure 16. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X3-DSN1010-3

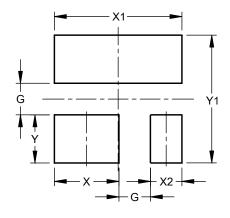


X3-DSN1010-3						
Dim	Min	Max	Тур			
Α	-	0.29	0.27			
A1	0.034	0.046	0.04			
A1a	0.015	0.025	0.02			
A1b	0.017	0.023	0.02			
b	0.18	0.22	0.20			
b1	0.39	0.43	0.41			
b2	0.79	0.83	0.81			
D	0.92	1.00	0.96			
Е	0.92	1.00	0.96			
е	-	-	0.505			
e1	-	-	0.505			
L	0.285	0.325	0.305			
All Dimensions in mm						

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X3-DSN1010-3



Dimensions	(in mm)		
G	0.200		
X	0.410		
X1	0.810		
X2	0.200		
Υ	0.305		
Y1	0.810		



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