





P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

| BV _{DSS} | R _{DS(ON)} max | I _D T _A = +25°C |
|-------------------|--------------------------------|--|
| | $45m\Omega$ @ $V_{GS} = -4.5V$ | -4.3A |
| -20V | $58m\Omega @ V_{GS} = -2.5V$ | -3.8A |
| | 90mΩ @ V _{GS} = -1.8V | -3.1A |

Description

This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power Management Functions

SOT23





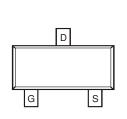
Top View

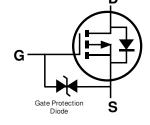
Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208 63
- Terminals Connections: See Diagram Below
- Weight: 0.009 grams (Approximate)





Top View Internal Schematic

Equivalent Circuit

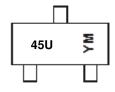
Ordering Information (Note 4)

| Part Number | Compliance | Case | Packaging |
|-------------|------------|-------|--------------------|
| DMP2045U-7 | Standard | SOT23 | 3,000/Tape & Reel |
| DMP2045U-13 | Standard | SOT23 | 10,000/Tape & Reel |

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information



 $45U = Product Type Marking Code YM or <math>\overline{Y}M = Date Code Marking Y or \overline{Y} = Year (ex: F = 2018) M = Month (ex: 9 = September)$

Date Code Key

| Year | 2017 | 20 | 18 | 2019 | 20 | 020 | 2021 | 2 | 2022 | 2023 | | 2024 |
|-------|------|-----|-----|------|-----|-----|------|-----|------|------|-----|------|
| Code | E | F | | G | | Н | | | J | K | | L |
| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | N | D |



| Characteristic | Symbol | Value | Unit |
|---|-----------------|--------------|------|
| Drain-Source Voltage | V_{DSS} | -20 | V |
| Gate-Source Voltage | V_{GSS} | ±8 | V |
| Continuous Drain Current (Note 6) V _{GS} = -4.5V | ΙD | -4.3 -3.5 | Α |
| Maximum Continuous Body Diode Forward Current (| ls | -1.2 | Α |
| Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%) | I _{DM} | -25 | A |

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Value | Unit | |
|--|--------------|-----------------------------------|-------------|------|
| Total Power Dissipation (Note 5) | | P_{D} | 0.8 | W |
| Thermal Resistance, Junction to Ambient (Note 5) | Steady State | $R_{\theta JA}$ | 154 | °C/W |
| Total Power Dissipation (Note 6) | | P _D | 1.2 | W |
| Thermal Resistance, Junction to Ambient (Note 6) | Steady State | $R_{	heta JA}$ | 98 | °C/W |
| Operating and Storage Temperature Range | | T _J , T _{STG} | -55 to +150 | °C |

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Min | Тур | Max | Unit | Test Condition | |
|--|---------------------|------|------|------|------|--|--|
| OFF CHARACTERISTICS (Note 7) | | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | -20 | | | V | $V_{GS} = 0V, I_D = -250\mu A$ | |
| Zero Gate Voltage Drain Current $T_J = +25$ °C | I _{DSS} | | | -1 | μΑ | $V_{DS} = -20V, V_{GS} = 0V$ | |
| Gate-Source Leakage | I _{GSS} | _ | _ | ±10 | μΑ | $V_{GS} = \pm 8.0V, V_{DS} = 0V$ | |
| ON CHARACTERISTICS (Note 7) | | | | | | | |
| Gate Threshold Voltage | V _{GS(TH)} | -0.3 | | -1.0 | V | $V_{DS} = V_{GS}$, $I_D = -250\mu A$ | |
| | | _ | 32 | 45 | | $V_{GS} = -4.5V, I_D = -4.0A$ | |
| Static Drain-Source On-Resistance | R _{DS(ON)} | _ | 42 | 58 | mΩ | $V_{GS} = -2.5V, I_D = -3.5A$ | |
| | | | 54 | 90 | | $V_{GS} = -1.8V, I_D = -1.0A$ | |
| Diode Forward Voltage | V_{SD} | _ | -0.7 | -1.2 | V | $V_{GS} = 0V, I_S = -1.0A$ | |
| DYNAMIC CHARACTERISTICS (Note 8) | | | | | | | |
| Input Capacitance | Ciss | _ | 634 | _ | pF | ., ,,,,, | |
| Output Capacitance | Coss | | 81 | _ | pF | $V_{DS} = -10V, V_{GS} = 0V$ f = 1.0MHz | |
| Reverse Transfer Capacitance | C _{rss} | | 66 | _ | pF | 1 - 1.500112 | |
| Gate Resistance | R_g | | 20 | _ | Ω | $V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1.0MHz$ | |
| Total Gate Charge | Q_g | - | 6.8 | _ | nC | | |
| Gate-Source Charge | Q _{gs} | _ | 0.7 | _ | nC | $V_{GS} = -4.5V, V_{DS} = -10V$ $I_{D} = -4A$ | |
| Gate-Drain Charge | Q_{gd} | _ | 1.6 | _ | nC | 1D = -4A | |
| Turn-On Delay Time | t _{D(ON)} | _ | 4.2 | _ | ns | | |
| Turn-On Rise Time | t _R | _ | 3.4 | _ | ns | $V_{DD} = -10V, V_{GS} = -4.5V,$ | |
| Turn-Off Delay Time | t _{D(OFF)} | _ | 23 | _ | ns | $R_L = 3.3\Omega$, $R_G = 1\Omega$ | |
| Turn-Off Fall Time | t _F | _ | 9.6 | _ | ns | | |
| Reverse Recovery Time | t _{RR} | _ | 1.8 | _ | ns | $I_F = -1.0A$, $di/dt = 100A/\mu s$ | |
| Reverse Recovery Charge | Q _{RR} | _ | 9.4 | _ | nC | $I_F = -1.0A$, $di/dt = 100A/\mu s$ | |

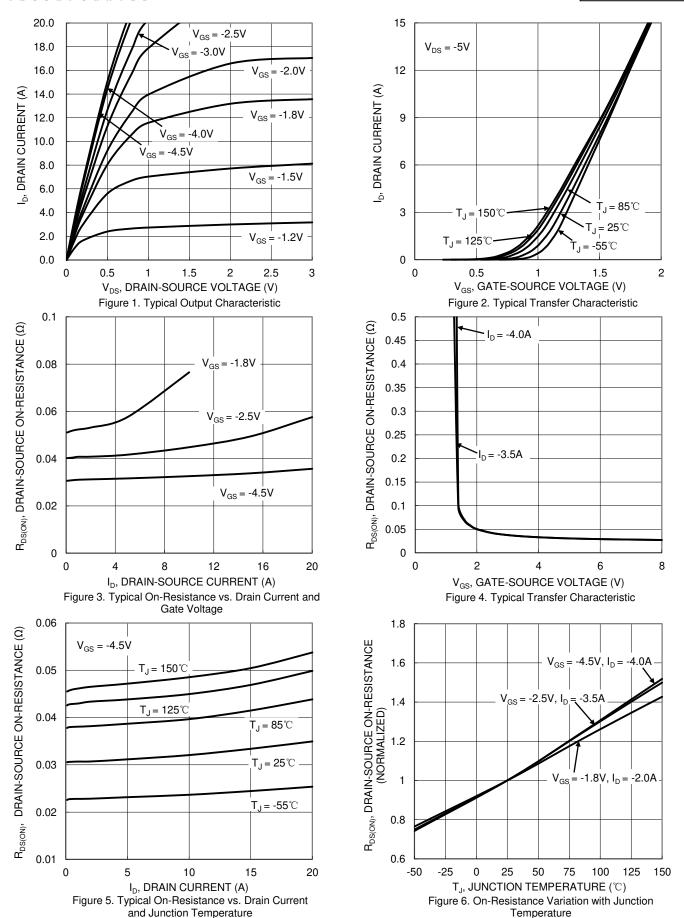
Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

^{6.} Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

^{7.} Short duration pulse test used to minimize self-heating effect.

^{8.} Guaranteed by design. Not subject to product testing.









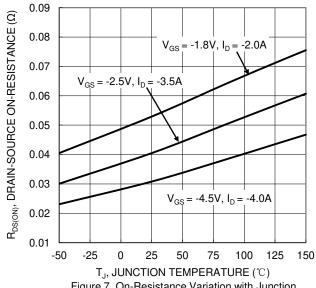


Figure 7. On-Resistance Variation with Junction Temperature

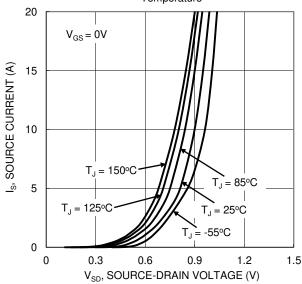
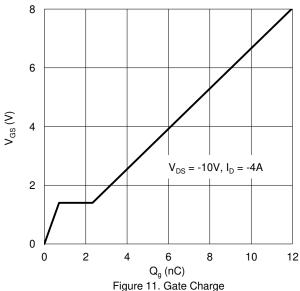
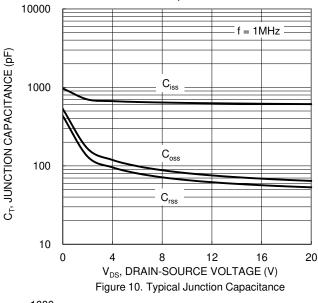


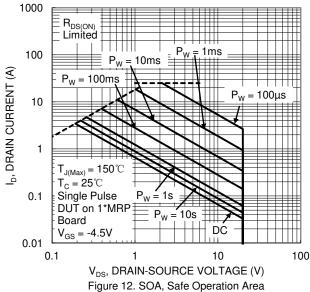
Figure 9. Diode Forward Voltage vs. Current



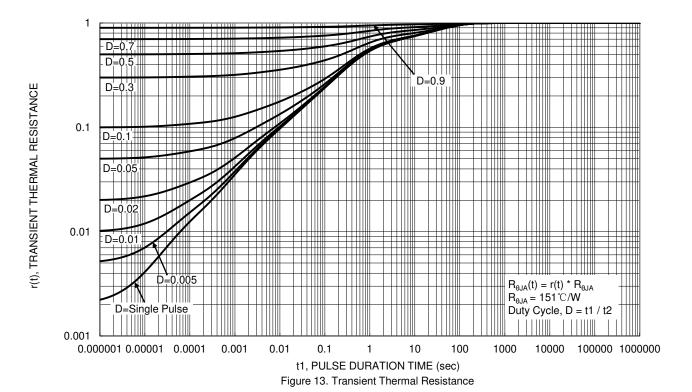
8.0 $V_{\text{GS}(\text{TH})},$ GATE THRESHOLD VOLTAGE (V) 0.7 0.6 0.5 $I_D = -1mA$ 0.4 0.3 $I_D = -250 \mu A$ 0.2 0.1 0 -50 -25 0 25 50 75 100 125 150 T., JUNCTION TEMPERATURE (°C)

Figure 8. Gate Theshold Variation vs. Junction Temperature







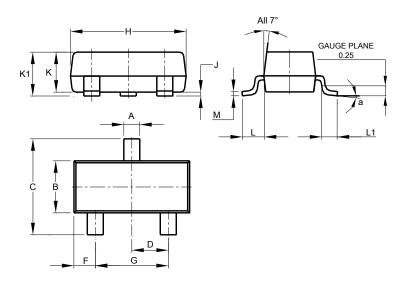




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23

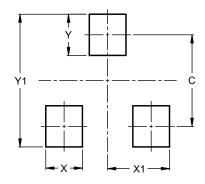


| SOT23 | | | | | | | |
|----------------------|-------|-------|-------|--|--|--|--|
| Dim | Min | Max | Тур | | | | |
| Α | 0.37 | 0.51 | 0.40 | | | | |
| В | 1.20 | 1.40 | 1.30 | | | | |
| С | 2.30 | 2.50 | 2.40 | | | | |
| D | 0.89 | 1.03 | 0.915 | | | | |
| F | 0.45 | 0.60 | 0.535 | | | | |
| G | 1.78 | 2.05 | 1.83 | | | | |
| H | 2.80 | 3.00 | 2.90 | | | | |
| J | 0.013 | 0.10 | 0.05 | | | | |
| K | 0.890 | 1.00 | 0.975 | | | | |
| K1 | 0.903 | 1.10 | 1.025 | | | | |
| L | 0.45 | 0.61 | 0.55 | | | | |
| L1 | 0.25 | 0.55 | 0.40 | | | | |
| M | 0.085 | 0.150 | 0.110 | | | | |
| а | 0° 8° | | | | | | |
| All Dimensions in mm | | | | | | | |

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23



| Dimensions | Value (in mm) |
|------------|---------------|
| С | 2.0 |
| Х | 0.8 |
| X1 | 1.35 |
| Υ | 0.9 |
| Y1 | 2.9 |



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