# N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVN4210A

ISSUE 2 – MARCH 94

FEATURES

* 100 Volt V_{DS}
* $R_{DS(on)}$= 1.5Ω
* Spice model available
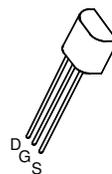
E-Line
TO92 Compatible

D
G
S

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current at T_{amb}=25°C	I_D	450	mA
Pulsed Drain Current	I_{DM}	6	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation at T_{amb}=25°C	P_{tot}	700	mW
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

| PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	100		V	I_D=1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.8	2.4	V	ID=1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}		100	nA	V_{GS}=± 20V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}		10 100	µA µA	V_{DS}=100V, V_{GS}=0 V_{DS}=80V, V_{GS}=0V, T=125°C(2)
On-State Drain Current(1)	$I_{D(on)}$	2.5		A	V_{DS}=25V, V_{GS}=10V
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		1.5 1.8	Ω	V_{GS}=10V,I_D=1.5A V_{GS}=5V,I_D=500mA
Forward Transconductance(1)(2)	g_{fs}	250		mS	V_{DS}=25V,I_D=1.5A
Input Capacitance (2)	C_{iss}		100	pF	V_{DS}=25V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}		40	pF	
Reverse Transfer Capacitance (2)	C_{rss}		12	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		4	ns	V_{DD}≈25V, I_D=1.5A
Rise Time (2)(3)	t_r		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		20	ns	
Fall Time (2)(3)	t_f		30	ns	

TYPICAL CHARACTERISTICS
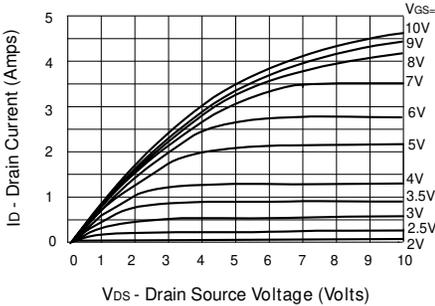
Saturation Characteristics
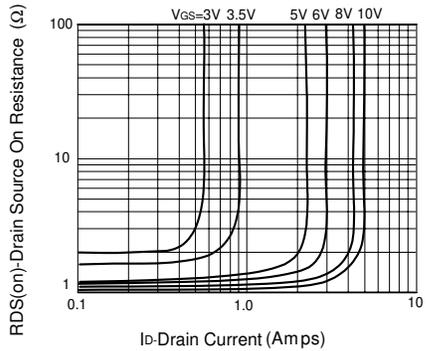
On-resistance v drain current


Normalised R_{DS(on)} and V_{GS(th)} v Temperature
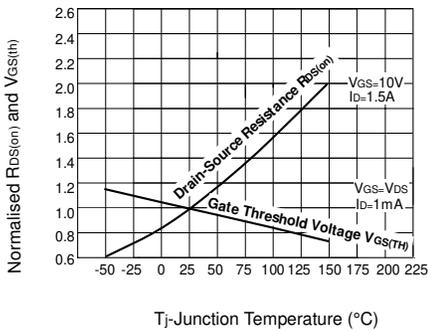
Normalised R$_{DS(on)}$ and V$_{GS(th)}$ v Temperature
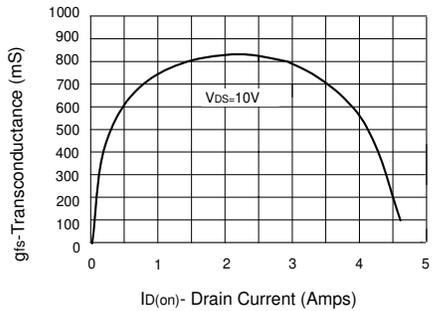

Transconductance v drain current
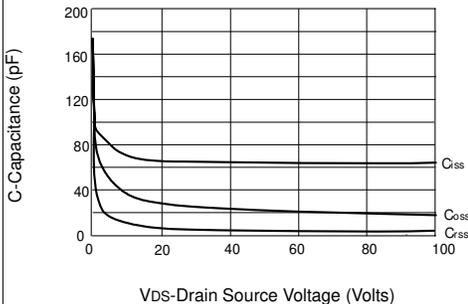
Capacitance v drain-source voltage
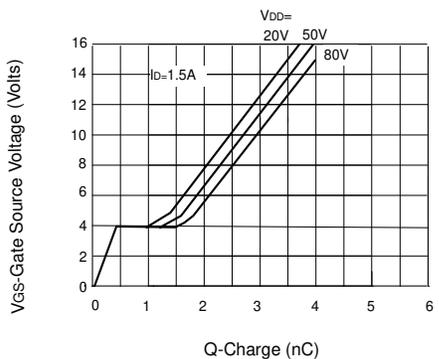
Gate charge v gate-source voltage