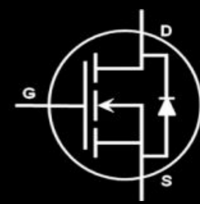
EPC8010 – Enhancement Mode Power Transistor

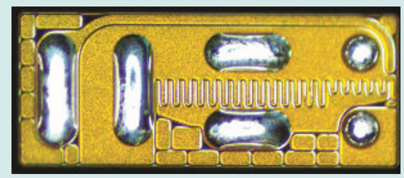
V_{DS} , 100 V
$R_{DS(on)}$, 160 mΩ
I_D , 2.7 A

New Product



Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
I_D	Continuous (T_A = 25˚C, $R_{θJA}$ = 57˚C/W)	2.7	A
	Pulsed (25˚C, T_{Pulse} = 300 µs)	7.5	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	



EPC8010 eGaN FETs are supplied only in passivated die form with solder bars

Applications
- Ultra High Speed DC-DC Conversion
- RF Envelope Tracking
- Wireless Power Transfer
- Game Console and Industrial Movement Sensing (LiDAR)

Benefits
- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

Static Characteristics (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	100			V
I_{DSS}	Drain Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		20	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.1	0.5	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		20	100	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.25 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 0.5 A		120	160	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		2.5		V

Specifications are with substrate shorted to source where applicable.

Thermal Characteristics			
		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction to Case	8.2	˚C/W
$R_{θJB}$	Thermal Resistance, Junction to Board	16	˚C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient (Note 1)	82	˚C/W

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J = 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		43	55	pF
C_{OSS}	Output Capacitance			25	36	
C_{RSS}	Reverse Transfer Capacitance			0.3	0.5	
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 1 A		360	480	pC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 1 A		130		
Q_{GD}	Gate-to-Drain Charge			60	100	
$Q_{G(TH)}$	Gate Charge at Threshold			100		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		2200	3300	
Q_{RR}	Source-Drain Recovery Charge			0		

Specifications are with substrate shorted to source where applicable.

Figure 1: Typical Output Characteristics at 25°C

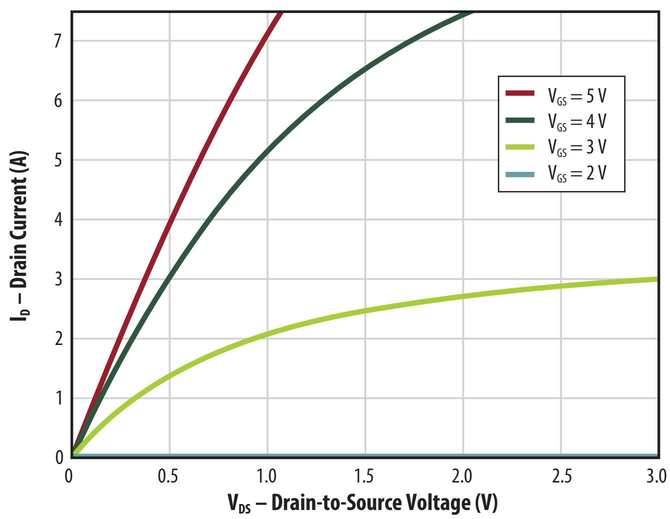


Figure 2: Transfer Characteristics

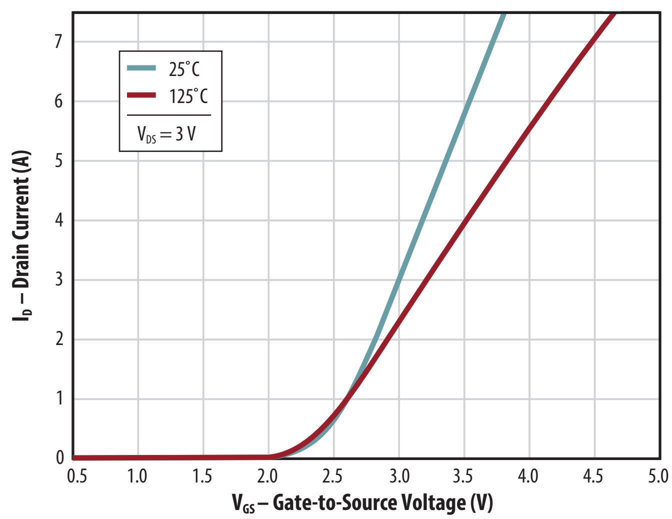


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

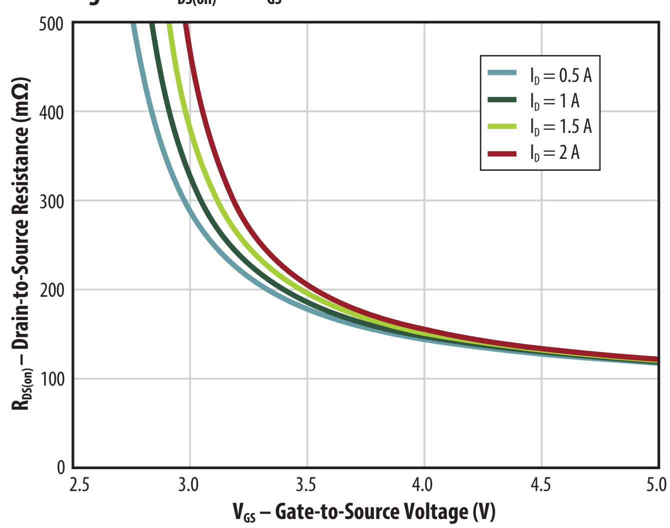


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

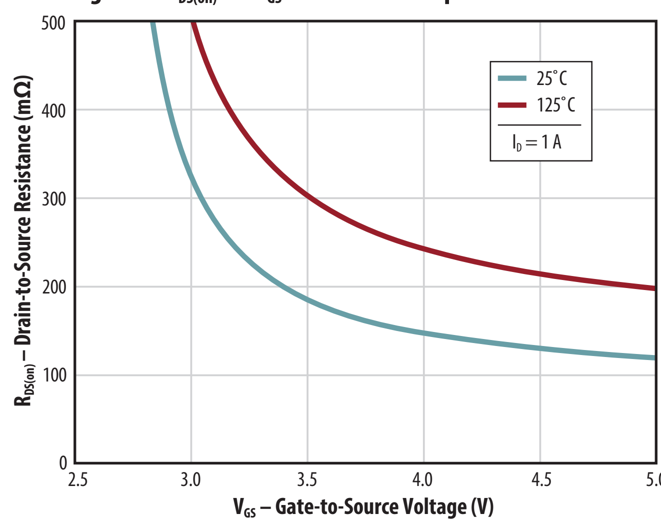


Figure 5a: Capacitance (Linear Scale)

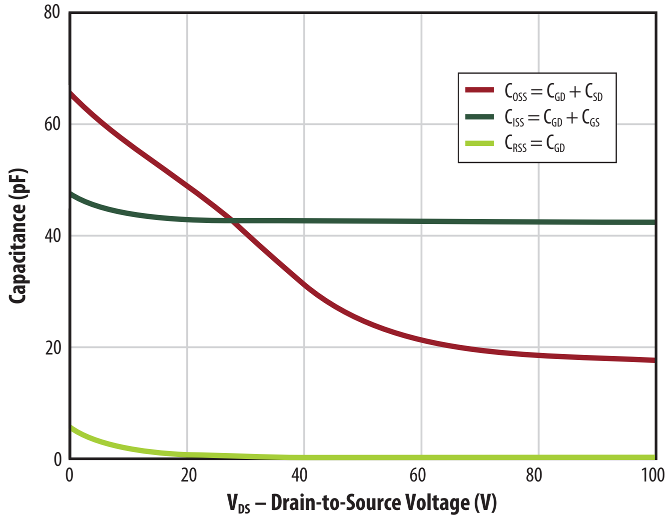


Figure 5b: Capacitance (Log Scale)

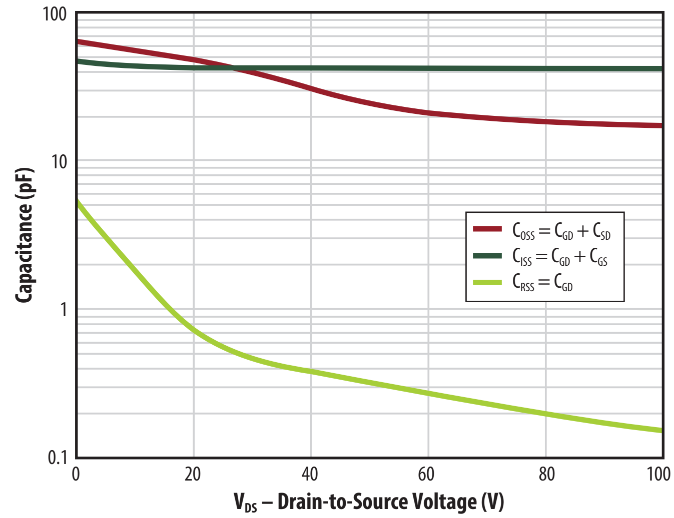


Figure 6: Gate Charge

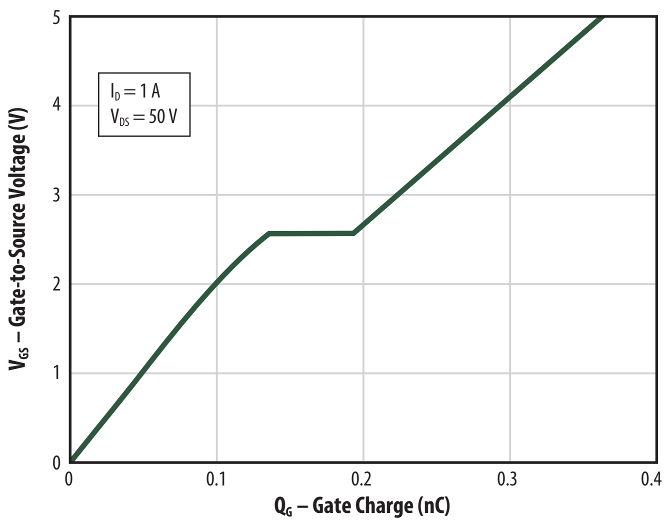


Figure 7: Reverse Drain-Source Characteristics

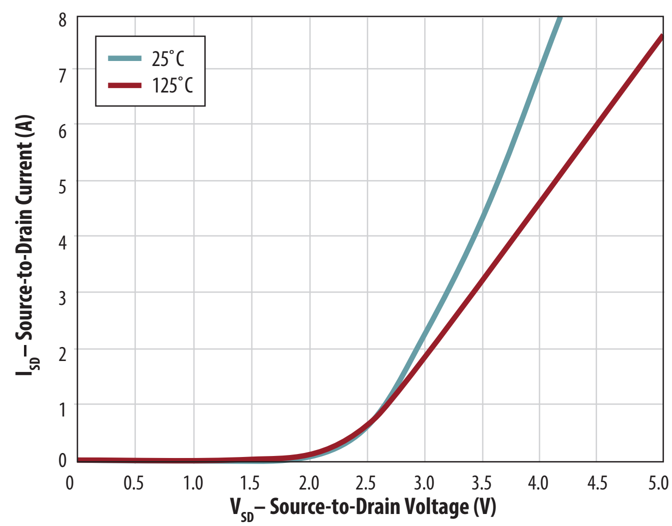


Figure 8: Normalized On-State Resistance vs. Temperature

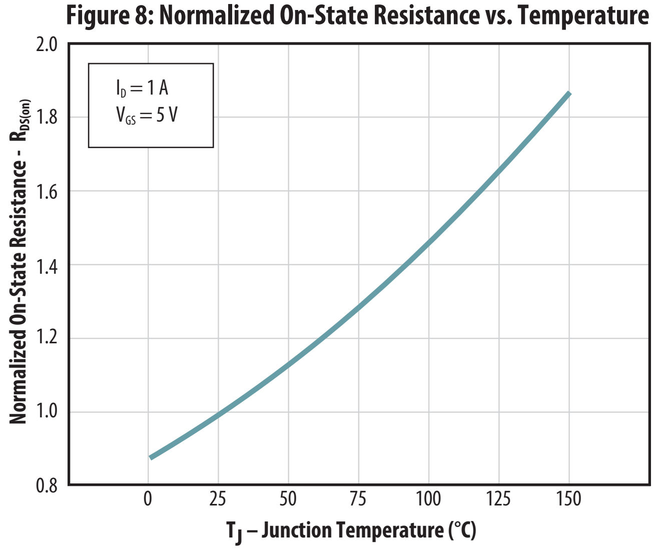


Figure 9: Normalized Threshold Voltage vs. Temperature

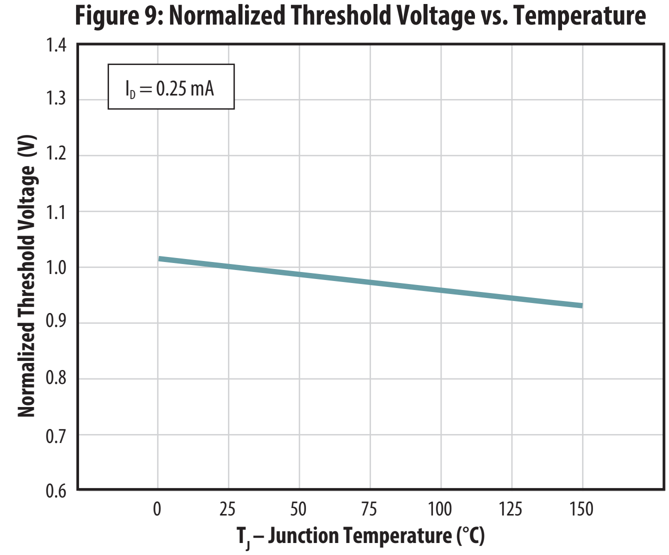
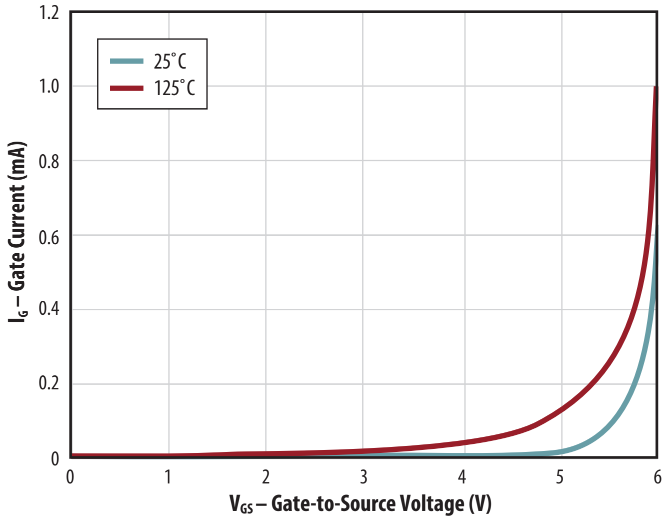


Figure 10: Gate Leakage Current



All measurements were done with substrate shortened to source.

Figure 11: Smith Chart

S-Parameter Characteristics
V_{GSQ} = 1.34 V, V_{DSQ} = 50 V, I_{DQ} = 0.50 A
Pulsed Measurement, Heat-Sink Installed, Z_0 = 50 Ω

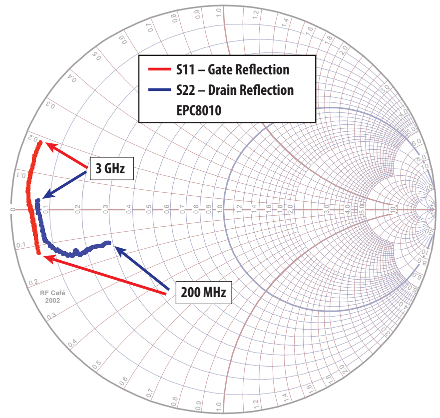
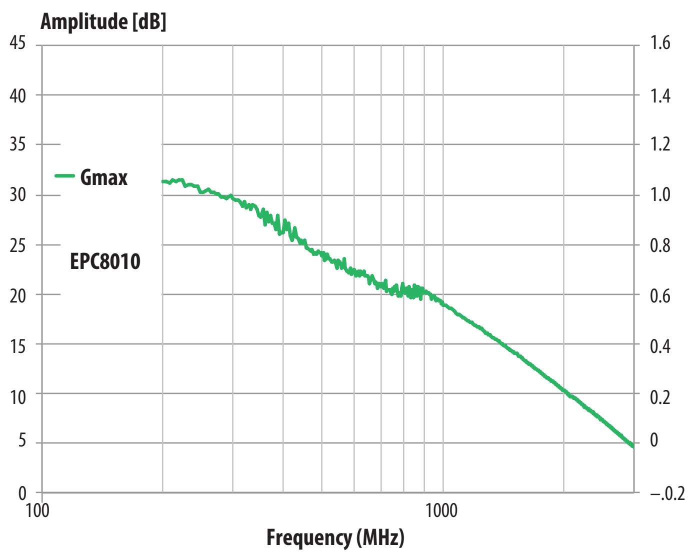


Figure 12: Gain Chart



Frequency	Gate (Z_{GS})	Drain (Z_{DS})
[MHz]	[Ω]	[Ω]
200	2.54 – j11.18	22.54 – j23.91
500	1.57 – j4.20	6.01 – j15.53
1000	0.94 – j0.23	1.85 – j6.89
1200	0.97 + j0.89	1.47 – j4.87
1500	0.97 + j2.38	1.51 – j2.52
2000	1.08 + j4.80	2.09 + j0.41
2400	1.21 + j6.74	2.50 + j2.25
3000	1.62 + j10.34	3.05 + j5.00

S-Parameter Table - Download S-parameter files at ***www.epc-co.com***

Figure 13: Device Reflection

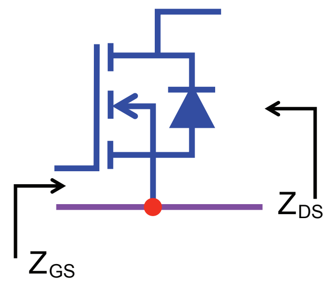


Figure 14: Taper and Reference Plane details – Device Connection

Micro-Strip design: 2-layer
½ oz (17.5 µm) thick copper
30 mil thick RO4350 substrate

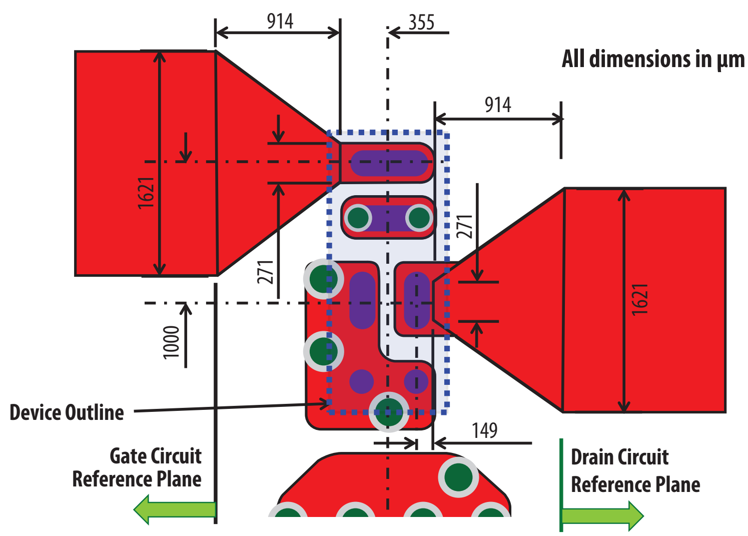
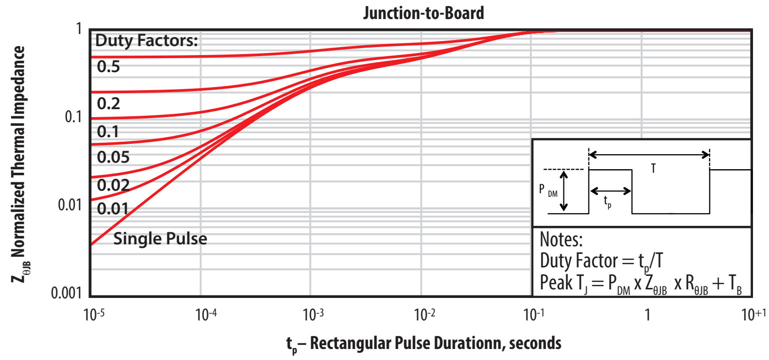


Figure 15: Transient Thermal Response Curves



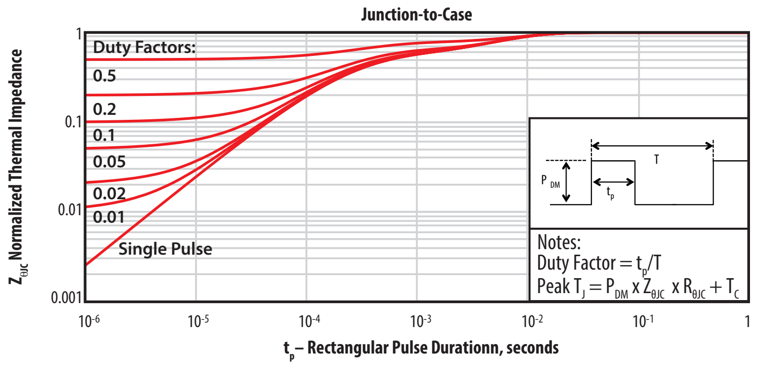
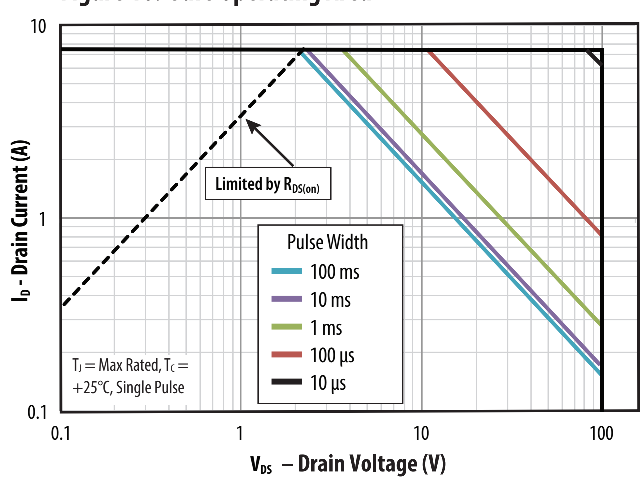
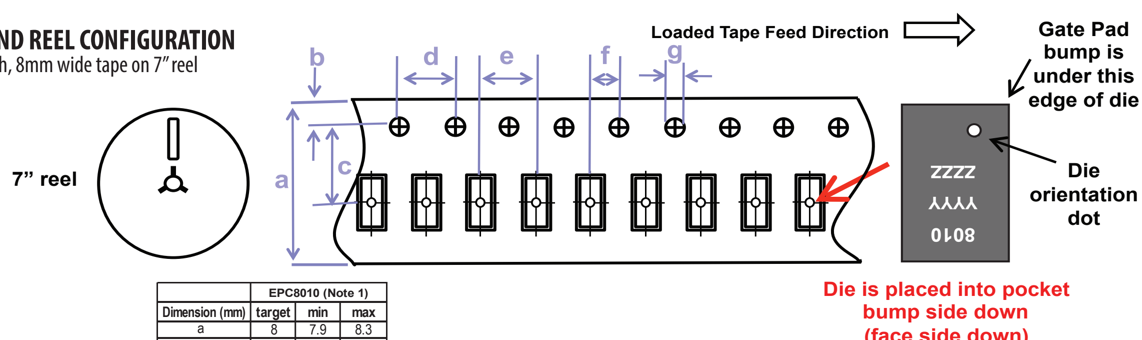


Figure 16: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

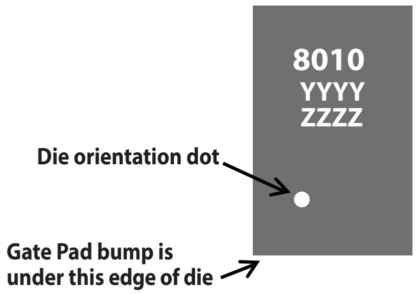


	EPC8010 (Note 1)		
Dimension (mm)	target	min	max
a	8	7.9	8.3
b	1.75	1.65	1.85
c (see note 2)	3.5	3.45	3.55
d	4	3.9	4.1
e	4	3.9	4.1
f (see note 2)	2	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

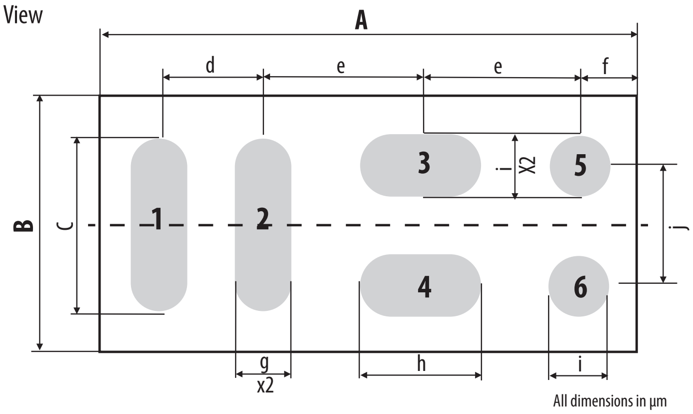
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC8010	8010	YYYY	ZZZZ

DIE OUTLINE

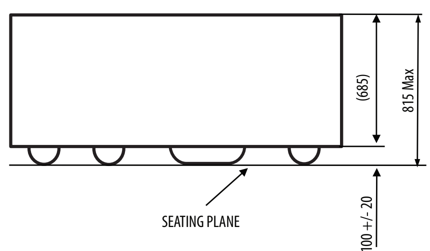
Solder Bar View



Dim	Micrometers		
	Min	Nominal	Max
A	2020	2050	2080
B	820	850	880
C	555	580	605
D	400	400	400
E	600	600	600
F	200	225	250
G	175	200	225
H	425	450	475
I	175	200	225
J	400	400	400

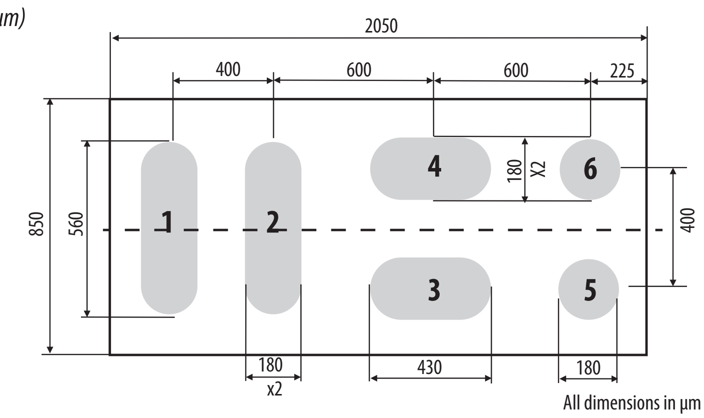
Pad no. 1 is Gate
Pad no. 2 is Source Return for Gate Driver
Pad no. 3 and 5 are Source
Pad no. 4 is Drain
Pad no. 6 is Substrate

Side View



RECOMMENDED LAND PATTERN

(units in µm)



Pad no. 1 is Gate
Pad no. 2 is Source Return for Gate Driver
Pad no. 3 and 5 are Source
Pad no. 4 is Drain
Pad no. 6 is Substrate

The land pattern is solder mask defined.
Solder mask opening is 10 µm smaller per side than bump.

U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398

Information subject to change without notice.
Revised January, 2015