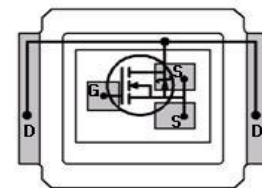


**OptiMOS™3 Power-MOSFET**
**Features**

- Optimized technology for DC/DC converters
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Superior thermal resistance
- Dual sided cooling
- low parasitic inductance
- Low profile (<0.7mm)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Compatible with DirectFET® package MN footprint and outline<sup>2)</sup>

**Product Summary**

$V_{DS}$	60	V
$R_{DS(on),max}$	2.8	mΩ
$I_D$	90	A

**CanPAK™ M  
MG-WDSO-2**


Type	Package	Outline	Marking
BSB028N06NN3 G	MG-WDSO-2	MN	0106

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	90	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	85	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=58\text{ K/W}^{2)}$	22	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	360	
Avalanche energy, single pulse	$E_{AS}$	$I_D=30\text{ A}, R_{GS}=25\text{ Ω}$	590	mJ
Gate source voltage	$V_{GS}$		±20	V

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> DirectFET® is a trademark of International Rectifier Corporation

BSB028N06NN3 G uses DirectFET® technology licensed from International Rectifier Corporation

**Maximum ratings**, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	78	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=58\text{ K/W}^2)$	2.2	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-40 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Thermal characteristics

Thermal resistance, junction - case	$R_{\text{thJC}}$	bottom	-	1.0	-	K/W
		top	-	-	1.6	
Device on PCB	$R_{\text{thJA}}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	58	

**Electrical characteristics**, at  $T_j=25\text{ °C}$ , unless otherwise specified

### Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	60	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=102\text{ }\mu\text{A}$	2	3	4	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=60\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	10	$\mu\text{A}$
		$V_{\text{DS}}=60\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=30\text{ A}$	-	2.2	2.8	m $\Omega$
Gate resistance	$R_{\text{G}}$		-	0.5	-	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=30\text{ A}$	42	83	-	S

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See figure 3 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V},$ $f=1\text{ MHz}$	-	8800	12000	pF
Output capacitance	$C_{oss}$		-	2100	2800	
Reverse transfer capacitance	$C_{rss}$		-	64	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_{G,ext}=1.6\ \Omega$	-	21	-	ns
Rise time	$t_r$		-	9	-	
Turn-off delay time	$t_{d(off)}$		-	38	-	
Fall time	$t_f$		-	6	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=30\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	41	-	nC
Gate to drain charge	$Q_{gd}$		-	8	-	
Switching charge	$Q_{sw}$		-	23	-	
Gate charge total	$Q_g$		-	108	143	
Gate plateau voltage	$V_{plateau}$		-	4.6	-	V
Output charge	$Q_{oss}$	$V_{DD}=30\text{ V}, V_{GS}=0\text{ V}$	-	87	116	

**Reverse Diode**

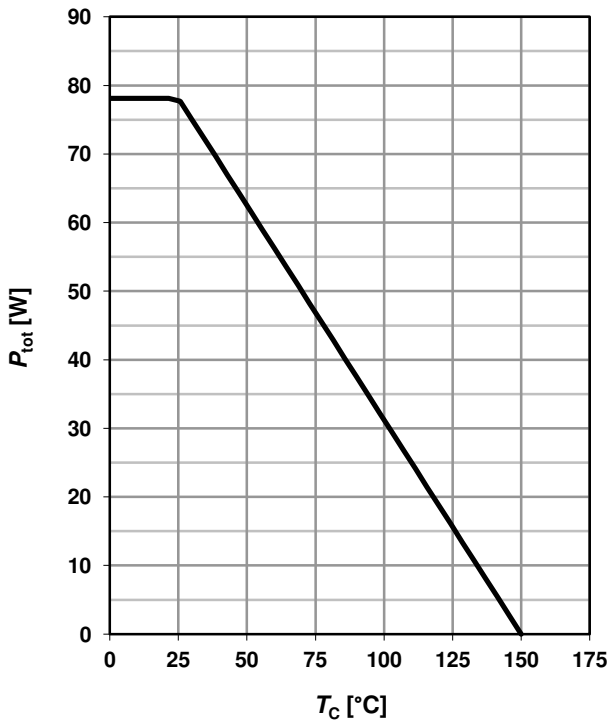
Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	30	A
Diode pulse current	$I_{S,pulse}$		-	-	120	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.8	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=30\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	60	-	ns
Reverse recovery charge	$Q_{rr}$		-	87	-	

<sup>4)</sup> See figure 13 for more detailed information

<sup>5)</sup> See figure 16 for gate charge parameter definition

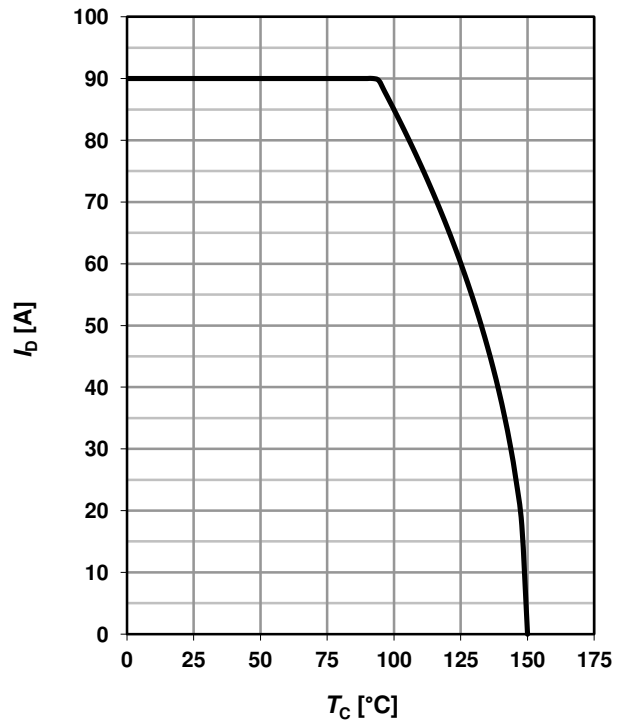
### 1 Power dissipation

$$P_{tot}=f(T_C)$$



### 2 Drain current

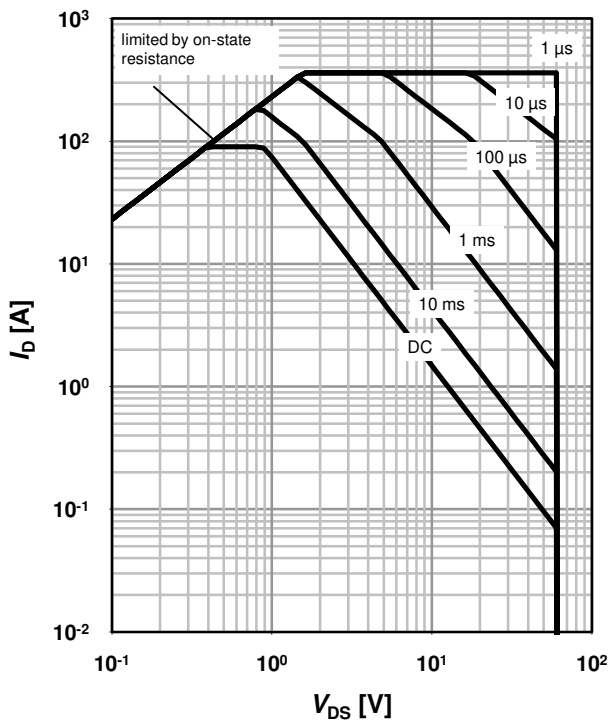
$$I_D=f(T_C); V_{GS} \geq 10 \text{ V}$$



### 3 Safe operating area

$$I_D=f(V_{DS}); T_C=25 \text{ °C}; D=0$$

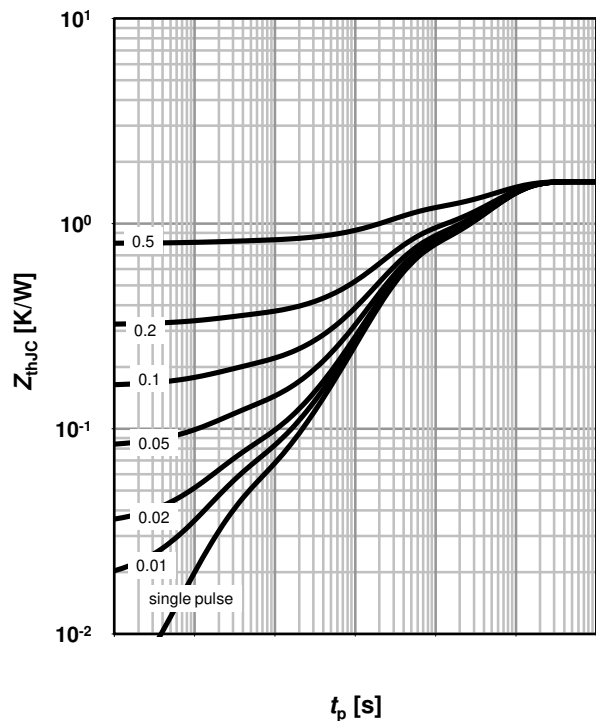
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$

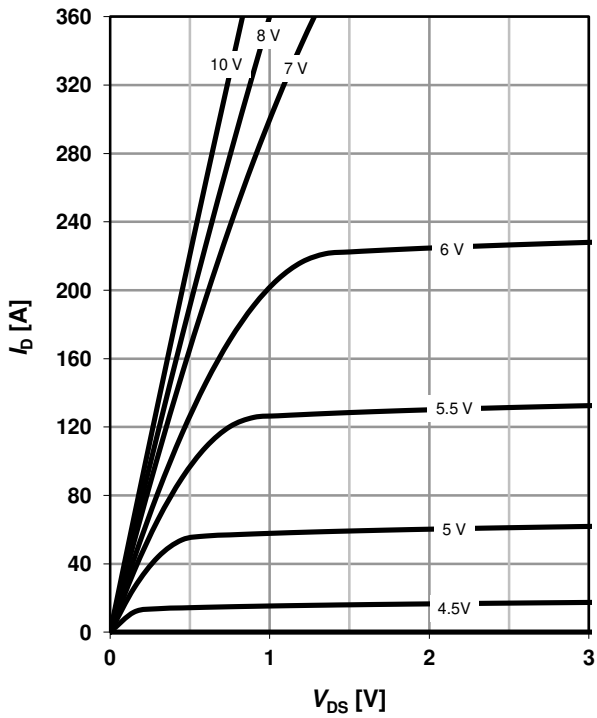
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

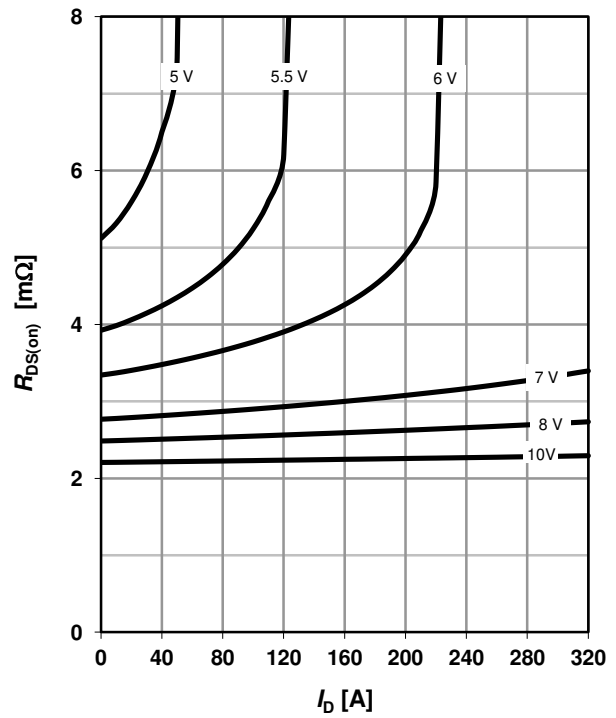
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

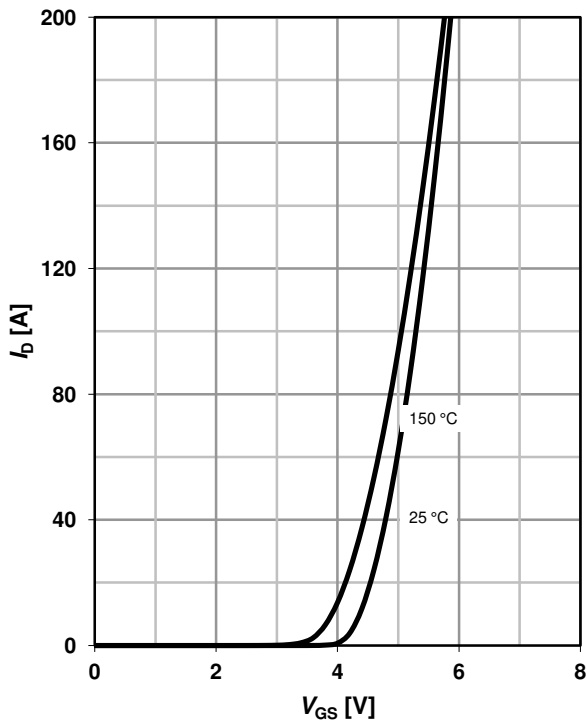
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

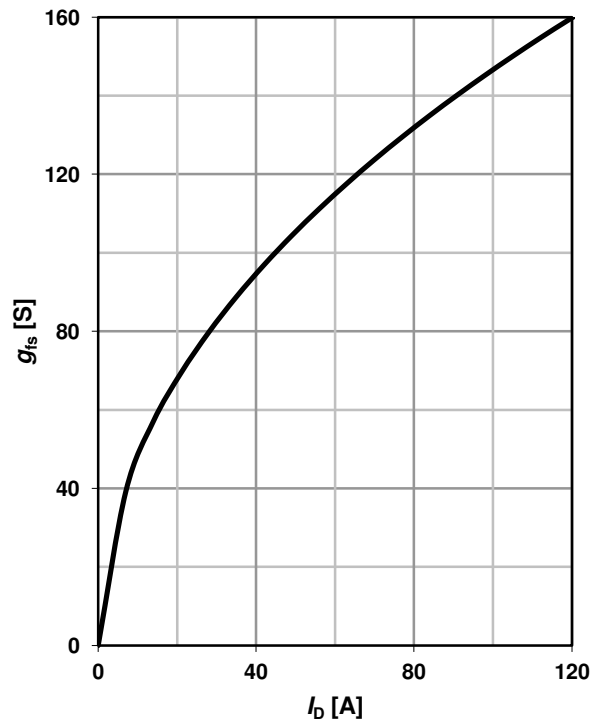
$I_D=f(V_{GS}); |V_{DS}|>2I_D R_{DS(on)max}$

parameter:  $T_j$



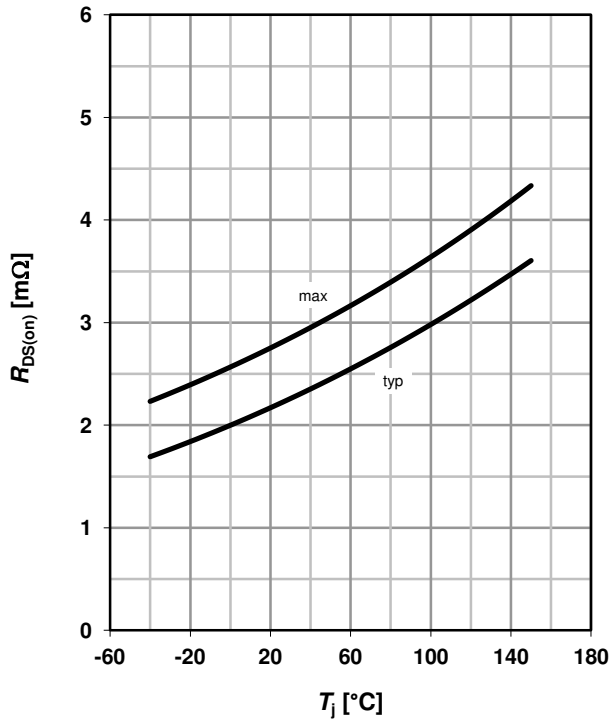
**8 Typ. forward transconductance**

$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$



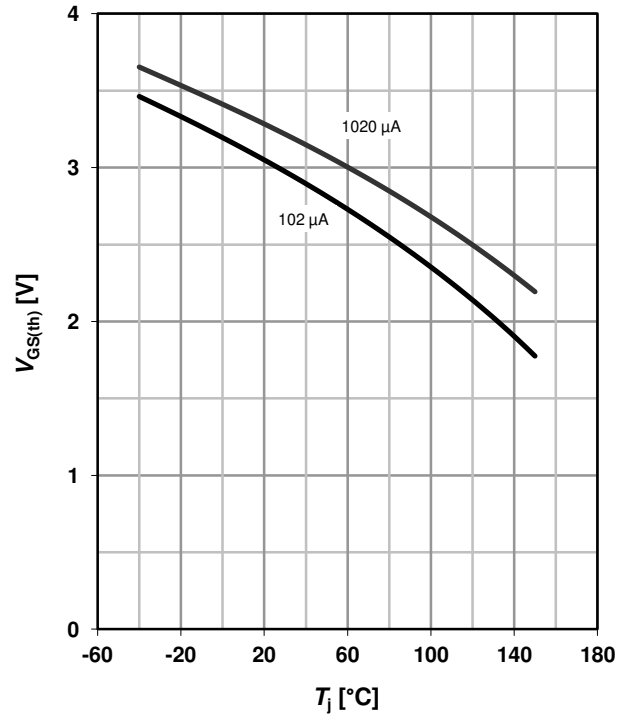
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=30\text{ A}; V_{GS}=10\text{ V}$



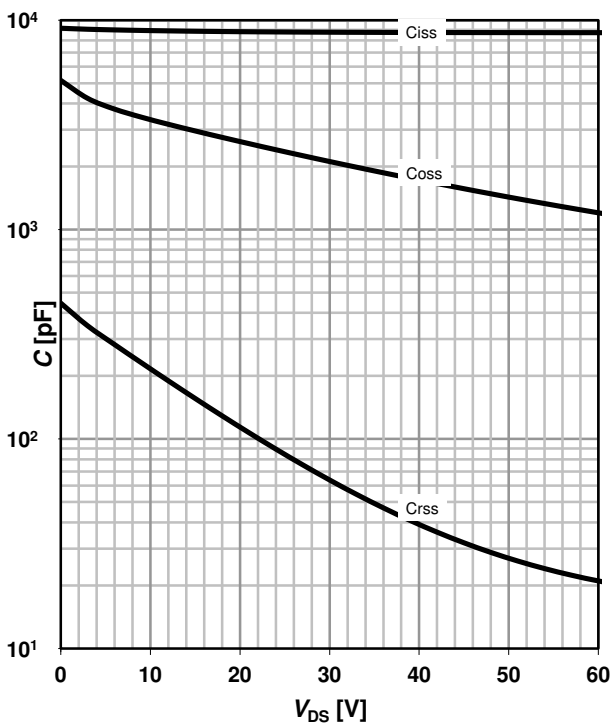
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$



**11 Typ. capacitances**

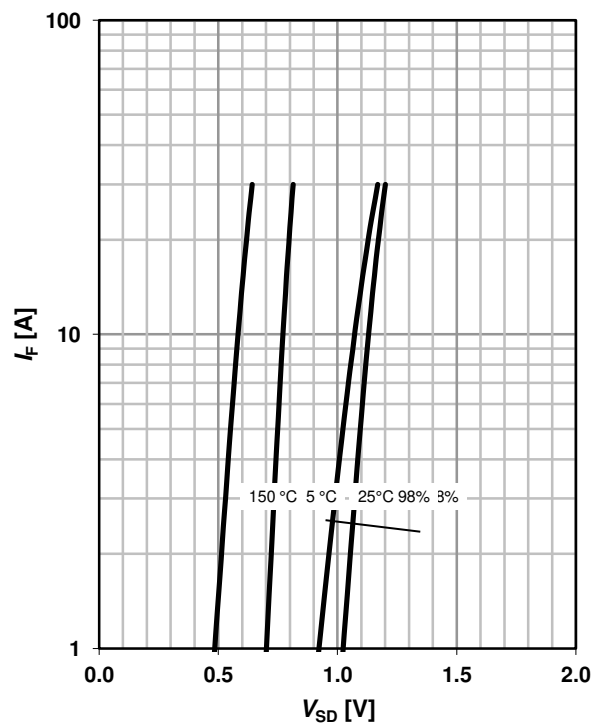
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

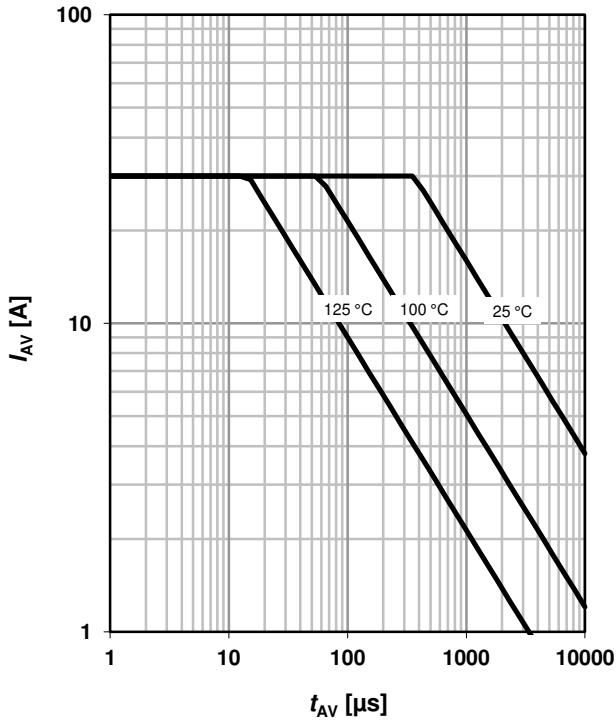
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

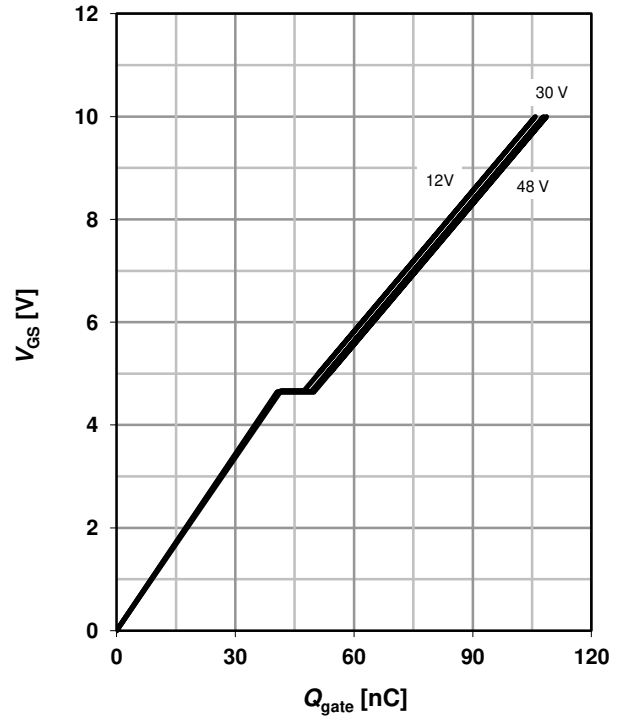
parameter:  $T_{j(\text{start})}$



**14 Typ. gate charge**

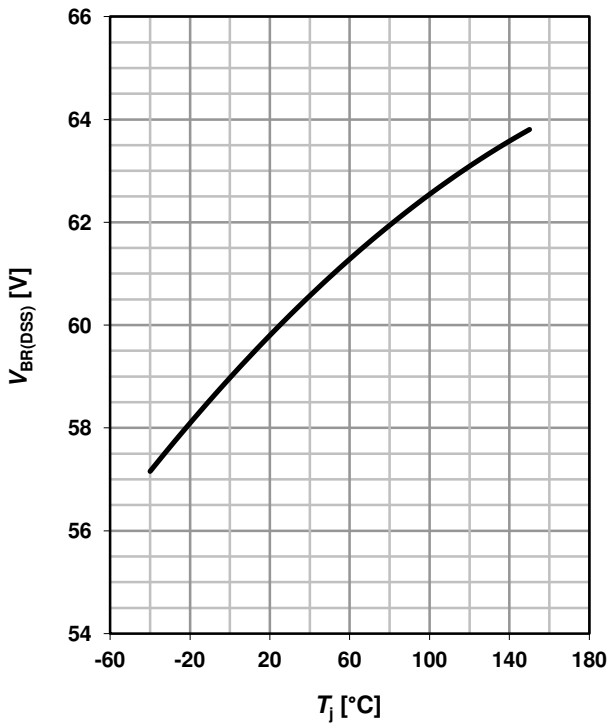
$V_{GS}=f(Q_{\text{gate}}); I_D=30 \text{ A pulsed}$

parameter:  $V_{DD}$

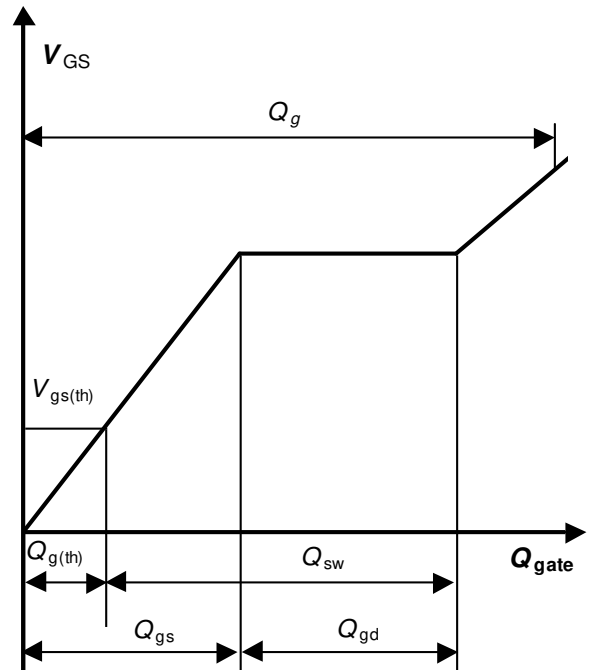


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

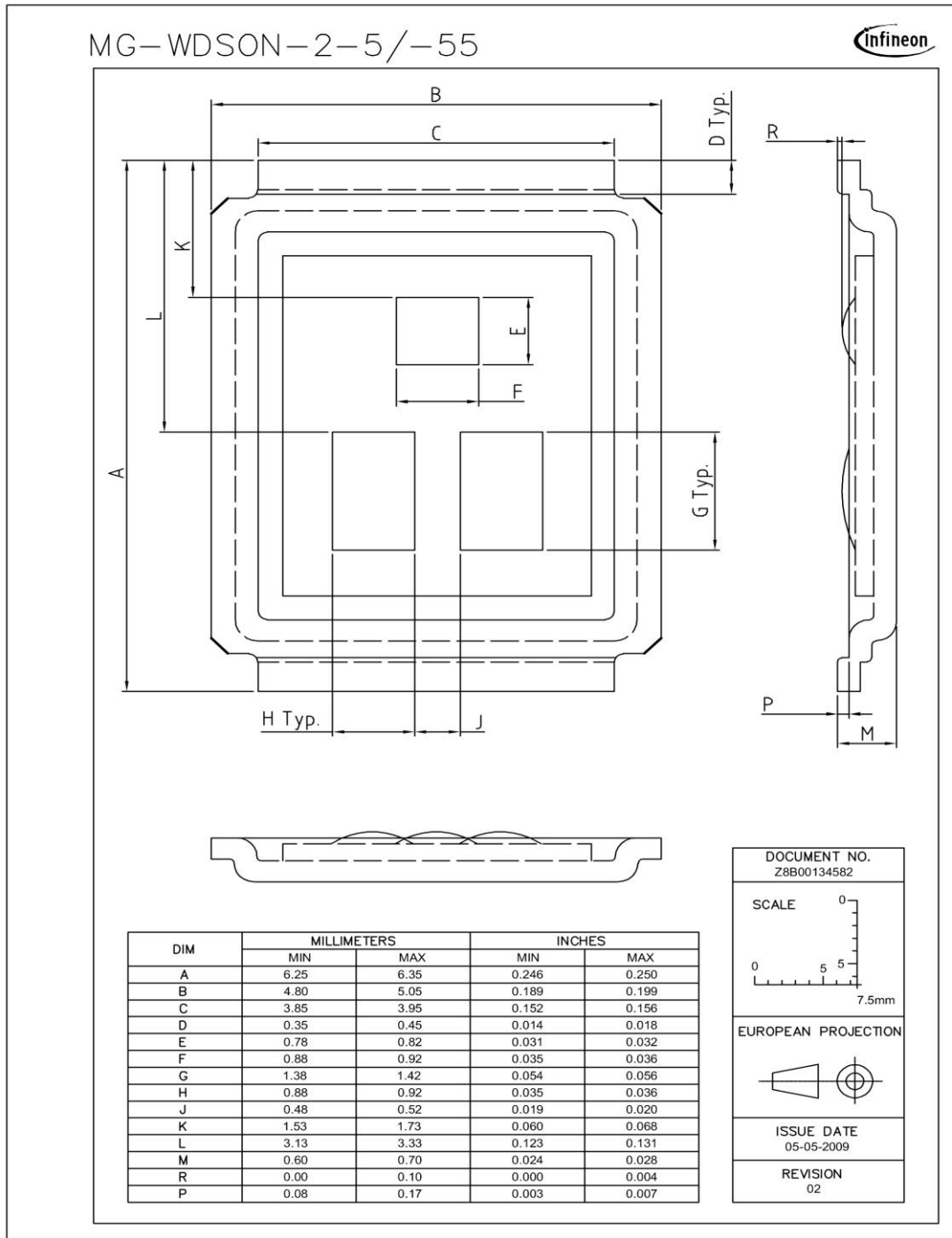


**16 Gate charge waveforms**



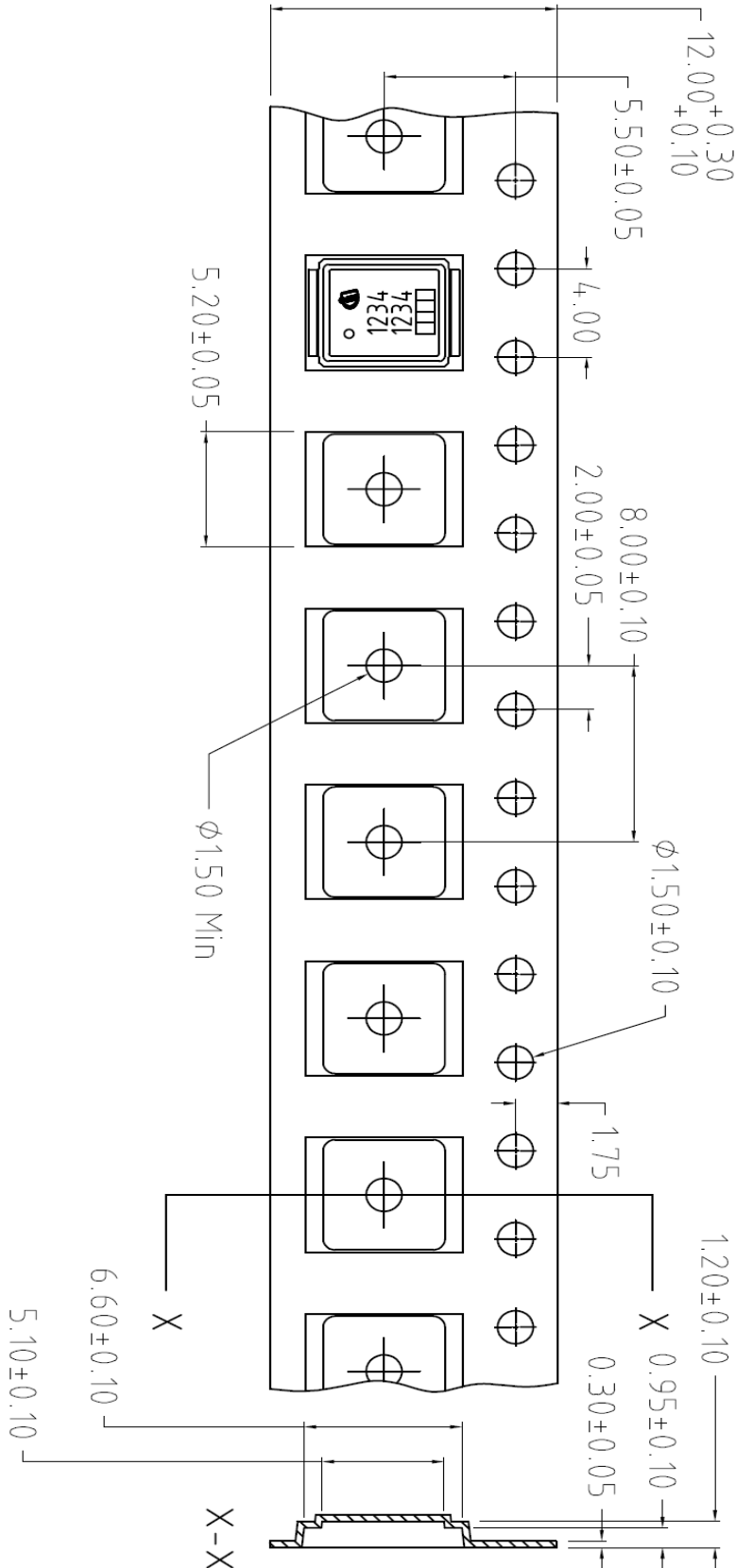
Package Outline

CanPAK™ M  
MG-WDSO-2

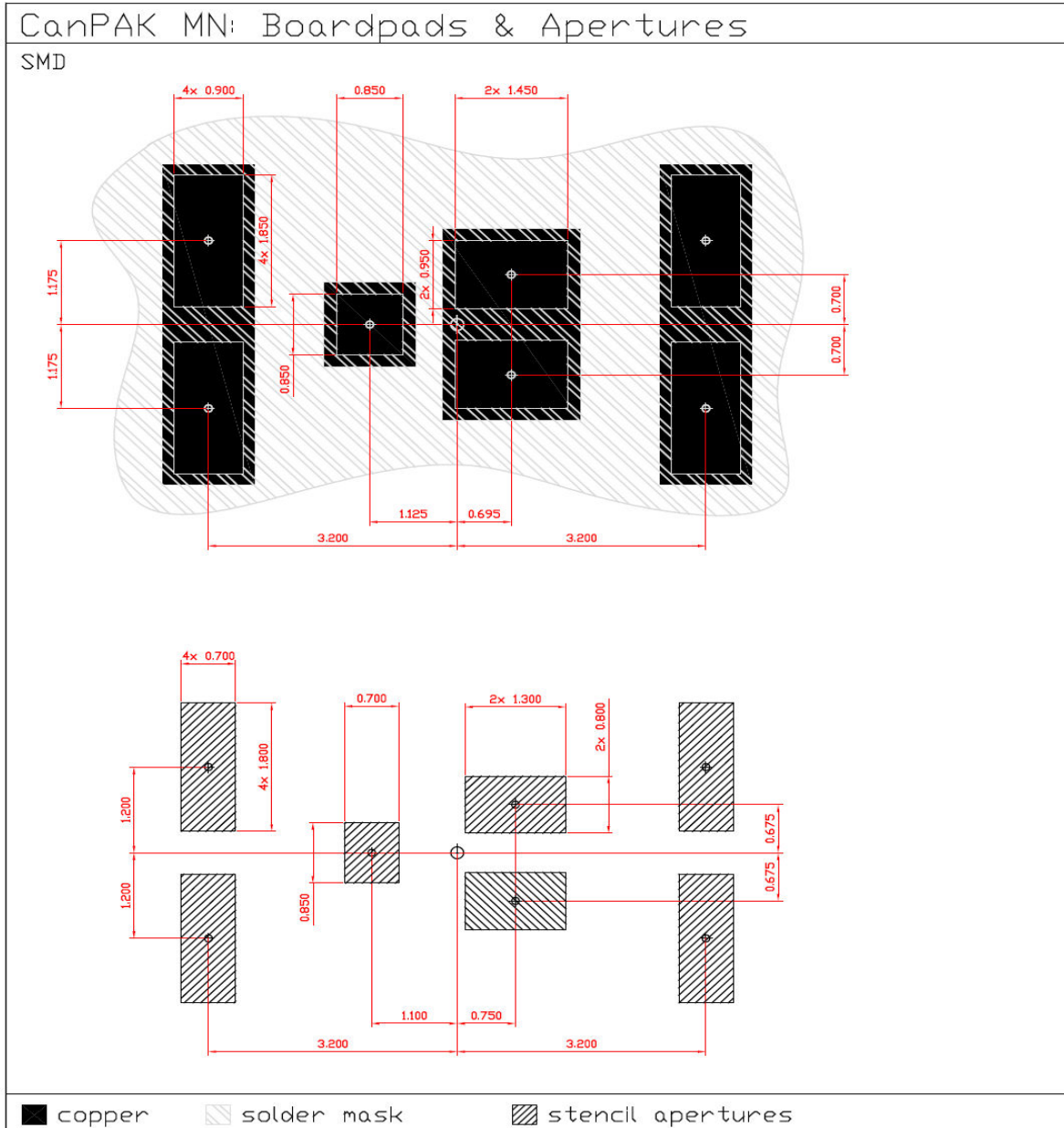




CanPAK™ M  
MG-WDSO-2



**CanPAK™ M**  
**MG-WDSO-2**



Dimensions in mm

Raccomended stencil thikness 150 µm

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