

**CoolMOS™ Power Transistor**
**Features**

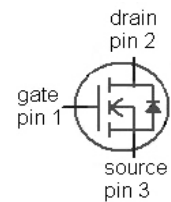
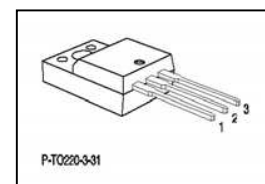
- Lowest figure of merit  $R_{ON} \times Q_g$
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Pb-free lead plating; RoHS compliant; Halogen free for mold compound
- Qualified for industrial grade applications according to JEDEC<sup>0)</sup>

**Product Summary**

$V_{DS} @ T_{jmax}$	550	V
$R_{DS(on),max}$	0.350	$\Omega$
$Q_{g,typ}$	19	nC

**CoolMOS CP is designed for:**

- Hard and softswitching SMPS topologies
- CCM PFC for Notebook adapter, PDP and LCD TV
- PWM for Notebook adapter, PDP and LCD TV

**TO220 Full PAK**


Type	Package	Marking
IPA50R350CP	PG-TO220FP	5R350P

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>1)</sup>	$I_D$	$T_C=25\text{ °C}$	10	A
		$T_C=100\text{ °C}$	6	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	22	
Avalanche energy, single pulse	$E_{AS}$	$I_D=3.7\text{ A}$ , $V_{DD}=50\text{ V}$	246	mJ
Avalanche energy, repetitive $t_{AR}^{2),3)}$	$E_{AR}$	$I_D=3.7\text{ A}$ , $V_{DD}=50\text{ V}$	0.37	
Avalanche current, repetitive $t_{AR}^{2),3)}$	$I_{AR}$		3.7	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=0\dots400\text{ V}$	50	V/ns
Gate source voltage	$V_{GS}$	static	$\pm 20$	V
		AC ( $f>1\text{ Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	32	W
Operating and storage temperature	$T_j$ , $T_{stg}$		-55 ... 150	$^{\circ}\text{C}$
Mounting torque		M2.5 screws	60	Ncm

**Maximum ratings**, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current <sup>1)</sup>	$I_S$	$T_C=25\text{ °C}$	5.6	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		22	
Reverse diode $dv/dt$ <sup>4)</sup>	$dv/dt$		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{thJC}$		-	-	3.9	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	leaded	-	-	62	
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C

**Electrical characteristics**, at  $T_j=25\text{ °C}$ , unless otherwise specified

**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=0.37\text{ mA}$	2.5	3	3.5	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=500\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-	1	$\mu\text{A}$
		$V_{DS}=500\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ °C}$	-	10	-	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=5.6\text{ A}, T_j=25\text{ °C}$	-	0.32	0.35	$\Omega$
		$V_{GS}=10\text{ V}, I_D=5.6\text{ A}, T_j=150\text{ °C}$	-	0.80	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	2.2	-	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=100\text{ V},$ $f=1\text{ MHz}$	-	1020	-	pF
Output capacitance	$C_{oss}$		-	46	-	
Effective output capacitance, energy related <sup>5)</sup>	$C_{o(er)}$	$V_{GS}=0\text{ V}, V_{DS}=0\text{ V}$ to 400 V	-	43	-	
Effective output capacitance, time related <sup>6)</sup>	$C_{o(tr)}$		-	92	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=400\text{ V},$ $V_{GS}=10\text{ V}, I_D=5.6\text{ A},$ $R_G=30.9\ \Omega$	-	35	-	ns
Rise time	$t_r$		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	80	-	
Fall time	$t_f$		-	12.0	-	

**Gate Charge Characteristics**

Gate to source charge	$Q_{gs}$	$V_{DD}=400\text{ V}, I_D=5.6\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	4	-	nC
Gate to drain charge	$Q_{gd}$		-	6	-	
Gate charge total	$Q_g$		-	19	25	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V

**Reverse Diode**

Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=5.6\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=400\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	250	-	ns
Reverse recovery charge	$Q_{rr}$		-	2.3	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rrm}$		-	19	-	A

<sup>0)</sup> J-STD20 and JESD22

<sup>1)</sup> Limited only by  $T_{j,max}$ 
<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$ 
<sup>3)</sup> Repetitive avalanche causes additional power losses that can be calculated as  $P_{AV}=E_{AR} \cdot f$ .

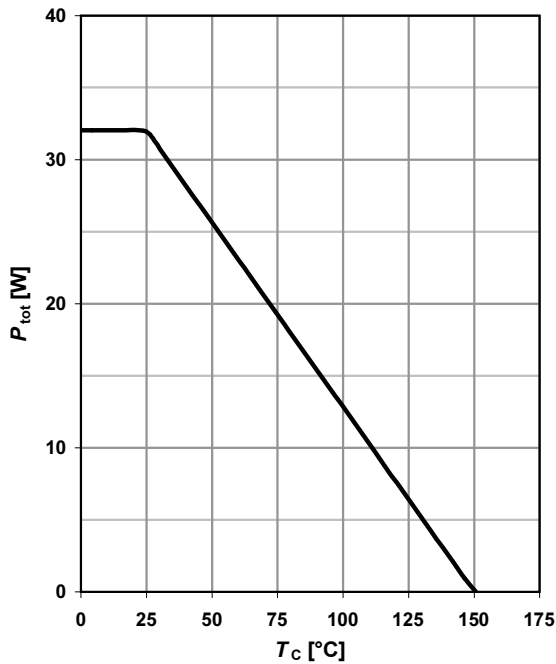
<sup>4)</sup>  $I_{SD} \leq I_D, di/dt \leq 400\text{ A}/\mu\text{s}, V_{DClink}=400\text{ V}, V_{peak} < V_{(BR)DSS}, T_j < T_{j,max}$ , identical low and high side switch

<sup>5)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

<sup>6)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**1 Power dissipation**

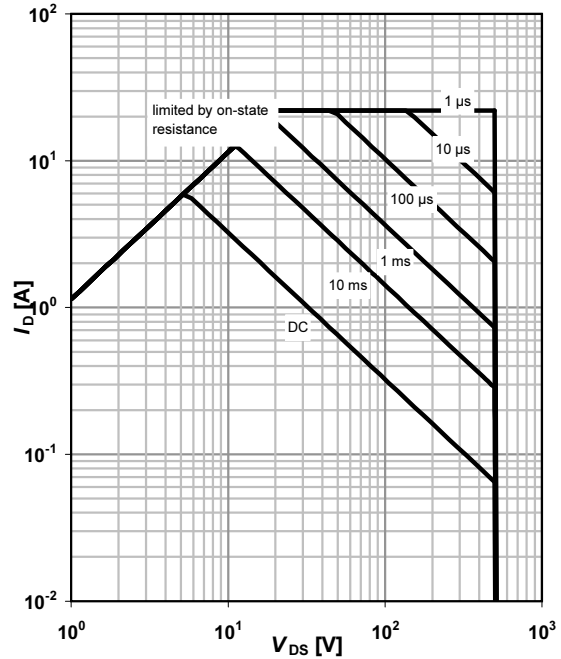
$P_{tot}=f(T_c)$



**2 Safe operating area**

$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0$

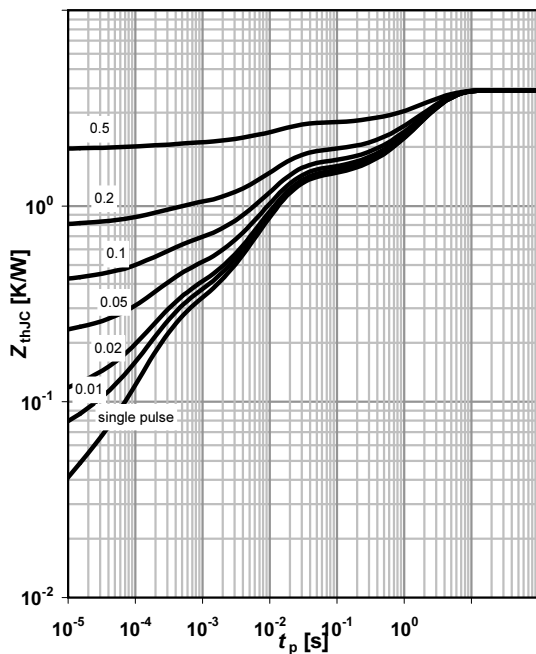
parameter:  $t_p$



**3 Max. transient thermal impedance**

$Z_{(th)JC}=f(t_p)$

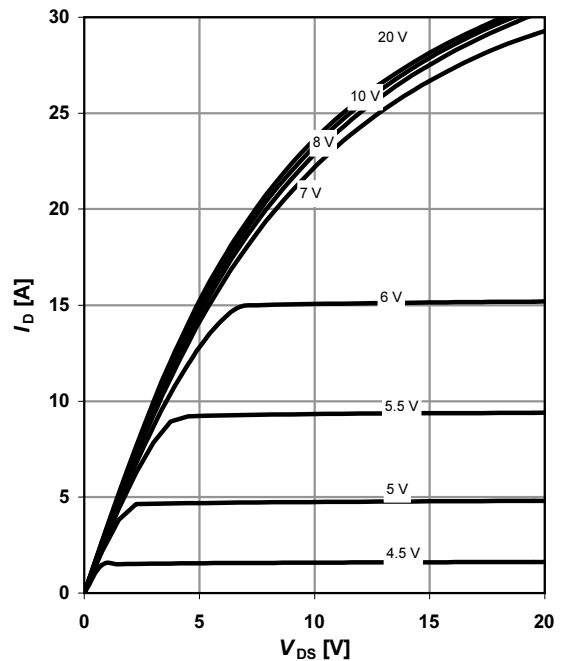
parameter:  $D=t_p/T$



**4 Typ. output characteristics**

$I_D=f(V_{DS}); T_j=25\text{ °C}$

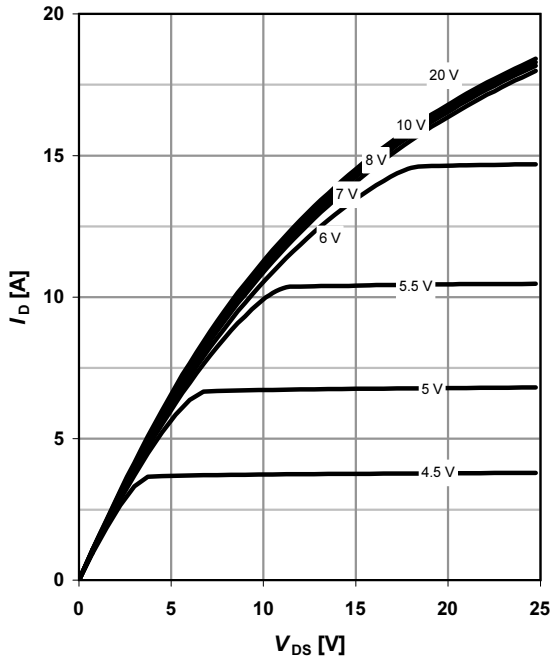
parameter:  $V_{GS}$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 150\text{ }^\circ\text{C}$

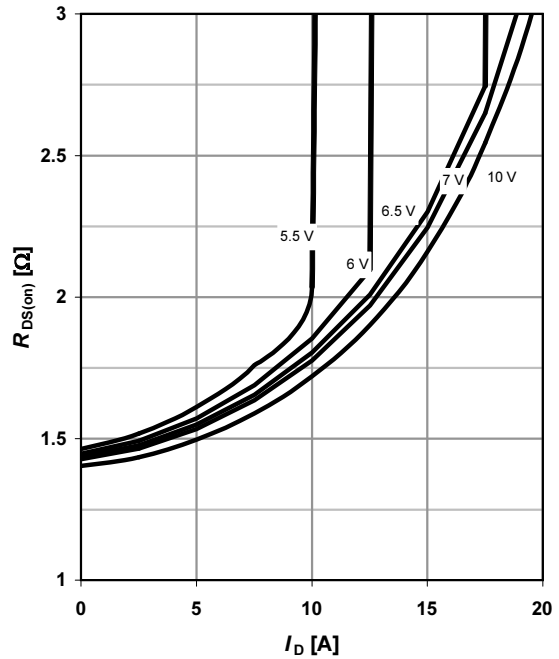
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

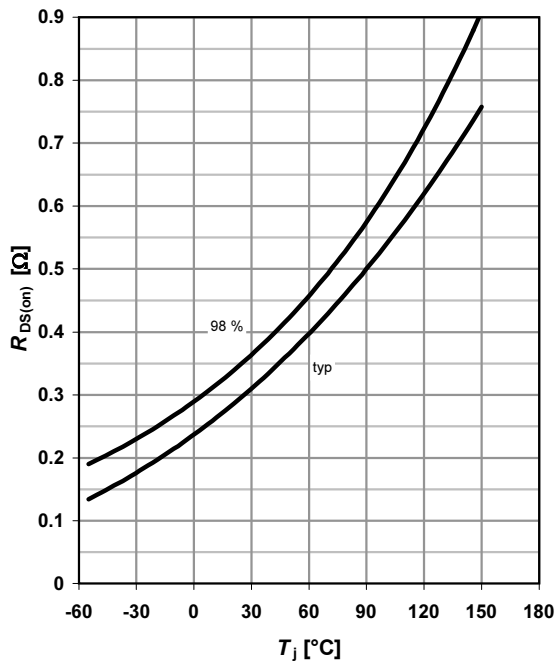
$R_{DS(on)} = f(I_D); T_j = 150\text{ }^\circ\text{C}$

parameter:  $V_{GS}$



**7 Drain-source on-state resistance**

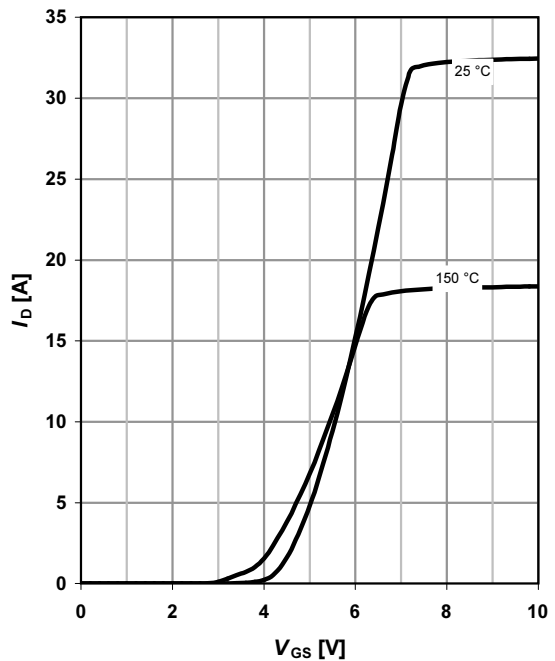
$R_{DS(on)} = f(T_j); I_D = 5.6\text{ A}; V_{GS} = 10\text{ V}$



**8 Typ. transfer characteristics**

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

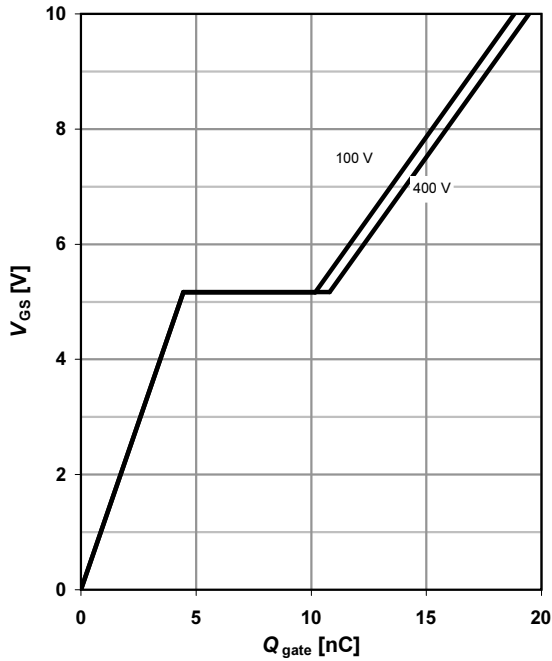
parameter:  $T_j$



**9 Typ. gate charge**

$V_{GS}=f(Q_{gate}); I_D=5.6$  A pulsed

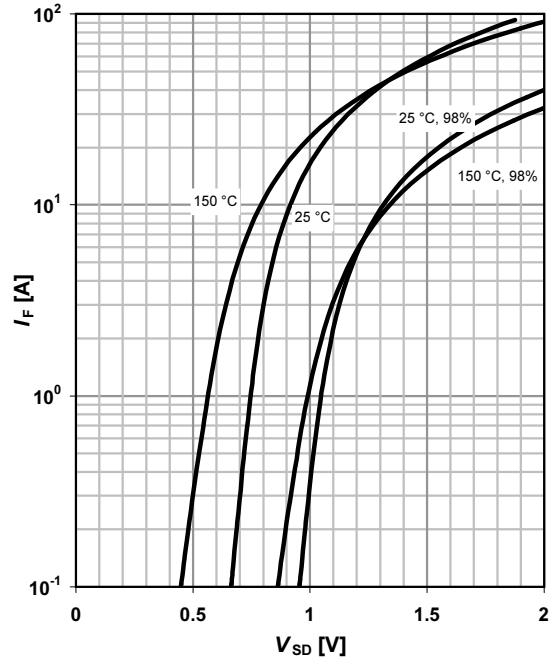
parameter:  $V_{DD}$



**10 Forward characteristics of reverse diode**

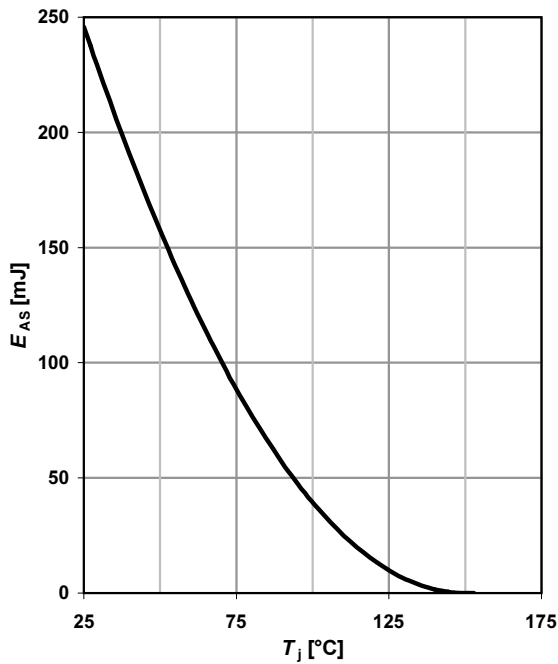
$I_F=f(V_{SD})$

parameter:  $T_j$



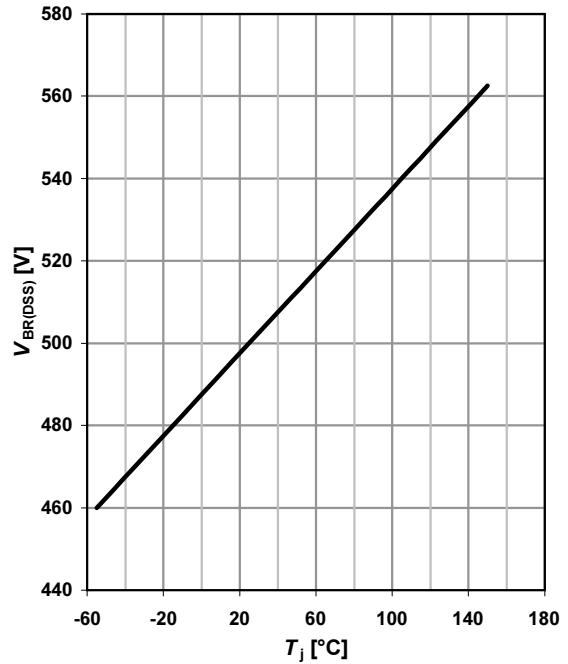
**11 Avalanche energy**

$E_{AS}=f(T_j); I_D=3.7$  A;  $V_{DD}=50$  V



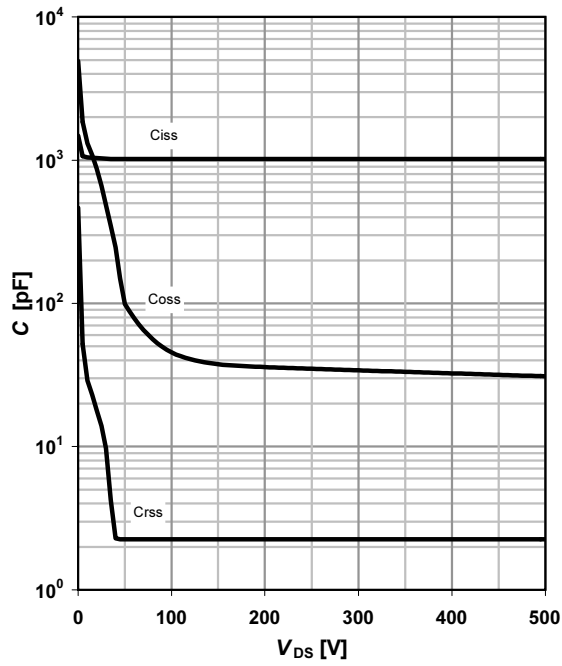
**12 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=0.25$  mA



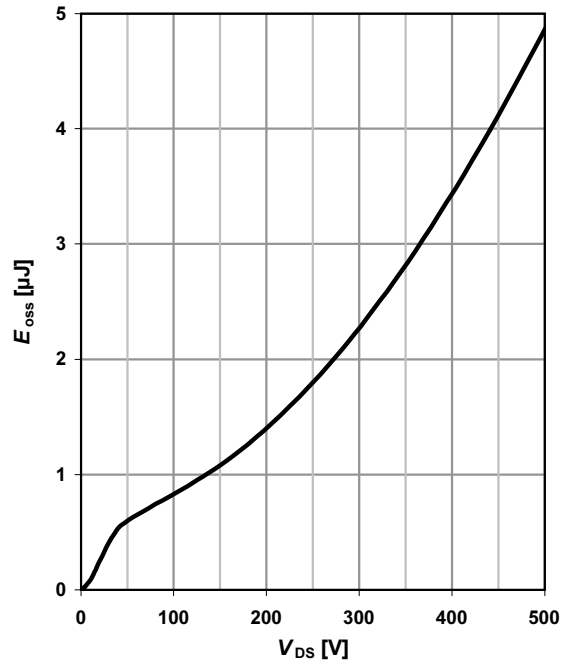
**13 Typ. capacitances**

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

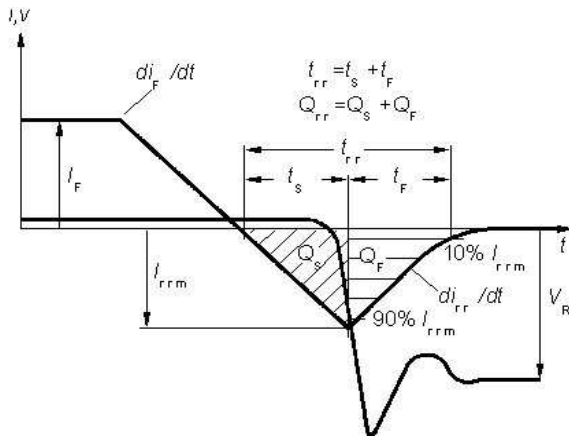


**14 Typ. Coss stored energy**

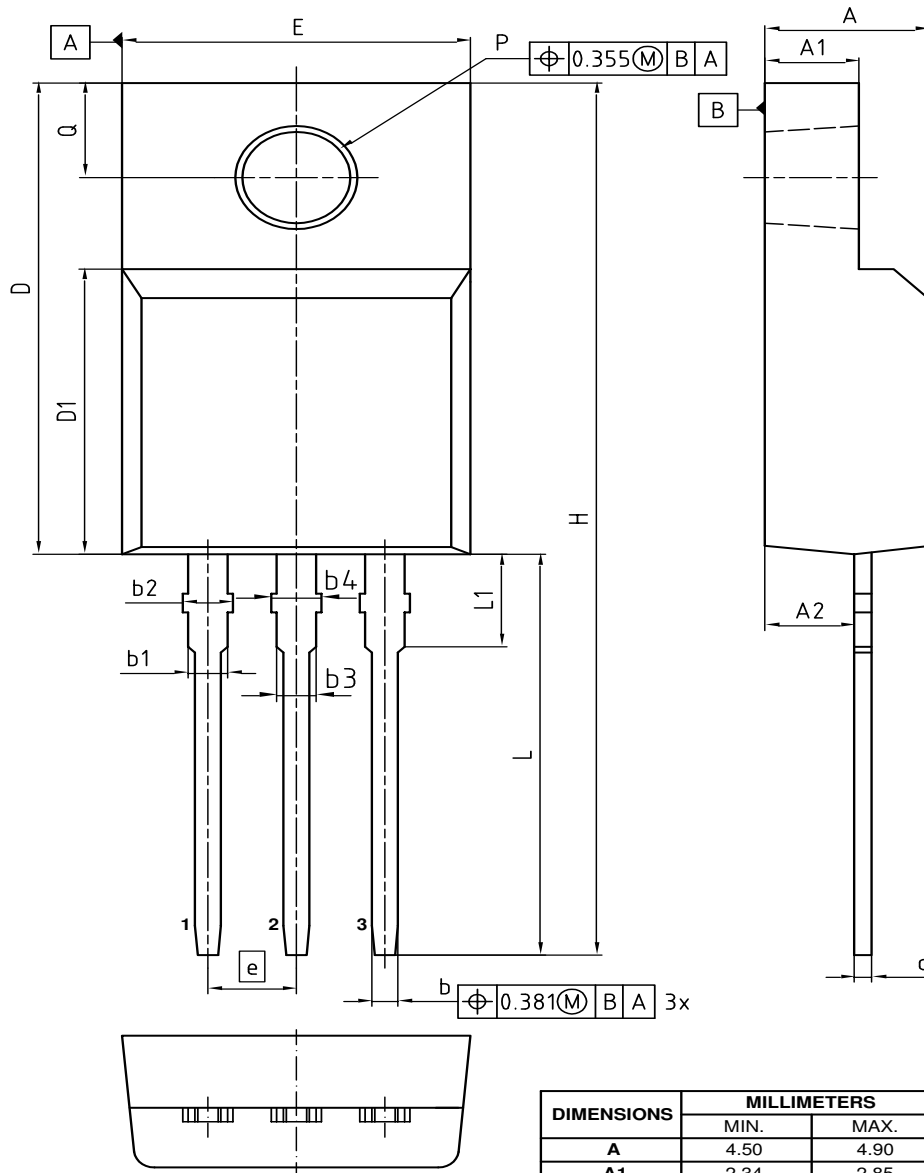
$$E_{oss} = f(V_{DS})$$



Definition of diode switching characteristics





**Outline PG-TO220 FullPAK**


NOTES:  
 ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281  
 AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS  
 OR GATE BURRS  
 GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
<b>A</b>	4.50	4.90
<b>A1</b>	2.34	2.85
<b>A2</b>	2.42	2.86
<b>b</b>	0.65	0.90
<b>b1</b>	0.95	1.38
<b>b2</b>	0.95	1.51
<b>b3</b>	0.65	1.38
<b>b4</b>	0.65	1.51
<b>c</b>	0.40	0.63
<b>D</b>	15.67	16.15
<b>D1</b>	8.97	9.83
<b>E</b>	10.00	10.65
<b>e</b>	2.54	
<b>H</b>	28.70	29.75
<b>L</b>	12.78	13.75
<b>L1</b>	2.83	3.45
<b>øP</b>	3.00	3.30
<b>Q</b>	3.15	3.50

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# 500V CoolMOS™ CP Power Transistor

## IPA50R350CP

### Revision History

IPA50R350CP

**Revision: 2018-02-26, Rev. 2.2**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.2	2018-02-26	Outline PG-TO220 FullPAK update

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