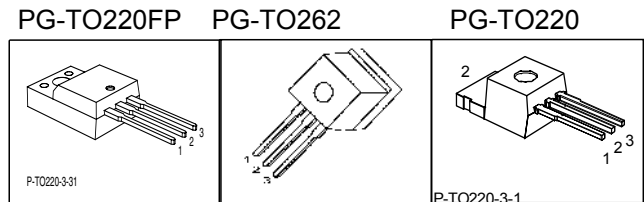


Cool MOS™ Power Transistor

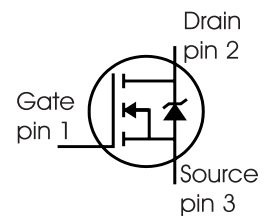
Feature

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability
- Improved transconductance
- PG-TO-220-3-31;-3-111: Fully isolated package (2500 VAC; 1 minute)
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC⁰⁾ for target applications

$V_{DS} @ T_{jmax}$	650	V
$R_{DS(on)}$	0.6	Ω
I_D	7.3	A



Type	Package	Ordering Code	Marking
SPP07N60C3	PG-TO220-3	Q67040-S4400	07N60C3
SPI07N60C3	PG-TO262	Q67040-S4424	07N60C3
SPA07N60C3	PG-TO220FP	SP000216303	07N60C3



Maximum Ratings

Parameter	Symbol	Value		Unit
		SPP_I	SPA	
Continuous drain current $T_C = 25\text{ }^\circ\text{C}$ $T_C = 100\text{ }^\circ\text{C}$	I_D	7.3 4.6	7.3 ¹⁾ 4.6 ¹⁾	A
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\text{ puls}}$	21.9	21.9	A
Avalanche energy, single pulse $I_D=5.5\text{A}, V_{DD}=50\text{V}$	E_{AS}	230	230	mJ
Avalanche energy, repetitive t_{AR} limited by T_{jmax} ²⁾ $I_D=7.3\text{A}, V_{DD}=50\text{V}$	E_{AR}	0.5	0.5	
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	7.3	7.3	A
Gate source voltage static	V_{GS}	± 20	± 20	V
Gate source voltage AC ($f > 1\text{Hz}$)	V_{GS}	± 30	± 30	
Power dissipation, $T_C = 25\text{ }^\circ\text{C}$	P_{tot}	83	32	W
Operating and storage temperature	T_j, T_{stg}	-55...+150		$^\circ\text{C}$
Reverse diode dv/dt ⁶⁾	dv/dt	15		V/ns

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope $V_{DS} = 480\text{ V}$, $I_D = 7.3\text{ A}$, $T_j = 125\text{ °C}$	dv/dt	50	V/ns

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	K/W
Thermal resistance, junction - case, FullPAK	$R_{thJC\text{ FP}}$	-	-	3.9	
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
Thermal resistance, junction - ambient, FullPAK	$R_{thJA\text{ FP}}$	-	-	80	
SMD version, device on PCB: @ min. footprint @ 6 cm ² cooling area ³⁾	R_{thJA}	-	-	62	
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s	T_{sold}	-	-	260	°C

Electrical Characteristics, at $T_j=25\text{ °C}$ unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}$, $I_D=0.25\text{mA}$	600	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	$V_{GS}=0\text{V}$, $I_D=7.3\text{A}$	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	$I_D=350\mu\text{A}$, $V_{GS}=V_{DS}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$, $T_j=25\text{ °C}$ $T_j=150\text{ °C}$	-	0.5	1	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=30\text{V}$, $V_{DS}=0\text{V}$	-	-	100	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=4.6\text{A}$ $T_j=25\text{ °C}$ $T_j=150\text{ °C}$	-	0.54	0.6	Ω
Gate input resistance	R_G	$f=1\text{MHz}$, open drain	-	0.8	-	

Electrical Characteristics, at $T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Characteristics						
Transconductance	g_{fs}	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 4.6\text{A}$	-	6	-	S
Input capacitance	C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$	-	790	-	pF
Output capacitance	C_{oss}		-	260	-	
Reverse transfer capacitance	C_{rss}		-	16	-	
Effective output capacitance, ⁴⁾ energy related	$C_{o(er)}$	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 480\text{V}$	-	30	-	
Effective output capacitance, ⁵⁾ time related	$C_{o(tr)}$		-	55	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 380\text{V}$, $V_{GS} = 0/13\text{V}$, $I_D = 7.3\text{A}$, $R_G = 12\Omega$, $T_j = 125\text{ }^\circ\text{C}$	-	6	-	ns
Rise time	t_r		-	3.5	-	
Turn-off delay time	$t_{d(off)}$		-	60	100	
Fall time	t_f		-	7	15	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD} = 480\text{V}$, $I_D = 7.3\text{A}$	-	3	-	nC
Gate to drain charge	Q_{gd}		-	9.2	-	
Gate charge total	Q_g	$V_{DD} = 480\text{V}$, $I_D = 7.3\text{A}$, $V_{GS} = 0\text{ to } 10\text{V}$	-	21	27	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 480\text{V}$, $I_D = 7.3\text{A}$	-	5.5	-	V

⁰J-STD20 and JESD22

¹Limited only by maximum temperature

²Repetitive avalanche causes additional power losses that can be calculated as $P_{AV} = E_{AR} \cdot f$.

³Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

⁴ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

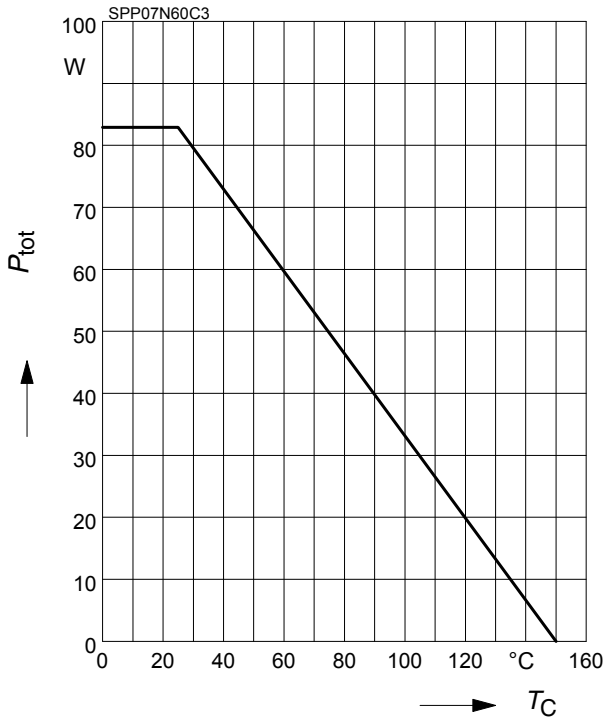
⁵ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁶ $I_{SD} \leq I_D$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DClink} = 400\text{V}$, $V_{peak} < V_{BR, DSS}$, $T_j < T_{j,max}$.

Identical low-side and high-side switch.

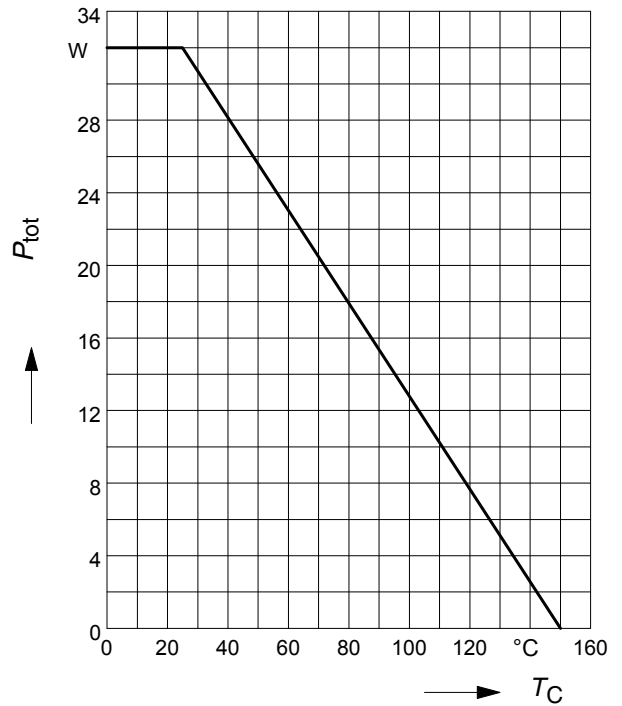
1 Power dissipation

$$P_{tot} = f(T_C)$$



2 Power dissipation FullPAK

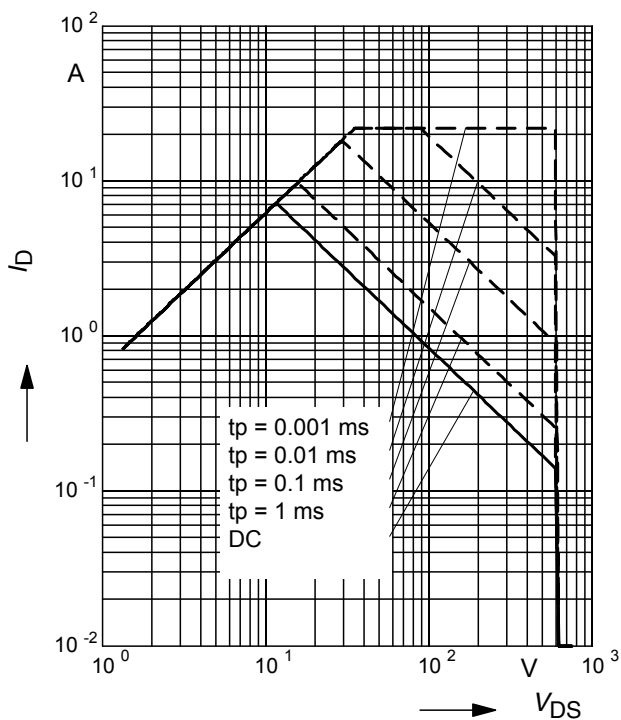
$$P_{tot} = f(T_C)$$



3 Safe operating area

$$I_D = f(V_{DS})$$

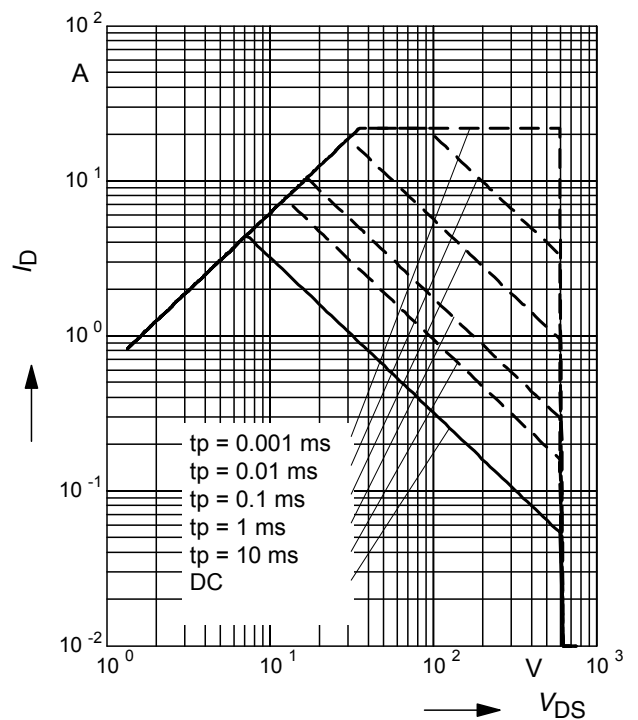
parameter : $D = 0$, $T_C = 25^\circ\text{C}$



4 Safe operating area FullPAK

$$I_D = f(V_{DS})$$

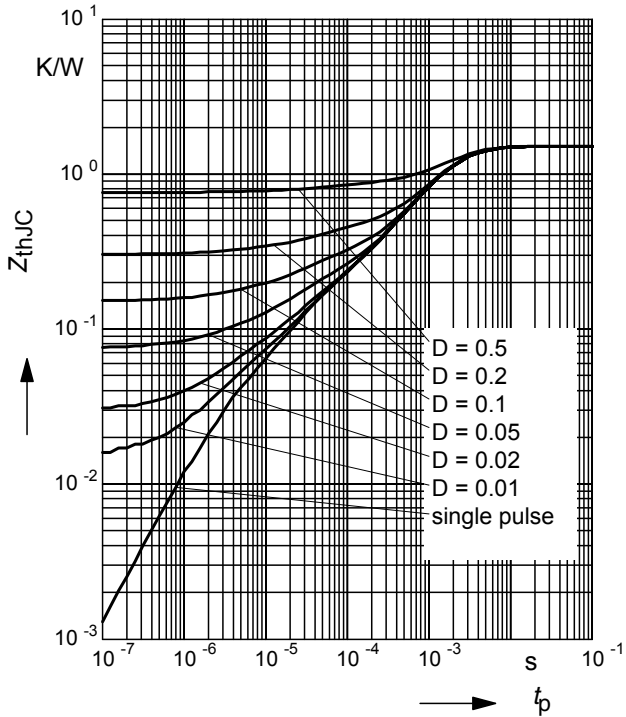
parameter: $D = 0$, $T_C = 25^\circ\text{C}$



5 Transient thermal impedance

$$Z_{thJC} = f(t_p)$$

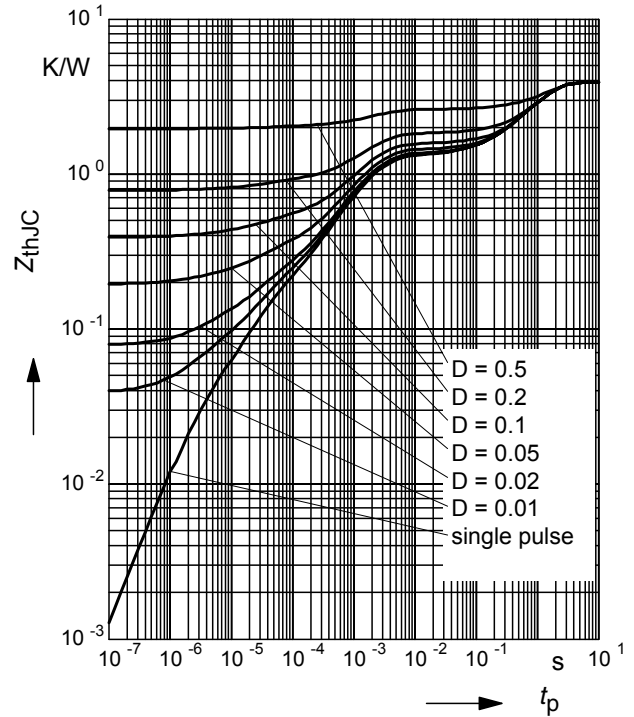
parameter: $D = t_p/T$



6 Transient thermal impedance FullPAK

$$Z_{thJC} = f(t_p)$$

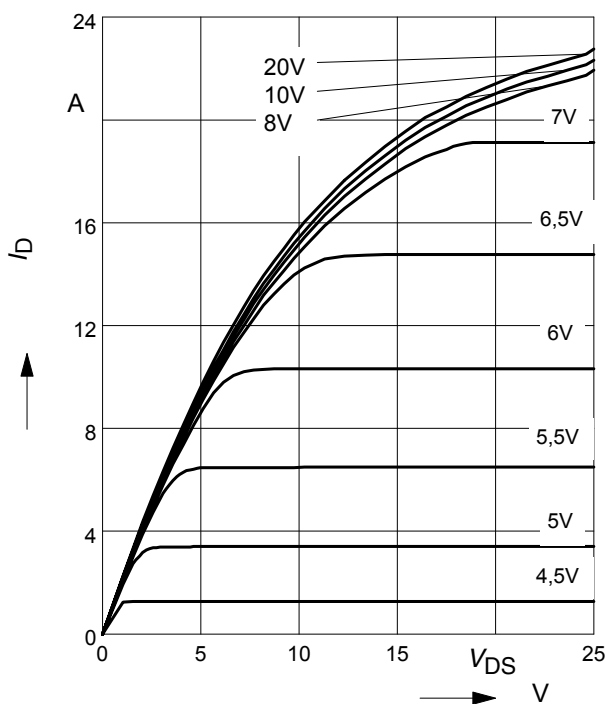
parameter: $D = t_p/t$



7 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

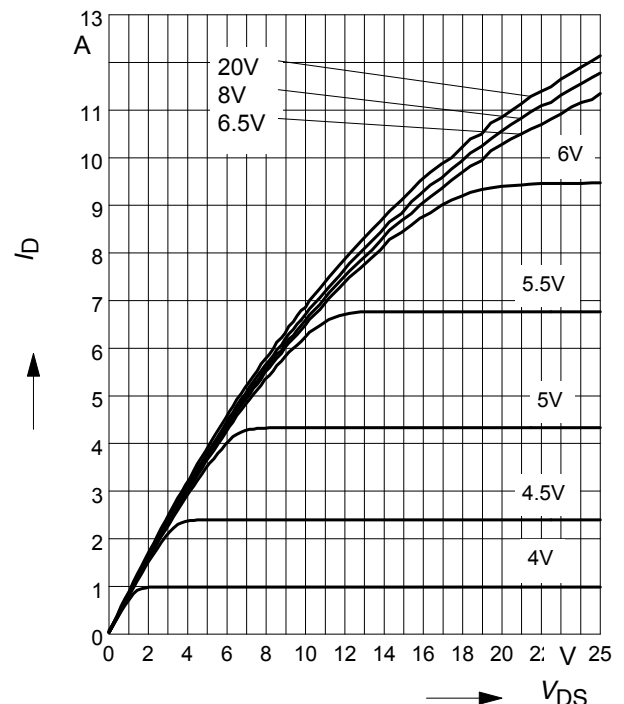
parameter: $t_p = 10 \mu\text{s}, V_{GS}$



8 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 150^\circ\text{C}$$

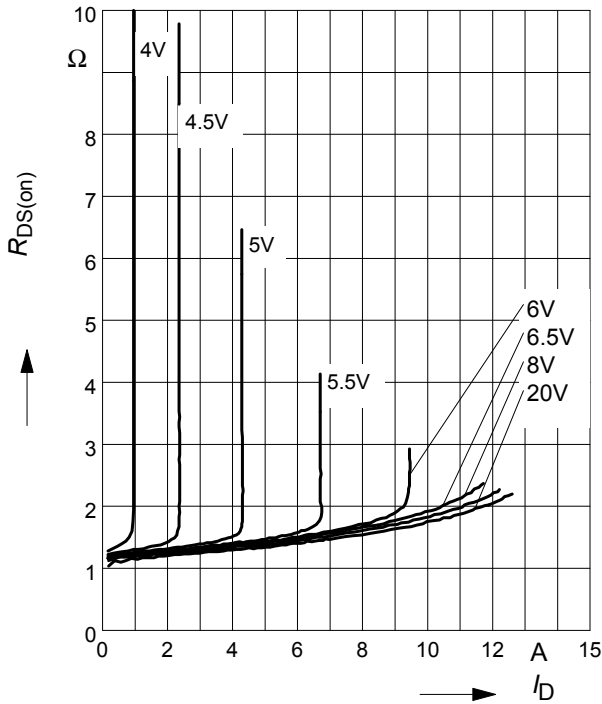
parameter: $t_p = 10 \mu\text{s}, V_{GS}$



9 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D)$$

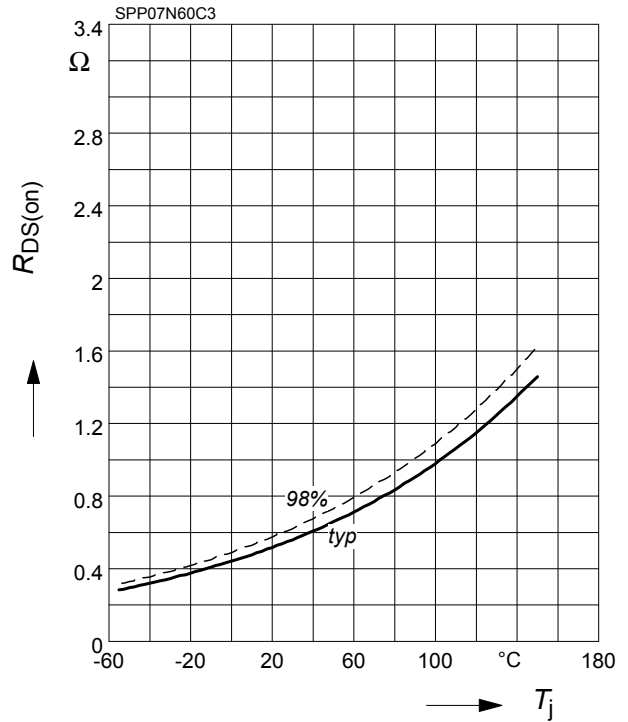
parameter: $T_j = 150^\circ\text{C}$, V_{GS}



10 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

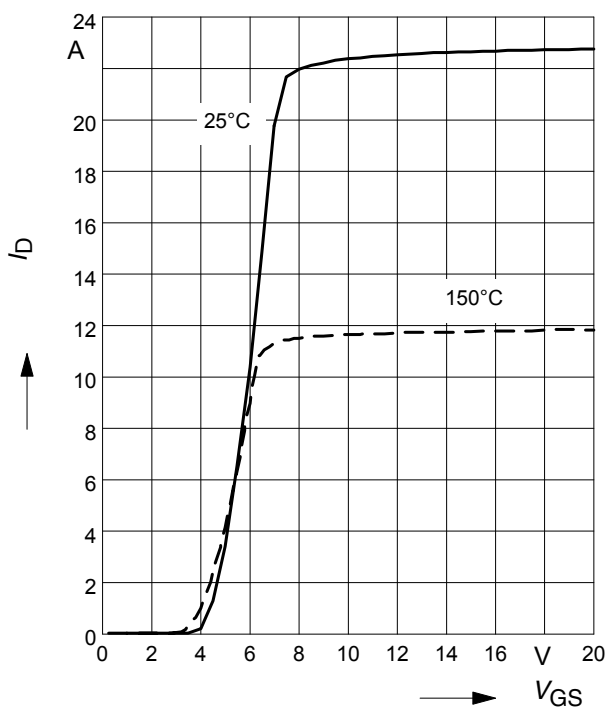
parameter: $I_D = 4.6\text{ A}$, $V_{GS} = 10\text{ V}$



11 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$$

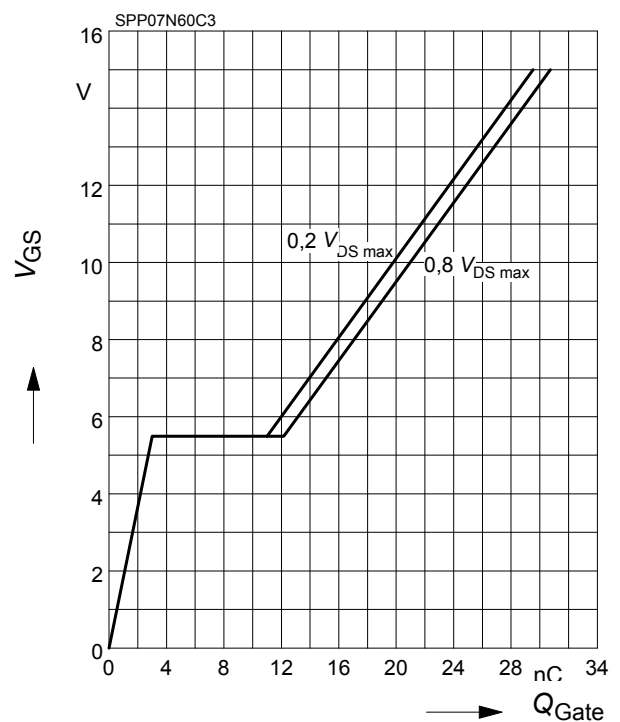
parameter: $t_p = 10\ \mu\text{s}$



12 Typ. gate charge

$$V_{GS} = f(Q_{Gate})$$

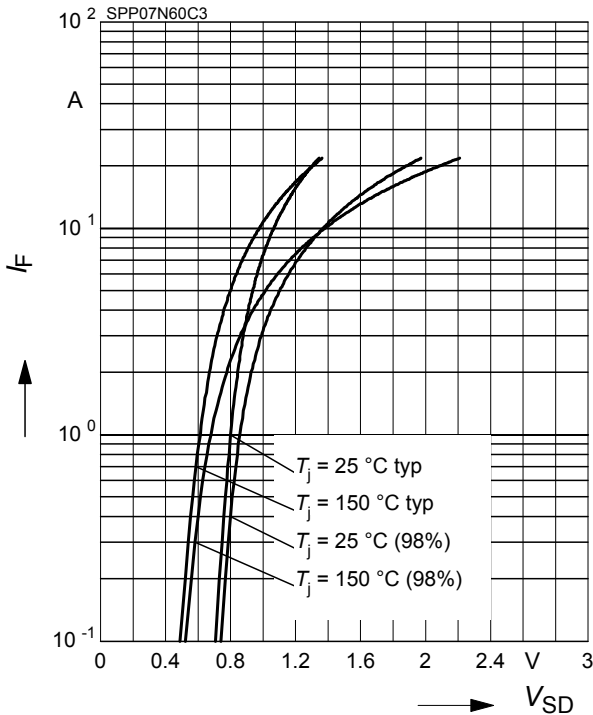
parameter: $I_D = 7.3\text{ A pulsed}$



13 Forward characteristics of body diode

$$I_F = f(V_{SD})$$

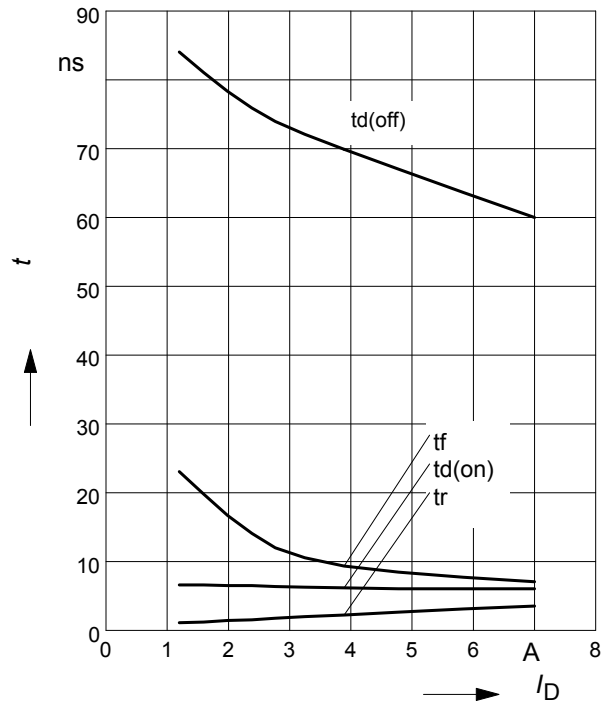
parameter: T_j , $t_p = 10 \mu s$



14 Typ. switching time

$$t = f(I_D), \text{ inductive load, } T_j=125^\circ C$$

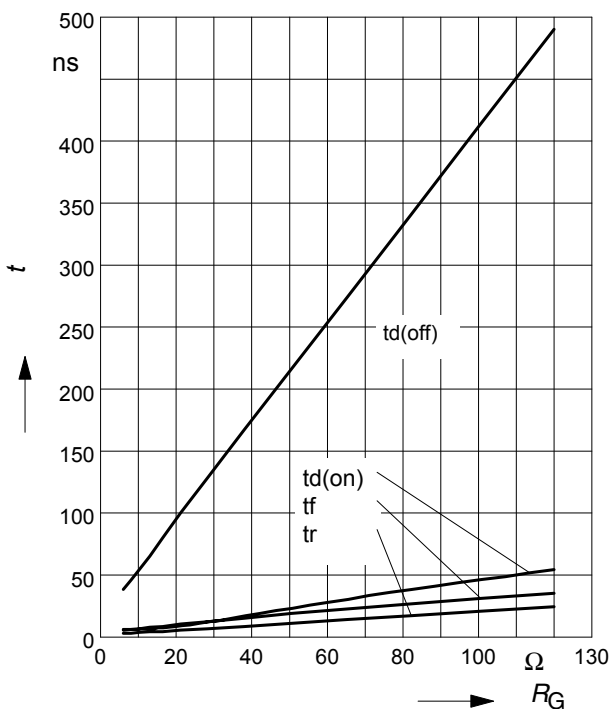
par.: $V_{DS}=380V$, $V_{GS}=0/+13V$, $R_G=12\Omega$



15 Typ. switching time

$$t = f(R_G), \text{ inductive load, } T_j=125^\circ C$$

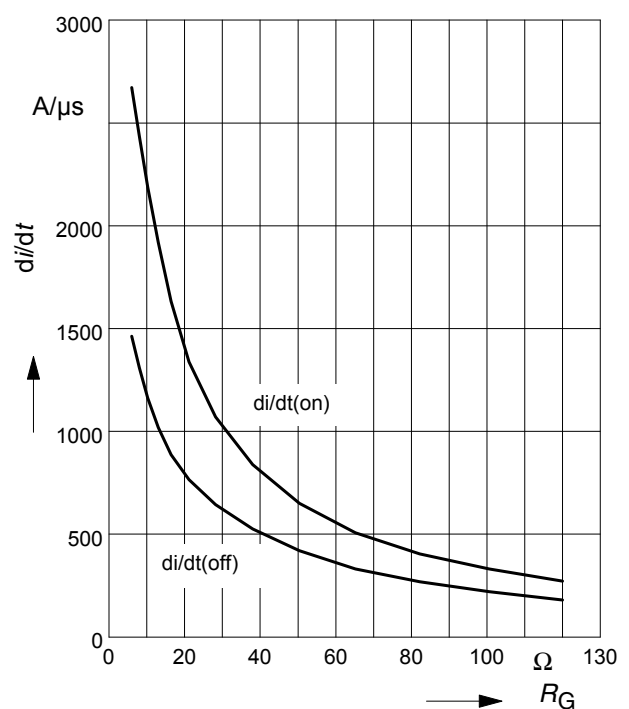
par.: $V_{DS}=380V$, $V_{GS}=0/+13V$, $I_D=7.3 A$



16 Typ. drain current slope

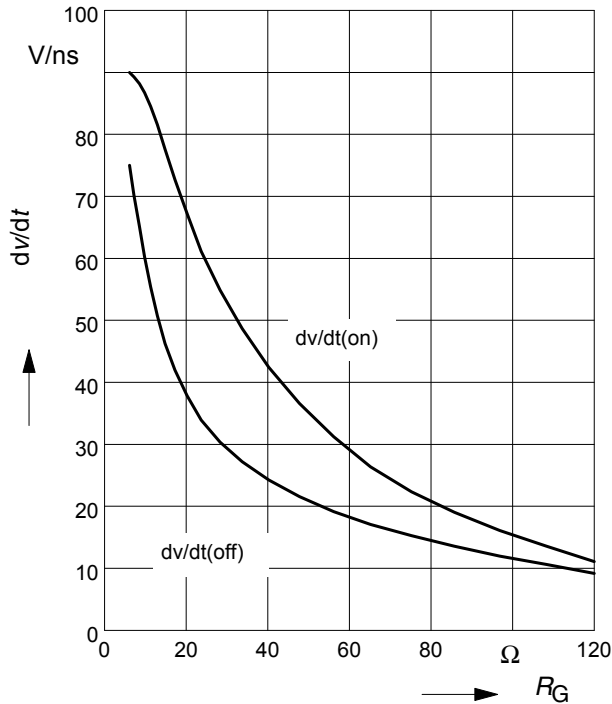
$$di/dt = f(R_G), \text{ inductive load, } T_j = 125^\circ C$$

par.: $V_{DS}=380V$, $V_{GS}=0/+13V$, $I_D=7.3A$



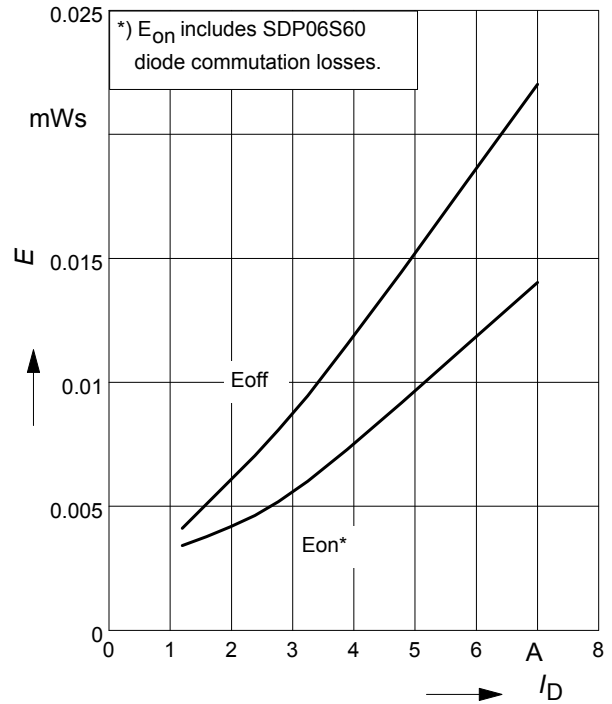
17 Typ. drain source voltage slope

$dv/dt = f(R_G)$, inductive load, $T_j = 125^\circ\text{C}$
 par.: $V_{DS}=380\text{V}$, $V_{GS}=0/+13\text{V}$, $I_D=7.3\text{A}$



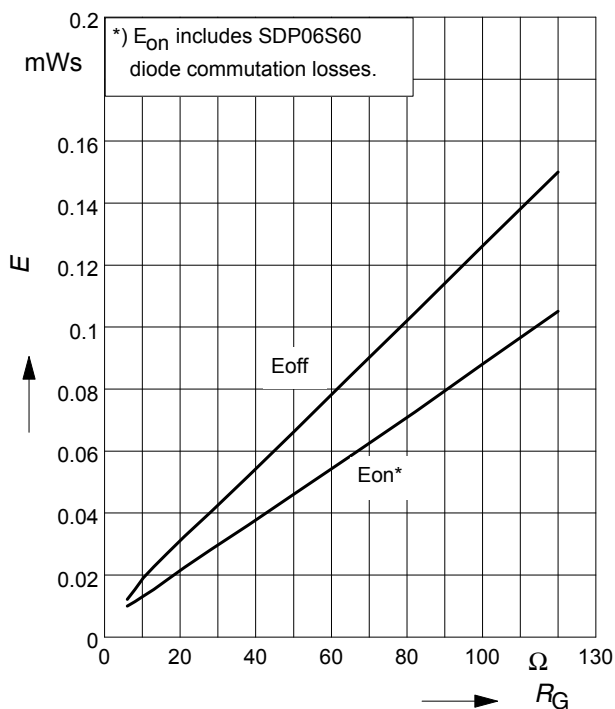
18 Typ. switching losses

$E = f(I_D)$, inductive load, $T_j=125^\circ\text{C}$
 par.: $V_{DS}=380\text{V}$, $V_{GS}=0/+13\text{V}$, $R_G=12\Omega$



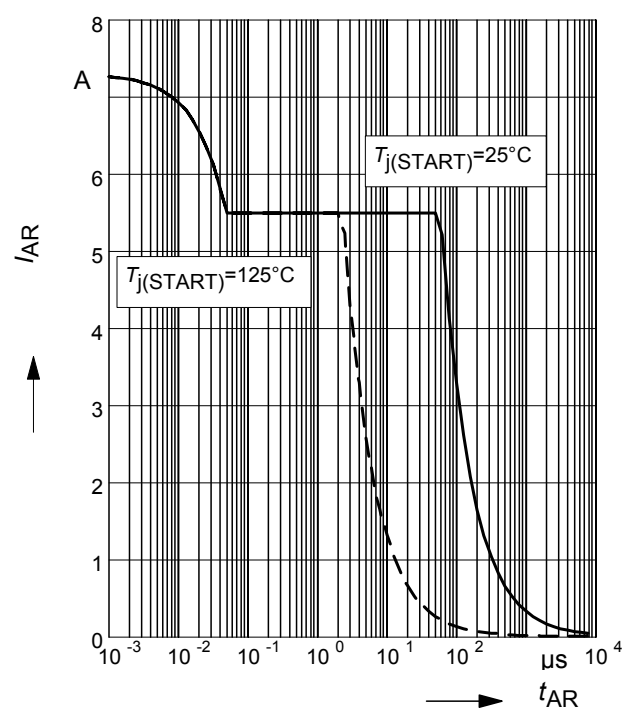
19 Typ. switching losses

$E = f(R_G)$, inductive load, $T_j=125^\circ\text{C}$
 par.: $V_{DS}=380\text{V}$, $V_{GS}=0/+13\text{V}$, $I_D=7.3\text{A}$



20 Avalanche SOA

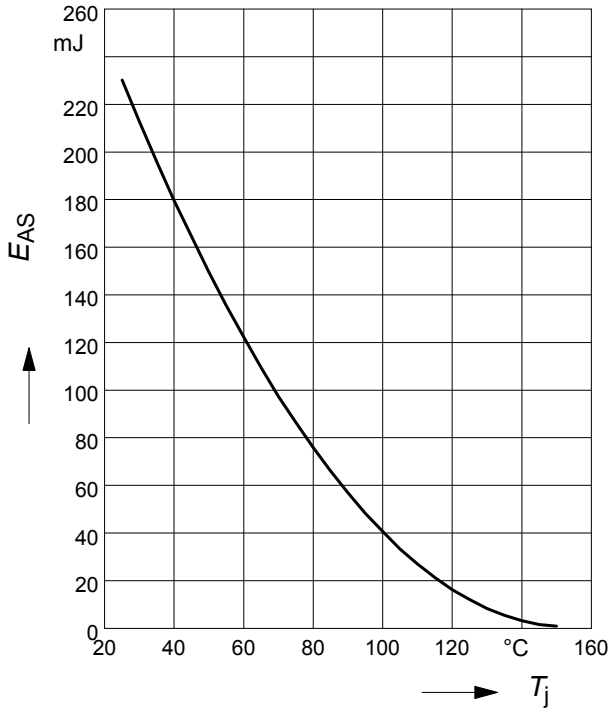
$I_{AR} = f(t_{AR})$
 par.: $T_j \leq 150^\circ\text{C}$



21 Avalanche energy

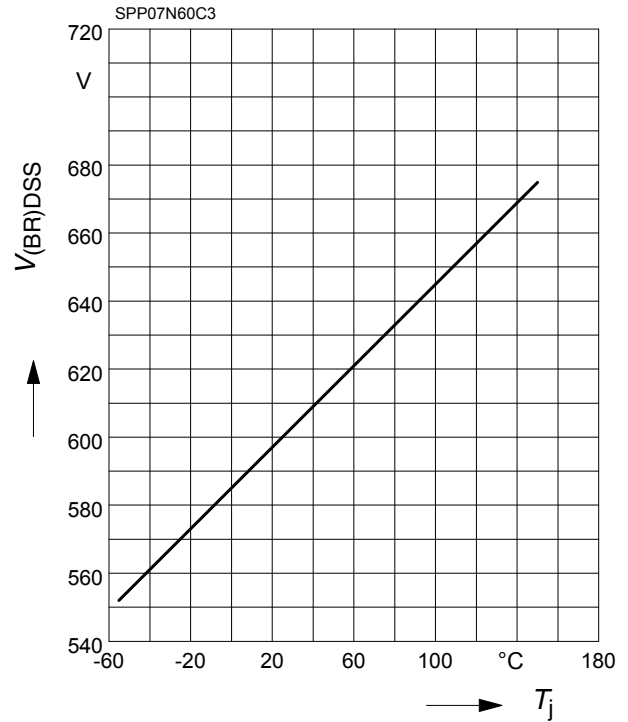
$$E_{AS} = f(T_j)$$

par.: $I_D = 5.5 \text{ A}$, $V_{DD} = 50 \text{ V}$



22 Drain-source breakdown voltage

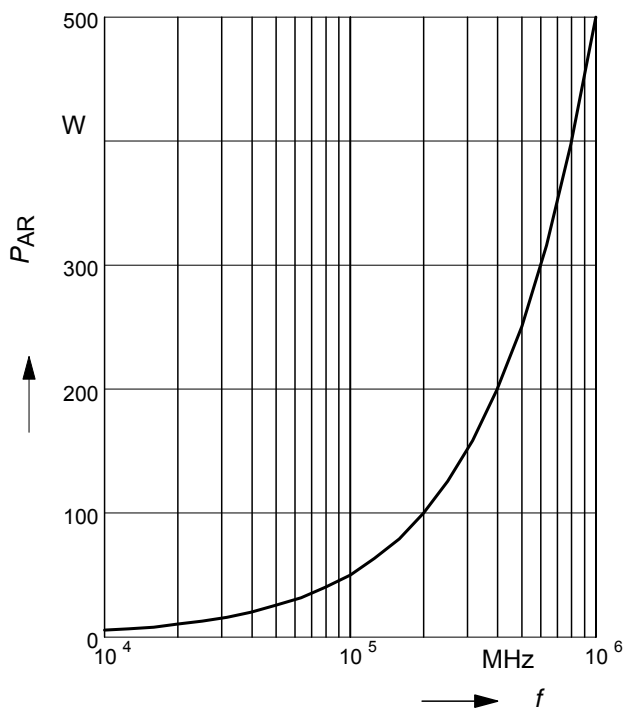
$$V_{(BR)DSS} = f(T_j)$$



23 Avalanche power losses

$$P_{AR} = f(f)$$

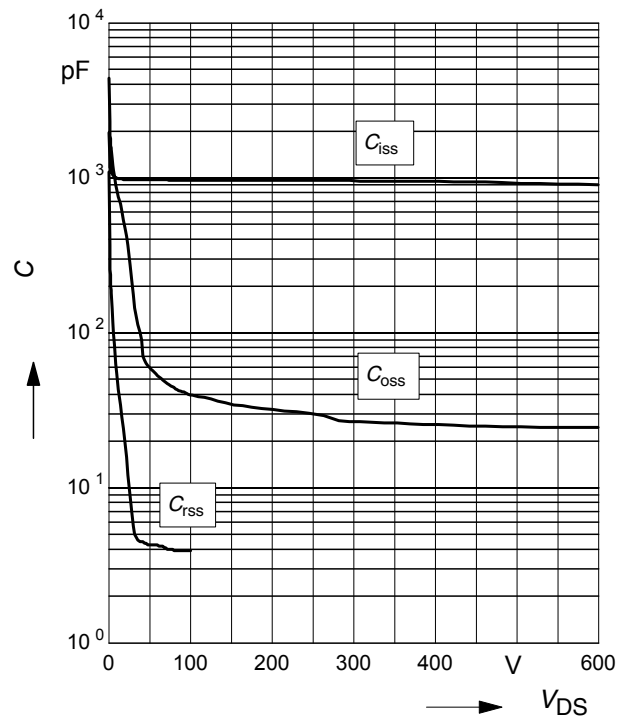
parameter: $E_{AR} = 0.5 \text{ mJ}$



24 Typ. capacitances

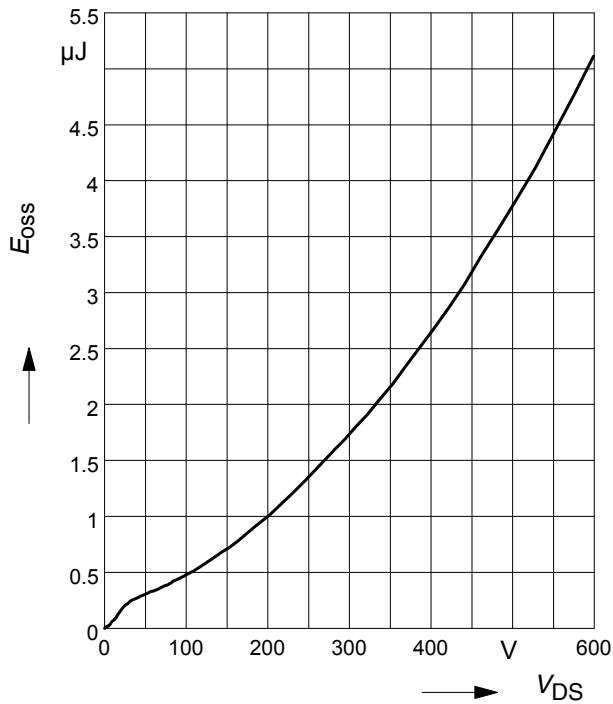
$$C = f(V_{DS})$$

parameter: $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$

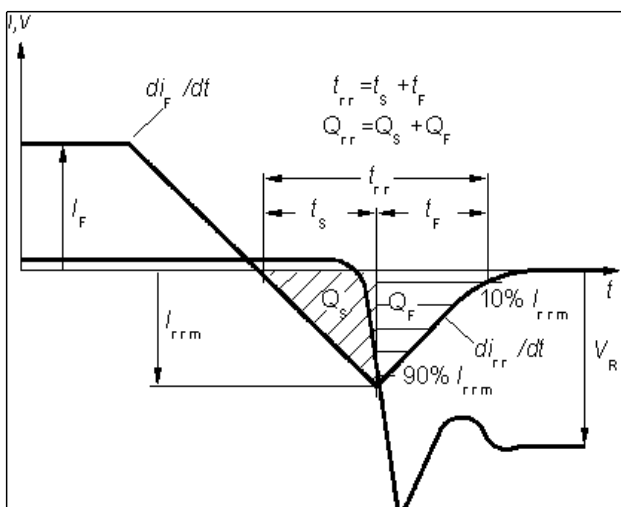


25 Typ. C_{OSS} stored energy

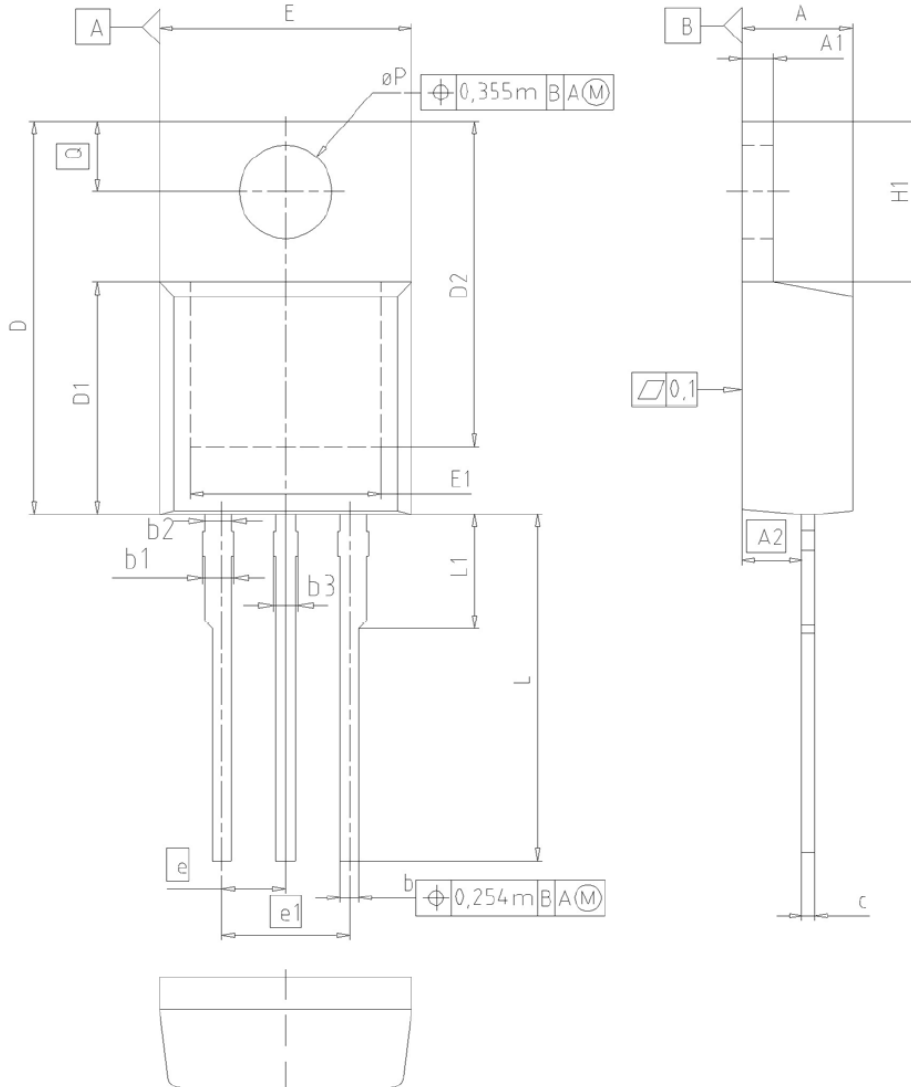
$$E_{OSS} = f(V_{DS})$$



Definition of diodes switching characteristics



PG-TO220-3-1, PG-TO220-3-21 : Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

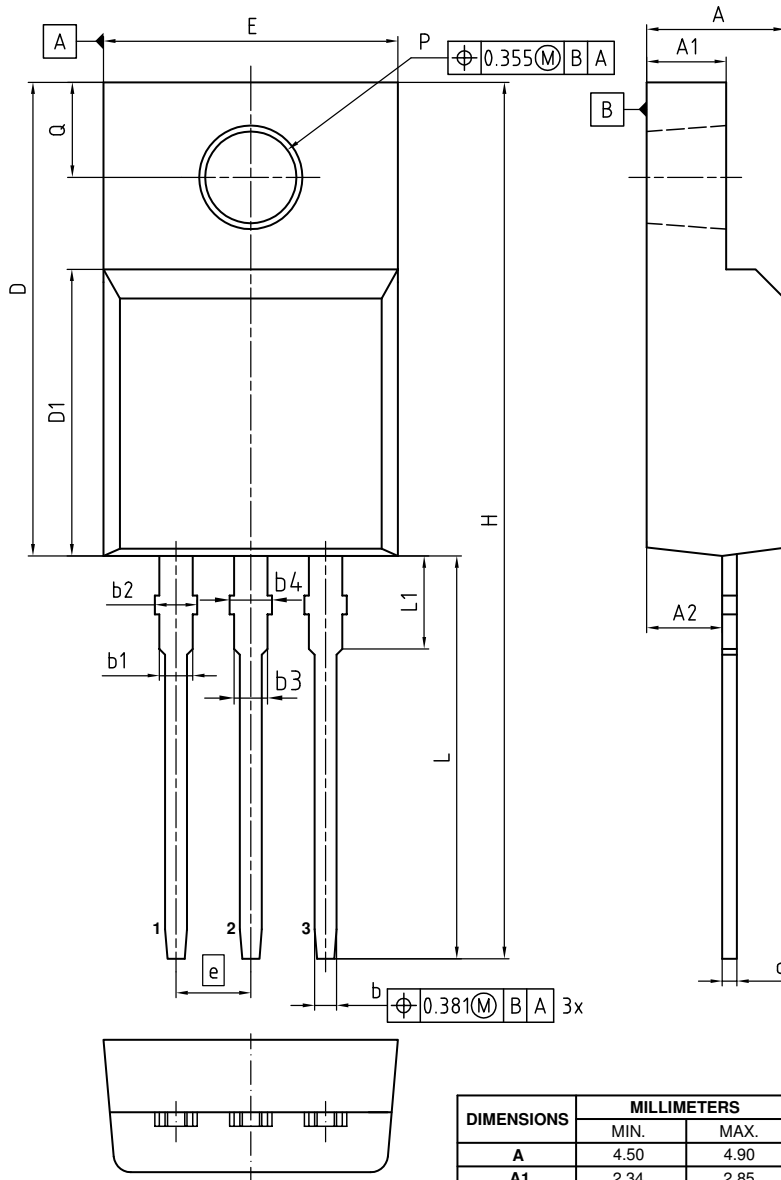
SCALE

EUROPEAN PROJECTION

ISSUE DATE
23-08-2007

REVISION
05

Outline PG-TO220 FullPAK

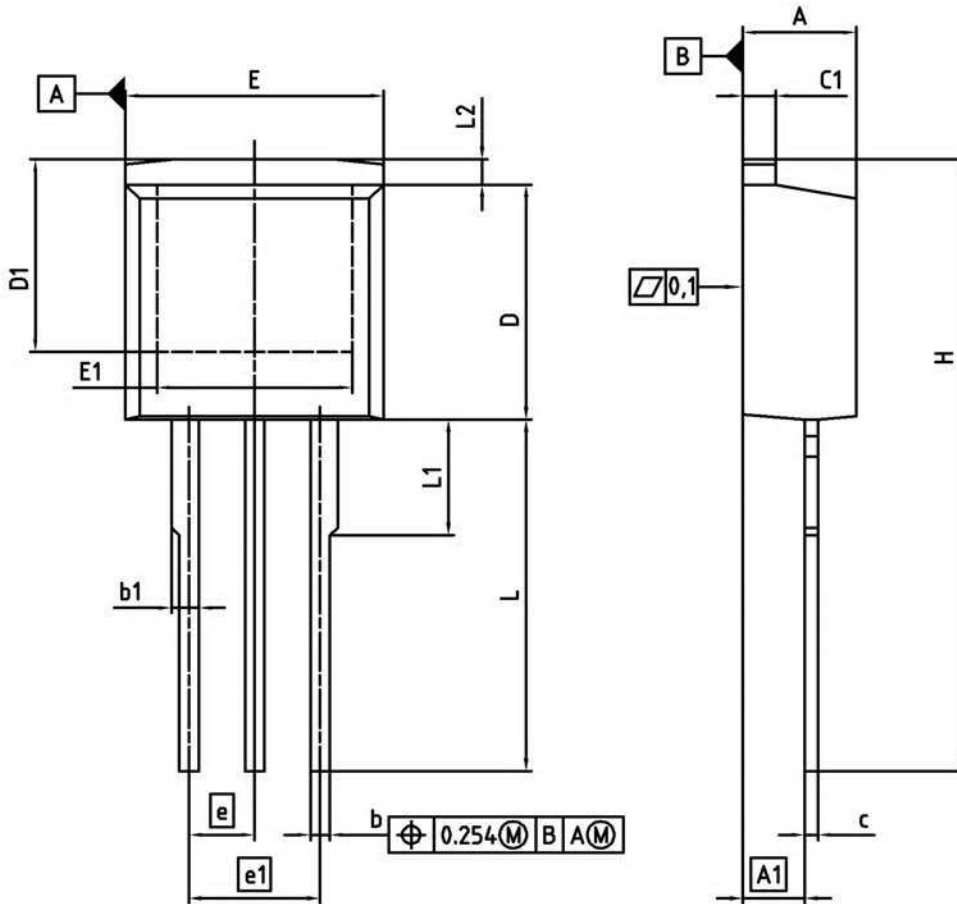


NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281
AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS
OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

DOCUMENT NO. Z8B00003319
REVISION 07
SCALE 5:1 0 1 2 3 4 5mm
EUROPEAN PROJECTION
ISSUE DATE 27.01.2017

PG-TO-262-3-1/PG-TO262-3-21 (I²-PAK)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.635	1.400	0.025	0.055
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE
JEDEC TO262

EUROPEAN PROJECTION

ISSUE DATE
05-05-2006

FILE
TO262_1

600V CoolMOS™ C3 Power Transistor

SPx07N60C3

Revision History

SPx07N60C3

Revision: 2018-02-27, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
3.3	2018-02-27	Outline PG-TO-220 FullPAK update

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Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.