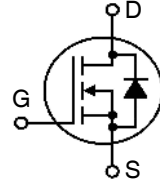


**Q3-Class
HiperFET™
Power MOSFET**

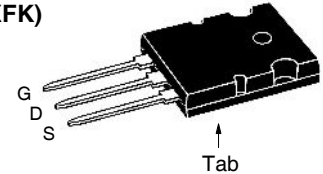
**IXFK80N50Q3
IXFX80N50Q3**

$V_{DSS} = 500V$
 $I_{D25} = 80A$
 $R_{DS(on)} \leq 65m\Omega$
 $t_{rr} \leq 250ns$

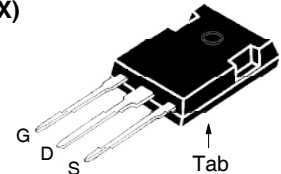
N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Rectifier



TO-264
(IXFK)



PLUS247
(IXFX)



G = Gate D = Drain
 S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	80	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	240	A
I_A	$T_C = 25^\circ C$	80	A
E_{AS}	$T_C = 25^\circ C$	5	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	50	V/ns
P_D	$T_C = 25^\circ C$	1250	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in
F_C	Mounting Force (PLUS247)	20..120 / 4.5..27	N/lb
Weight	TO-264	10	g
	PLUS247	6	g

Features

- Low Intrinsic Gate Resistance
- Low Package Inductance
- Fast Intrinsic Rectifier
- Low $R_{DS(on)}$ and Q_G

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- DC Choppers
- Temperature and Lighting Controls

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 3mA$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8mA$	3.5		V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			50 μA 2 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			65 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}, I_D = 0.5 \cdot I_{D25}$, Note 1	35	55	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		10	nF
C_{oss}			1260	pF
C_{rss}			115	pF
R_{Gi}	Gate Input Resistance		0.15	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		30	ns
t_r			20	ns
$t_{d(off)}$			43	ns
t_f			15	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		200	nC
Q_{gs}			77	nC
Q_{gd}			90	nC
R_{thJC}				0.10 $^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			80 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			320 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{V}$, Note 1			1.4 V
t_{rr}	$I_F = 40\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			250 ns
Q_{RM}			1.8	μC
I_{RM}			15.6	A

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

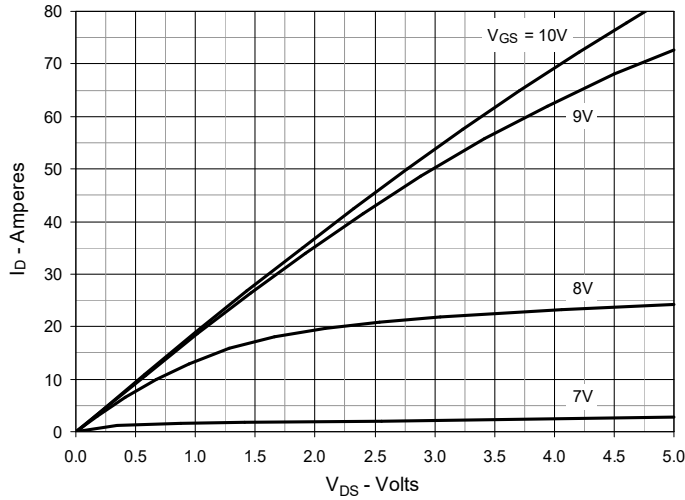


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

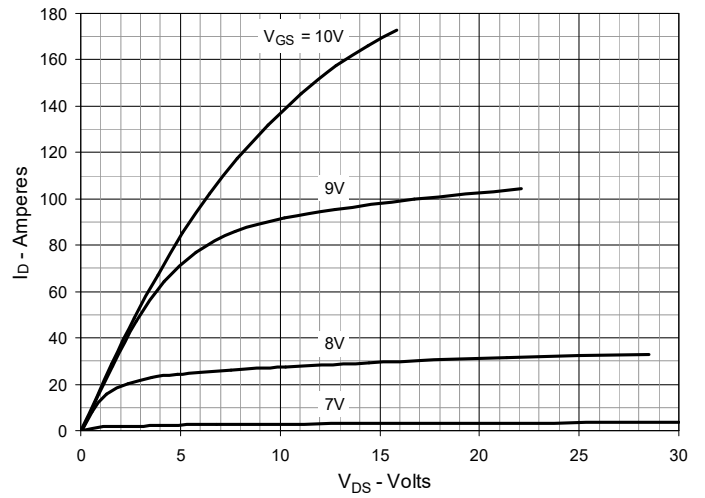


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

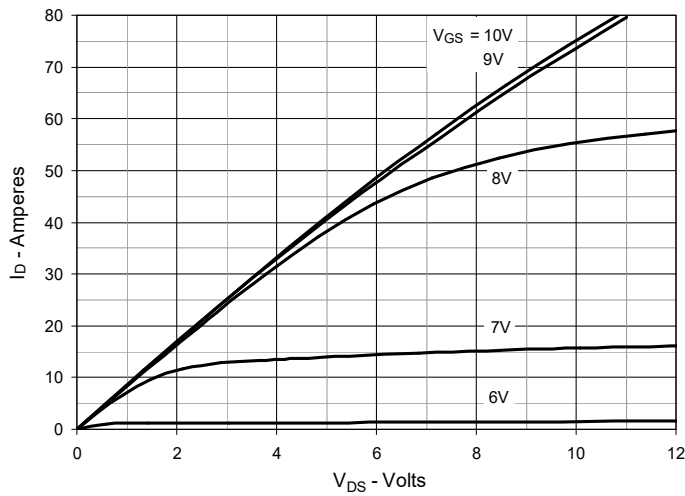


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 40\text{A}$ Value vs. Junction Temperature

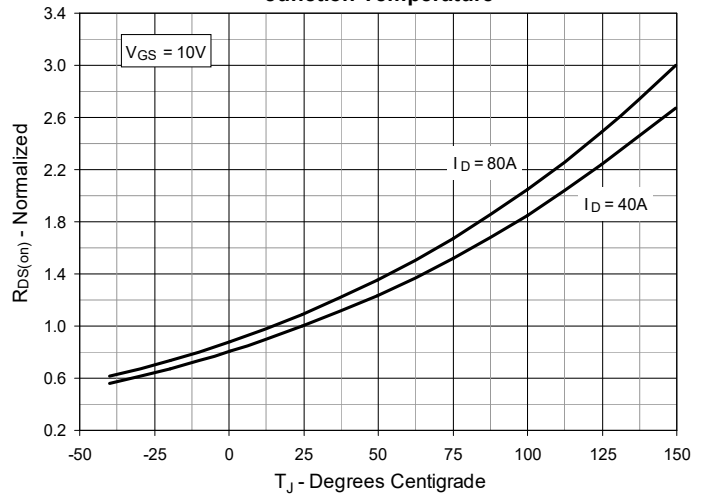


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 40\text{A}$ Value vs. Drain Current

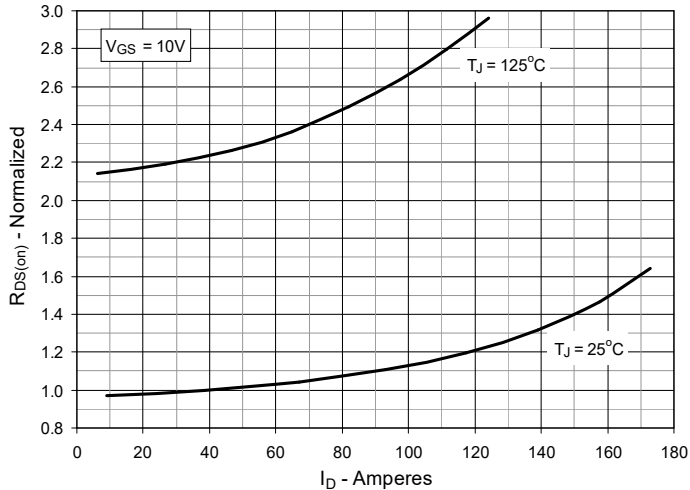


Fig. 6. Maximum Drain Current vs. Case Temperature

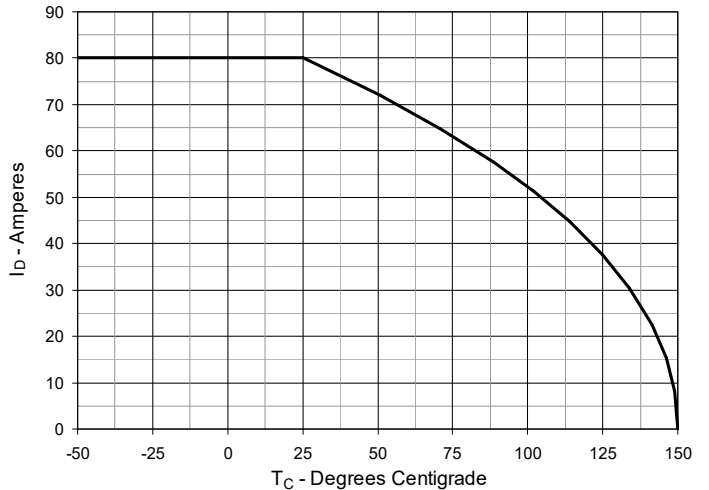


Fig. 7. Input Admittance

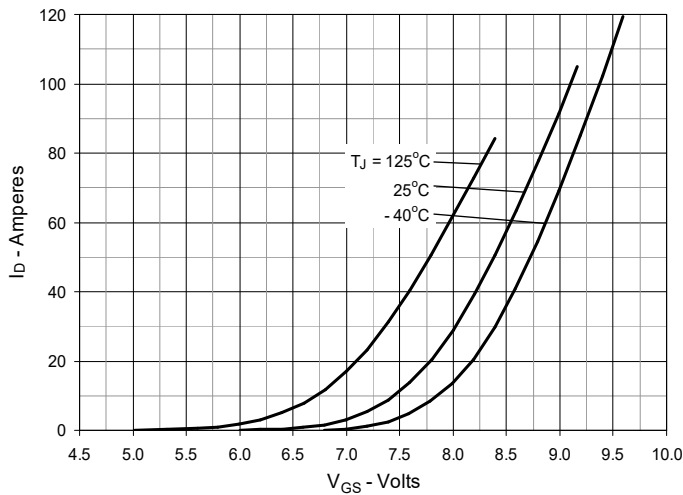


Fig. 8. Transconductance

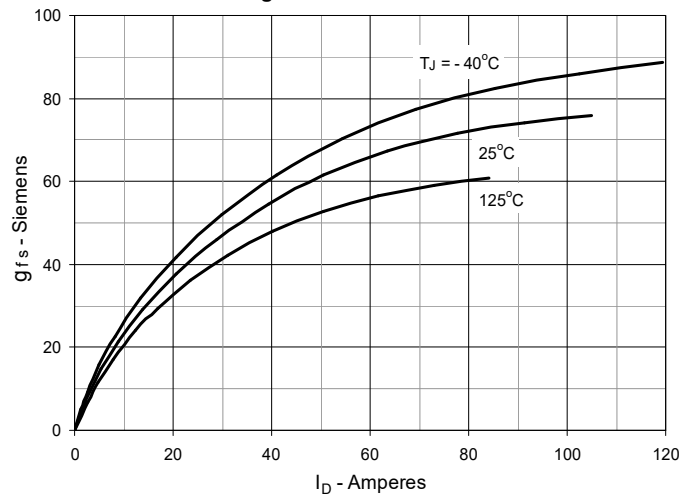


Fig. 9. Forward Voltage Drop of Intrinsic Diode

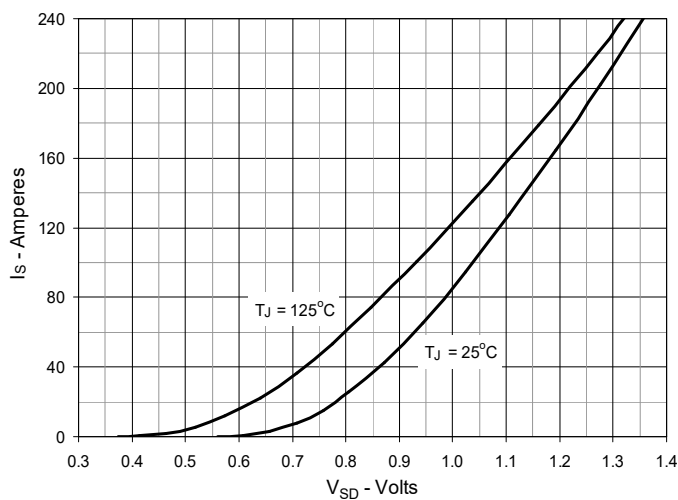


Fig. 10. Gate Charge

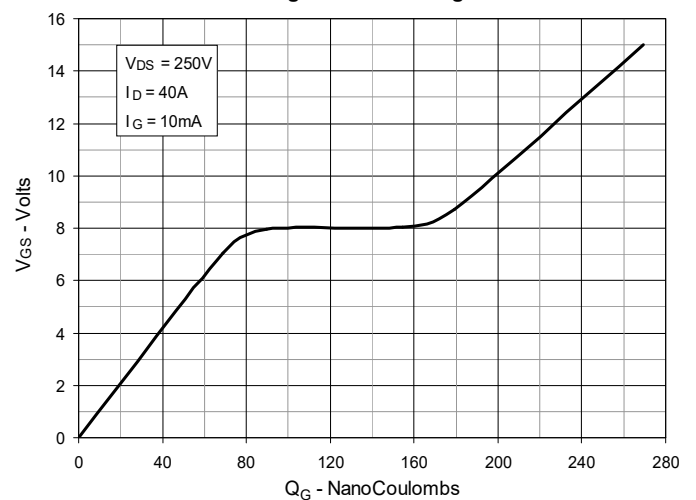


Fig. 11. Capacitance

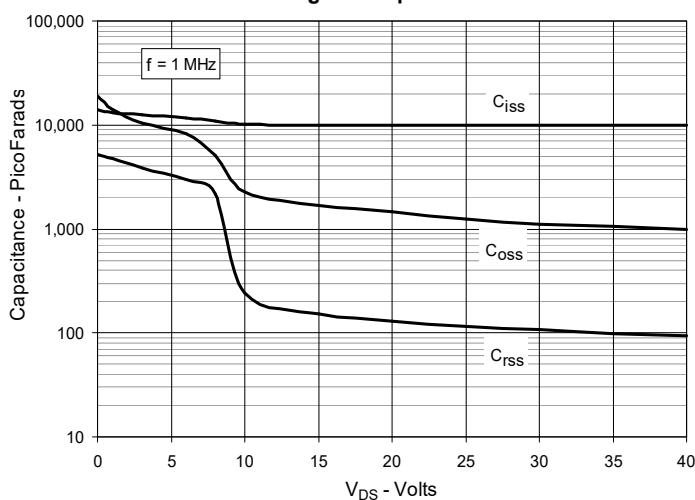


Fig. 12. Forward-Bias Safe Operating Area

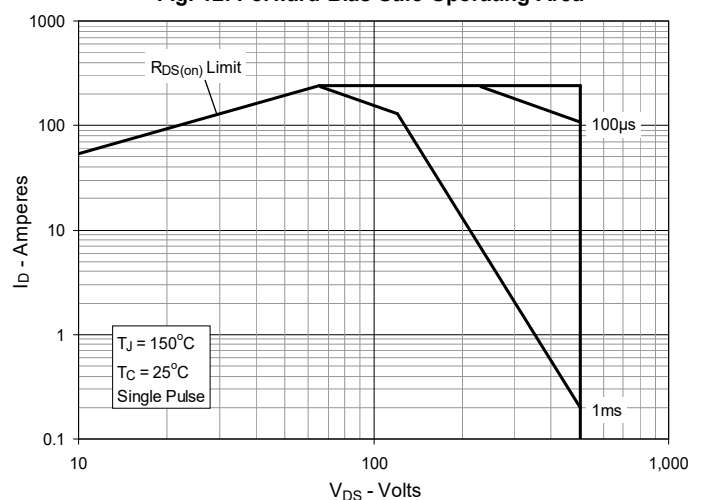
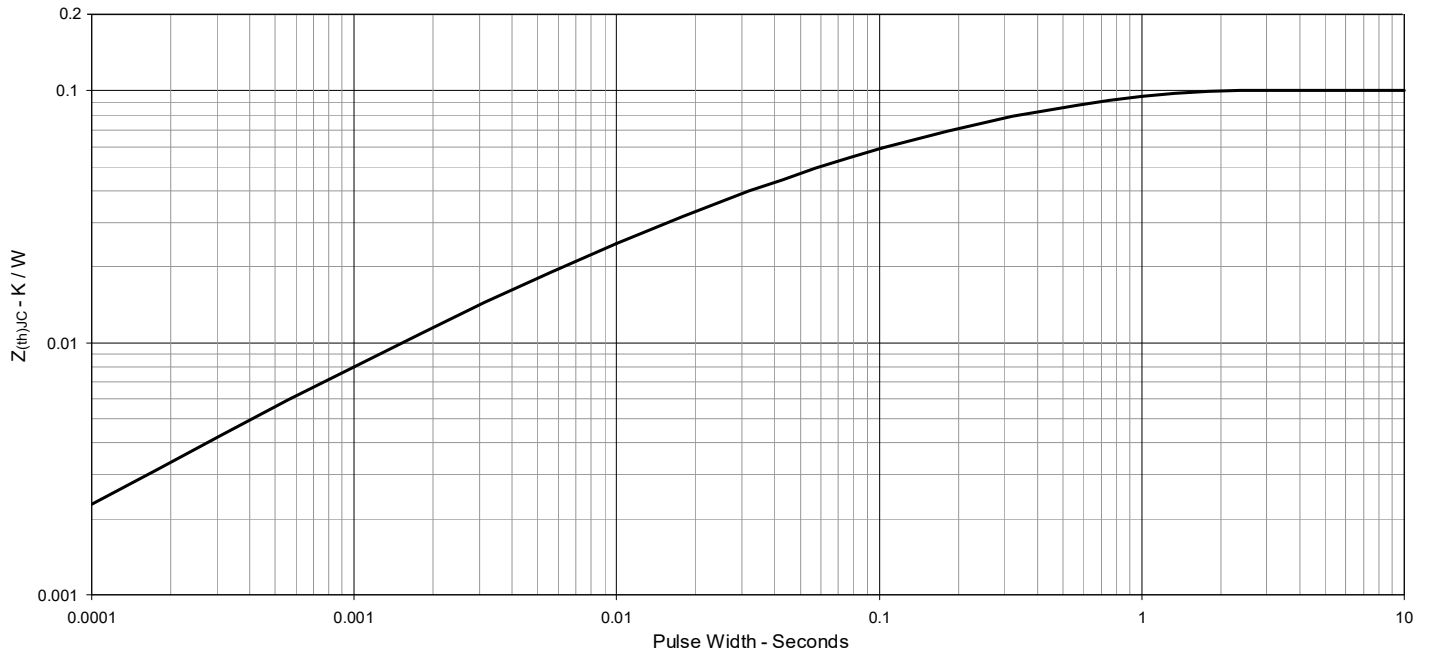
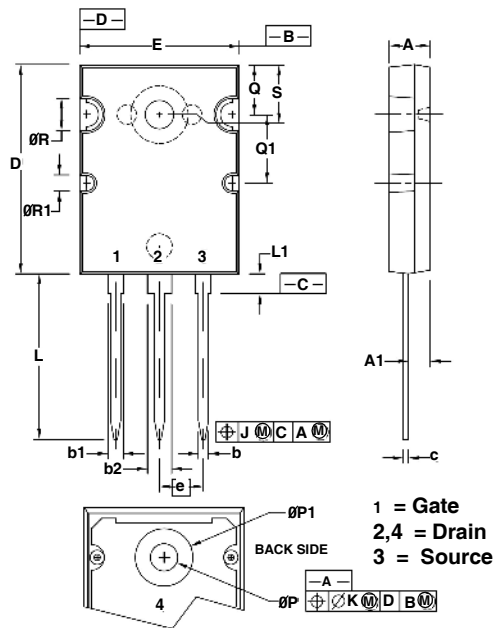


Fig. 13. Maximum Transient Thermal Impedance

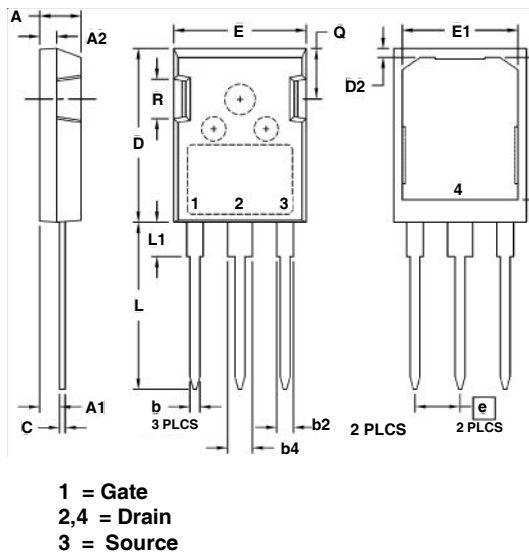


TO-264 Outline



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
∅P	.122	.138	3.10	3.51
∅P1	.270	.290	6.86	7.37
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
∅R	.155	.187	3.94	4.75
∅R1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

PLUS247™ Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.520	.560	13.08	14.22
e	.215 BSC		5.45 BSC	
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83



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