

## N-Channel Depletion-Mode Vertical DMOS FET

### Features

- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

### Applications

- Normally-On Switches
- Solid-State Relays
- Converters
- Linear Amplifiers
- Constant-Current Sources
- Power Supply Circuits
- Telecommunications

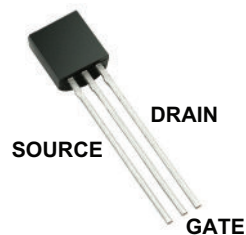
### General Description

The DN3545 Depletion-mode normally-on transistor uses an advanced vertical Diffusion Metal Oxide Semiconductor (DMOS) structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power-handling capabilities of bipolar transistors and the high-input impedance and positive-temperature coefficient inherent in Metal-Oxide Semiconductor (MOS) devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

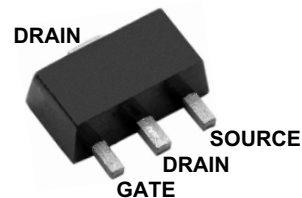
Vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

### Package Types

**3-lead TO-92**  
(Top view)



**3-lead SOT-89**  
(Top view)



See [Table 3-1](#) and [Table 3-2](#) for pin information.

# DN3545

## 1.0 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS†

|   |                   |
|---|-------------------|
| Drain-to-Source Voltage.....                        | BV <sub>DSX</sub> |
| Drain-to-Gate Voltage.....                          | BV <sub>DGX</sub> |
| Gate-to-Source Voltage.....                         | ±20V              |
| Operating Ambient Temperature, T <sub>A</sub> ..... | -55°C to +150°C   |
| Storage Temperature, T <sub>S</sub> .....           | -55°C to +150°C   |

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** T<sub>A</sub> = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle.

| Parameter                                      | Sym.                  | Min. | Typ. | Max. | Unit  | Conditions  |
|--|-----------------------|------|------|------|-------|---|
| Drain-to-Source Breakdown Voltage              | BV <sub>DSX</sub>     | 450  | —    | —    | V     | V <sub>GS</sub> = -5V, I <sub>D</sub> = 100 μA  |
| Gate-to-Source Off Voltage                     | V <sub>GS(OFF)</sub>  | -1.5 | —    | -3.5 | V     | V <sub>DS</sub> = 25V, I <sub>D</sub> = 10 μA   |
| V <sub>GS(OFF)</sub> Change with Temperature   | ΔV <sub>GS(OFF)</sub> | —    | —    | -4.5 | mV/°C | V <sub>DS</sub> = 25V, I <sub>D</sub> = 10 μA ( <b>Note 1</b> )                                       |
| Gate Body Leakage Current                      | I <sub>GSS</sub>      | —    | —    | 100  | nA    | V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V  |
| Drain-to-Source Leakage Current                | I <sub>D(OFF)</sub>   | —    | —    | 1    | μA    | V <sub>DS</sub> = Maximum rating, V <sub>GS</sub> = -5V   |
|  |                       | —    | —    | 1    | mA    | V <sub>DS</sub> = 0.8 Maximum rating, V <sub>GS</sub> = -5V, T <sub>A</sub> = 125°C ( <b>Note 1</b> ) |
| Saturated Drain-to-Source Current              | I <sub>DSS</sub>      | 200  | —    | —    | mA    | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V   |
| Static Drain-to-Source On-State Resistance     | R <sub>DS(ON)</sub>   | —    | —    | 20   | Ω     | V <sub>GS</sub> = 0V, I <sub>D</sub> = 150 mA   |
| Change in R <sub>DS(ON)</sub> with Temperature | ΔR <sub>DS(ON)</sub>  | —    | —    | 1.1  | %/°C  | V <sub>GS</sub> = 0V, I <sub>D</sub> = 150 mA ( <b>Note 1</b> )                                       |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

### AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise specified, for all specifications T<sub>A</sub> = 25°C. Specification is obtained by characterization and is not 100% tested.

| Parameter                        | Sym.                | Min. | Typ. | Max. | Unit | Conditions  |
|----------------------------------|---------------------|------|------|------|------|---|
| Forward Transconductance         | G <sub>FS</sub>     | 150  | —    | —    | mmho | V <sub>DS</sub> = 10V, I <sub>D</sub> = 100 mA  |
| Input Capacitance                | C <sub>ISS</sub>    | —    | —    | 360  | pF   | V <sub>GS</sub> = -5V,<br>V <sub>DS</sub> = 25V,<br>f = 1 MHz   |
| Common Source Output Capacitance | C <sub>OSS</sub>    | —    | —    | 40   | pF   |   |
| Reverse Transfer Capacitance     | C <sub>RSS</sub>    | —    | —    | 15   | pF   |   |
| Turn-On Delay Time               | t <sub>d(ON)</sub>  | —    | —    | 20   | ns   | V <sub>DD</sub> = 25V,<br>I <sub>D</sub> = 150 mA,<br>R <sub>GEN</sub> = 25Ω,<br>V <sub>GS</sub> = 0V to -10V |
| Rise Time                        | t <sub>r</sub>      | —    | —    | 30   | ns   |   |
| Turn-Off Delay Time              | t <sub>d(OFF)</sub> | —    | —    | 30   | ns   |   |
| Fall Time                        | t <sub>f</sub>      | —    | —    | 40   | ns   |   |

#### DIODE PARAMETER

|                            |                 |   |     |     |    |   |
|----------------------------|-----------------|---|-----|-----|----|---|
| Diode Forward Voltage Drop | V <sub>SD</sub> | — | —   | 1.8 | V  | V <sub>GS</sub> = -5V, I <sub>SD</sub> = 150 mA ( <b>Note 1</b> ) |
| Reverse Recovery Time      | t <sub>rr</sub> | — | 800 | —   | ns | V <sub>GS</sub> = -5V, I <sub>SD</sub> = 150 mA                   |

**Note 1:** All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle.

## TEMPERATURE SPECIFICATIONS

| Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25^\circ\text{C}$ . |               |      |      |      |                    |            |
|---|---------------|------|------|------|--------------------|------------|
| Parameter   | Sym.          | Min. | Typ. | Max. | Unit               | Conditions |
| <b>TEMPERATURE RANGE</b>  |               |      |      |      |                    |            |
| Operating Ambient Temperature   | $T_A$         | -55  | —    | 150  | $^\circ\text{C}$   |            |
| Storage Temperature   | $T_S$         | -55  | —    | 150  | $^\circ\text{C}$   |            |
| <b>PACKAGE THERMAL RESISTANCE</b>   |               |      |      |      |                    |            |
| 3-lead TO-92  | $\theta_{JA}$ | —    | 132  | —    | $^\circ\text{C/W}$ |            |
| 3-lead SOT-89   | $\theta_{JA}$ | —    | 133  | —    | $^\circ\text{C/W}$ |            |

## THERMAL CHARACTERISTICS

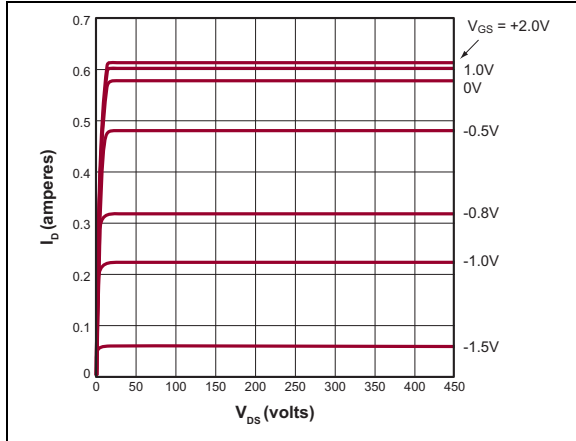
| Package       | $I_D$ (Note 1)<br>Continuous<br>(mA) | $I_D$<br>Pulsed<br>(mA) | Power<br>Dissipation<br>at $T_C = 25^\circ\text{C}$<br>(W) | $I_{DR}$ (Note 1)<br>(mA) | $I_{DRM}$<br>(mA) |
|---------------|--------------------------------------|-------------------------|--|---------------------------|-------------------|
| 3-lead TO-92  | 136                                  | 1600                    | 0.74   | 136                       | 1600              |
| 3-lead SOT-89 | 200                                  | 300                     | 1.6 (Note 2)   | 200                       | 300               |

**Note 1:**  $I_D$  continuous is limited by the maximum rated  $T_J$ .

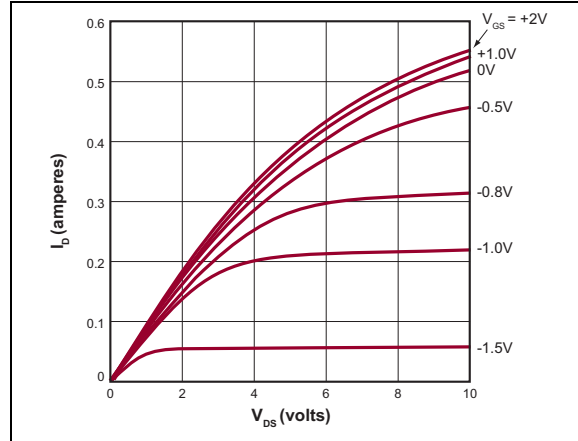
**Note 2:** Mounted on an FR4 board, 25 mm x 25 mm x 1.57 mm

## 2.0 TYPICAL PERFORMANCE CURVES

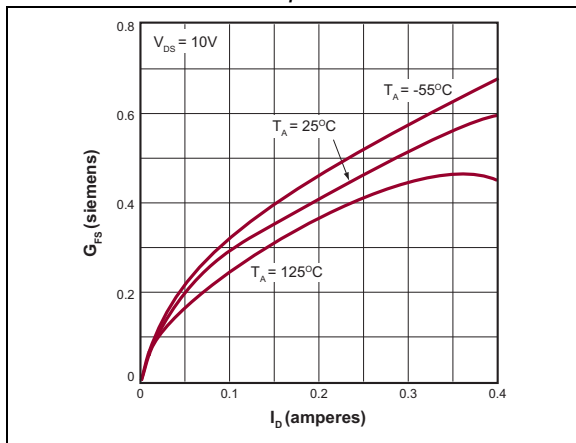
**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.



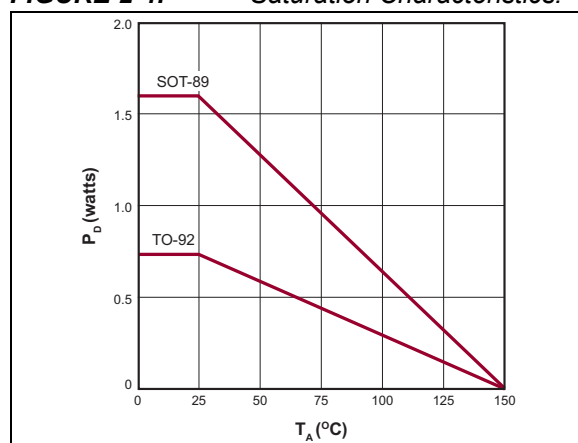
**FIGURE 2-1:** Output Characteristics.



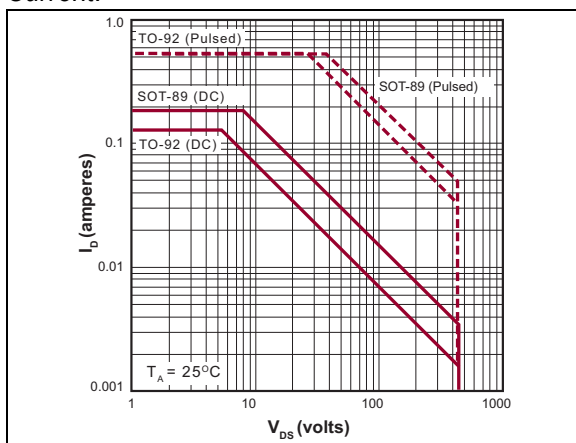
**FIGURE 2-4:** Saturation Characteristics.



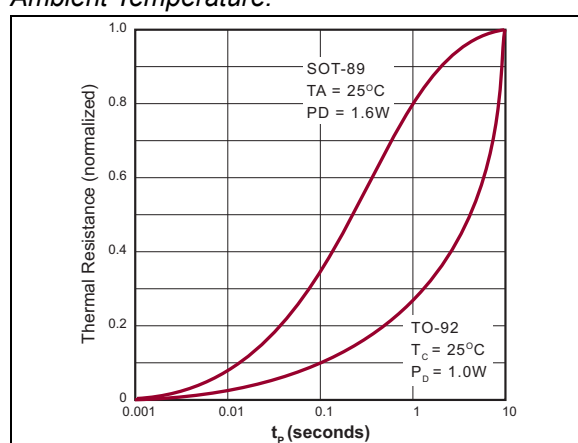
**FIGURE 2-2:** Transconductance vs. Drain Current.



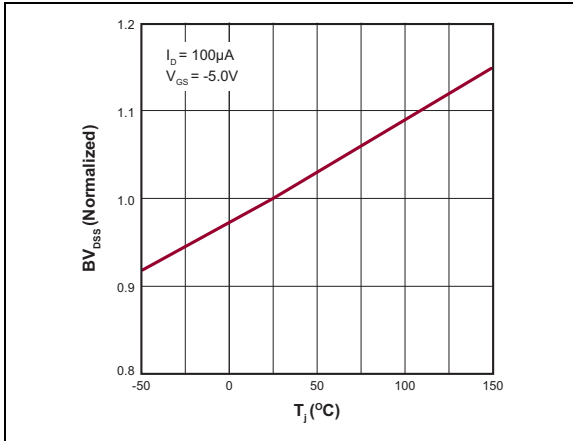
**FIGURE 2-5:** Power Dissipation vs. Ambient Temperature.



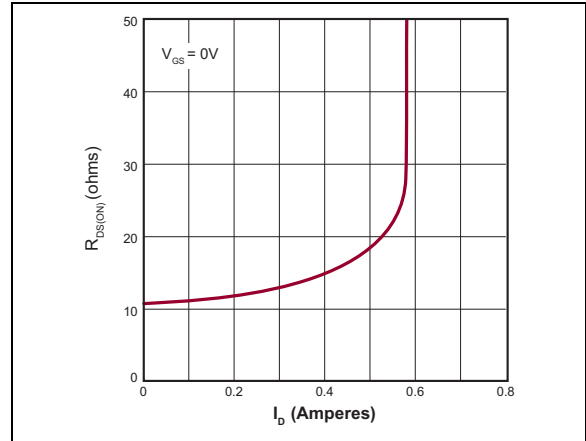
**FIGURE 2-3:** Maximum Rated Safe Operating Area.



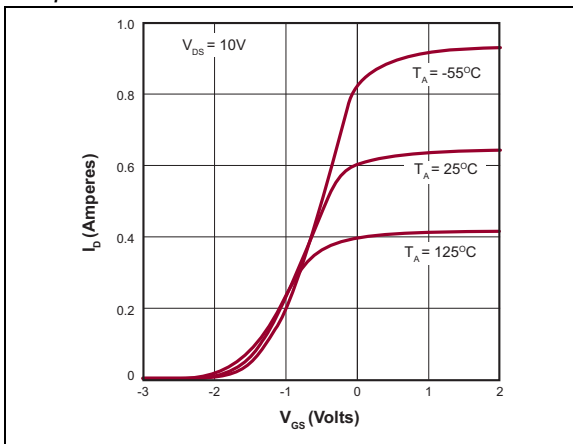
**FIGURE 2-6:** Thermal Response Characteristics.



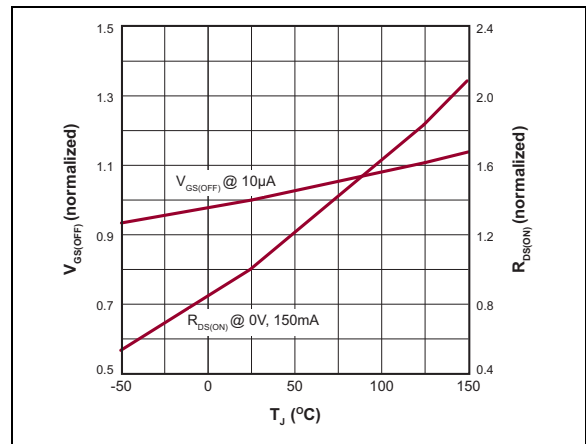
**FIGURE 2-7:**  $BV_{DSS}$  Variation with Temperature.



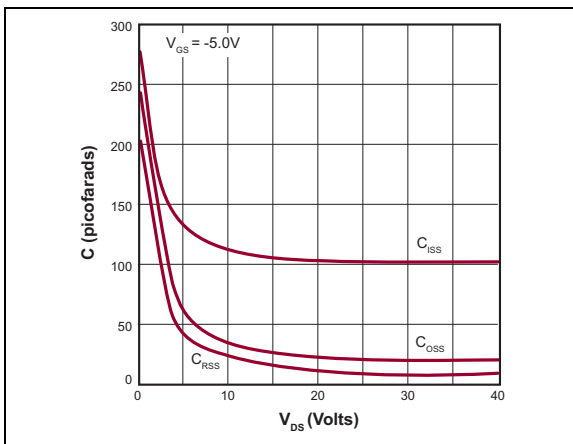
**FIGURE 2-10:** On-Resistance vs. Drain Current.



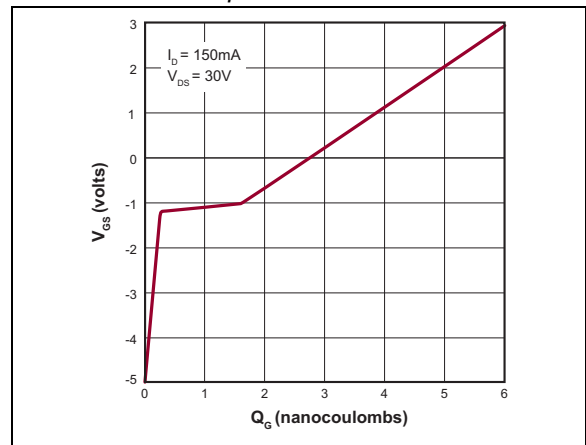
**FIGURE 2-8:** Transfer Characteristics.



**FIGURE 2-11:**  $V_{GS(th)}$  and  $R_{DS(ON)}$  Variation with Temperature.



**FIGURE 2-9:** Capacitance vs. Drain-to-Source Voltage.



**FIGURE 2-12:** Gate Drive Dynamic Characteristics.

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## 3.0 PIN DESCRIPTION

The details on the pins of 3-lead TO-92 and 3-lead SOT-89 packages are listed on [Table 3-1](#) and [Table 3-2](#), respectively. The locations of pins are indicated in [Package Types](#).

**TABLE 3-1: 3-LEAD TO-92 PIN FUNCTION TABLE**

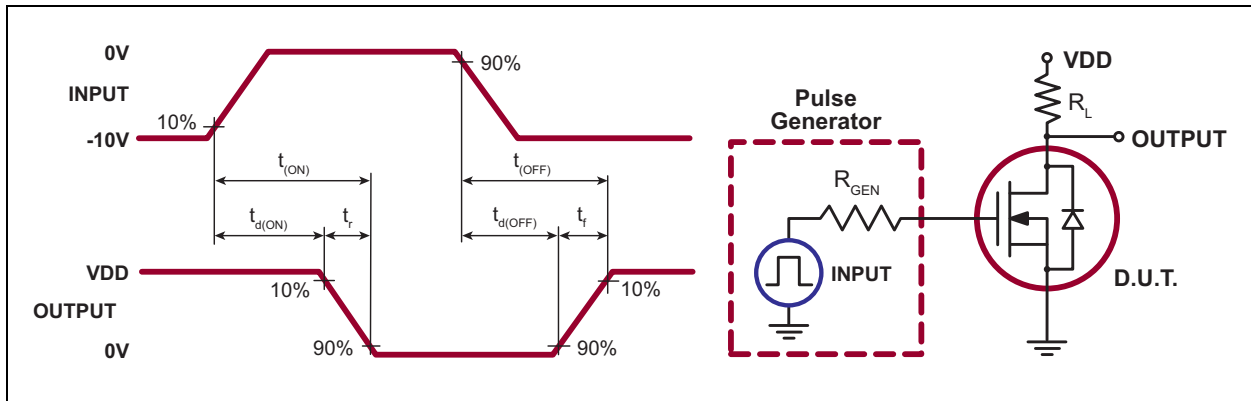
| Pin Number | Pin Name | Description |
|------------|----------|-------------|
| 1          | Source   | Source      |
| 2          | Gate     | Gate        |
| 3          | Drain    | Drain       |

**TABLE 3-2: 3-LEAD SOT-89 PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|------------|----------|-------------|
| 1          | Gate     | Gate        |
| 2, 4       | Drain    | Drain       |
| 3          | Source   | Source      |

## 4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for DN3545.



**FIGURE 4-1:** Switching Waveforms and Test Circuit.

**TABLE 4-1: PRODUCT SUMMARY**

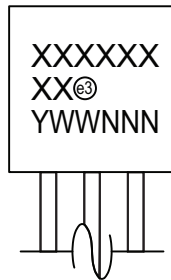
| $BV_{DSX}/BV_{DGX}$<br>(V) | $R_{DS(ON)}$<br>(Maximum)<br>( $\Omega$ ) | $I_{DSS}$<br>(Minimum)<br>(mA) |
|----------------------------|---|--------------------------------|
| 450                        | 20  | 200                            |

# DN3545

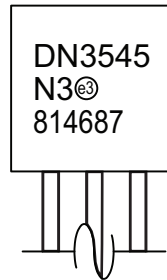
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

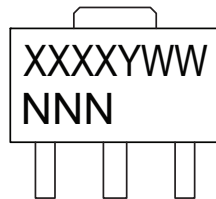
3-lead TO-92



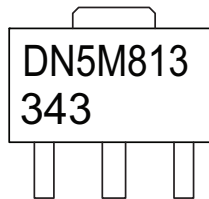
Example



3-lead TO-243AA



Example

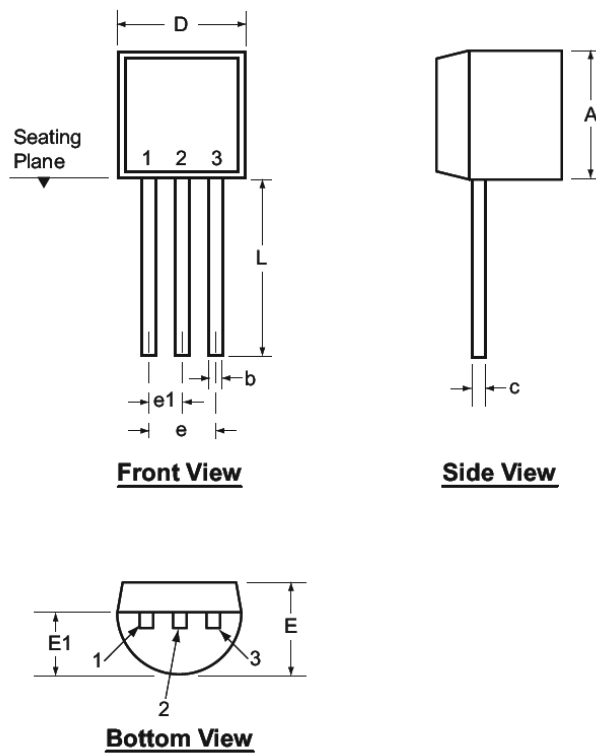


|                |        |  |
|----------------|--------|--|
| <b>Legend:</b> | XX...X | Product Code or Customer-specific information  |
|                | Y      | Year code (last digit of calendar year)  |
|                | YY     | Year code (last 2 digits of calendar year)   |
|                | WW     | Week code (week of January 1 is week '01')   |
|                | NNN    | Alphanumeric traceability code   |
|                | ⓔ3     | Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)   |
|                | *      | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.



## 3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

| Symbol                 | A   | b    | c                 | D                 | E    | E1   | e    | e1   | L    |       |
|------------------------|-----|------|-------------------|-------------------|------|------|------|------|------|-------|
| Dimensions<br>(inches) | MIN | .170 | .014 <sup>†</sup> | .014 <sup>†</sup> | .175 | .125 | .080 | .095 | .045 | .500  |
|                        | NOM | -    | -                 | -                 | -    | -    | -    | -    | -    | -     |
|                        | MAX | .210 | .022 <sup>†</sup> | .022 <sup>†</sup> | .205 | .165 | .105 | .105 | .055 | .610* |

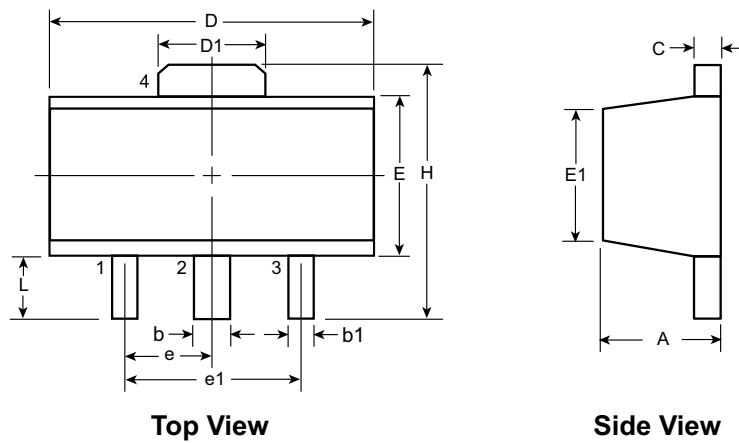
JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

## 3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

| Symbol             | A   | b    | b1   | C    | D    | D1   | E    | E1   | e                 | e1          | H           | L    |                   |   |
|--------------------|-----|------|------|------|------|------|------|------|-------------------|-------------|-------------|------|-------------------|---|
| Dimensions<br>(mm) | MIN | 1.40 | 0.44 | 0.36 | 0.35 | 4.40 | 1.62 | 2.29 | 2.00 <sup>†</sup> | 1.50<br>BSC | 3.00<br>BSC | 3.94 | 0.73 <sup>†</sup> |   |
|                    | NOM | -    | -    | -    | -    | -    | -    | -    | -                 |             |             | -    | -                 | - |
|                    | MAX | 1.60 | 0.56 | 0.48 | 0.44 | 4.60 | 1.83 | 2.60 | 2.29              |             |             | 4.25 | 1.20              |   |

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

<sup>†</sup> This dimension differs from the JEDEC drawing

Drawings not to scale.

## APPENDIX A: REVISION HISTORY

### Revision A (April 2018)

- Converted Supertex doc #DSFP-DN3545 to Microchip DS20005438A
- Added sections to comply with the standard Microchip format
- Changed the package marking format
- Removed the 3-lead TO-92 N3 P002, P003, P005, P013 and P014 media types
- Made minor text changes throughout the document

# DN3545

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u> | <u>XX</u>       | - | <u>X</u>                                   | - | <u>X</u>   |
|-----------------|-----------------|---|--|---|------------|
| Device          | Package Options |   | Environmental                              |   | Media Type |
| Device:         | DN3545          | = | N-Channel Depletion-Mode Vertical DMOS FET |   |            |
| Packages:       | N3              | = | 3-lead TO-92                               |   |            |
|                 | N8              | = | 3-lead SOT-89                              |   |            |
| Environmental:  | G               | = | Lead (Pb)-free/RoHS-compliant Package      |   |            |
| Media Types:    | (blank)         | = | 1000/Bag for an N3 Package                 |   |            |
|                 | (blank)         | = | 2000/Reel for an N8 Package                |   |            |

**Examples:**

a) DN3545N3-G: N-Channel Depletion-Mode Vertical DMOS FET, 3-lead TO-92, 1000/Bag

b) DN3545N8-G: N-Channel Depletion-Mode Vertical DMOS FET, 3-lead SOT-89, 2000/Reel

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