



# N-Channel Enhancement-Mode Vertical DMOS FET

## Features

- ▶ Low threshold (1.6V max.)
- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

## Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

## General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex’s well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex’s vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Ordering Information

Part Number	Package Option	Packing
TN0104N3-G	TO-92	1000/Bag
TN0104N3-G P002	TO-92	2000/Reel
TN0104N3-G P003		
TN0104N3-G P005		
TN0104N3-G P013		
TN0104N3-G P014		
TN0104N8-G	TO-243AA (SOT-89)	2000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package.  
 Contact factory for Wafer / Die availability.  
 Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

## Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

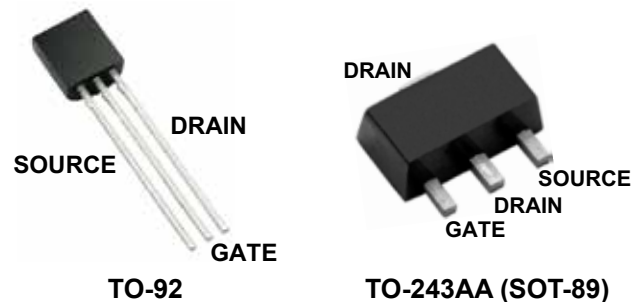
## Typical Thermal Resistance

Package	$\theta_{ja}$
TO-92	$132^{\circ}C/W$
TO-243AA (SOT-89)	$133^{\circ}C/W$

## Product Summary

$BV_{DSX}/BV_{DGX}$	$R_{DS(ON)}$ (max)	$I_{DSS}$ (min)
40V	$1.8\Omega$	2.0A

## Pin Configuration



## Product Marking



YY = Year Sealed  
 WW = Week Sealed  
 \_\_\_\_\_ = “Green” Packaging

Package may or may not include the following marks: Si or **TO-92**



W = Code for Week Sealed  
 \_\_\_\_\_ = “Green” Packaging

Package may or may not include the following marks: Si or **TO-243AA (SOT-89)**

## Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup>	$I_D$ (pulsed)	Power Dissipation @ $T_c = 25^\circ\text{C}$	$I_{DR}$ <sup>†</sup>	$I_{DRM}$
TO-92	450mA	2.40A	1.0W	450mA	2.40A
TO-243AA (SOT-89)	630mA	2.90A	1.6W <sup>‡</sup>	630mA	2.90A

### Notes:

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

<sup>‡</sup>  $T_A = 25^\circ\text{C}$ . Mounted on FR5 Board, 25mm x 25mm x 1.57mm. Significant  $P_D$  increase possible on ceramic substrate.

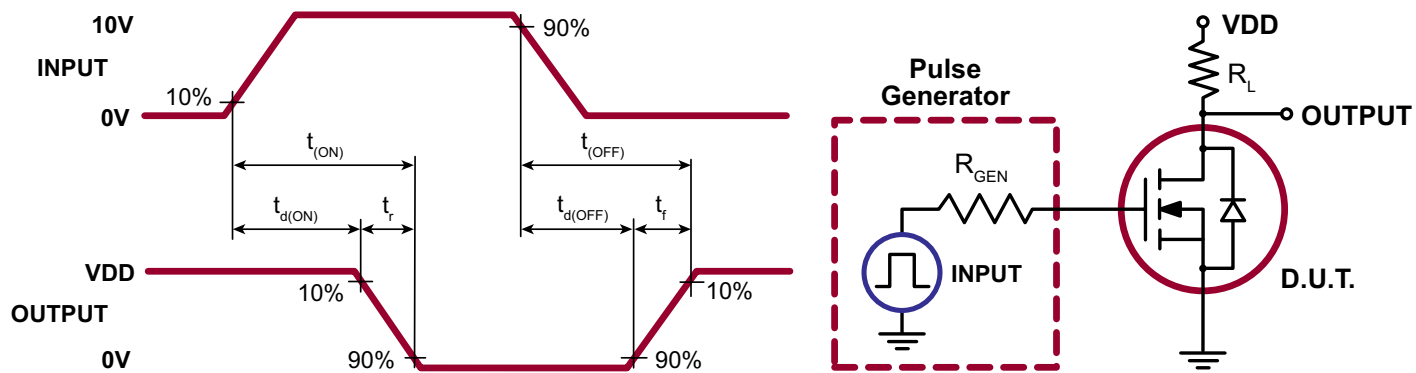
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions		
$BV_{DSS}$	Drain-to-source breakdown voltage	40	-	-	V	$V_{GS} = 0V, I_D = 1.0mA$		
$V_{GS(th)}$	Gate threshold voltage	0.6	-	1.6	V	$V_{GS} = V_{DS}, I_D = 500\mu A$		
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.8	-5.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0mA$		
$I_{GSS}$	Gate body leakage	-	0.1	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$		
$I_{DSS}$	Zero gate voltage drain current	-	-	1.0	$\mu A$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$		
		-	-	100		$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$		
$I_{D(ON)}$	On-state drain current	-	0.35	-	A	$V_{GS} = 3.0V, V_{DS} = 20V$		
		0.5	1.1	-		$V_{GS} = 5.0V, V_{DS} = 20V$		
		2.0	2.6	-		$V_{GS} = 10V, V_{DS} = 20V$		
$R_{DS(ON)}$	Static drain-to-source on-state resistance	Both packages		-	$\Omega$	$V_{GS} = 3.0V, I_D = 50mA$		
		-	2.3	2.5		$V_{GS} = 5.0V, I_D = 250mA$		
		TO-92		-		1.5	1.8	$V_{GS} = 10V, I_D = 1.0A$
		TO-243AA		-		-	2.0	
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.7	1.0	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 1.0A$		
$G_{FS}$	Forward transductance	340	450	-	mmho	$V_{DS} = 20V, I_D = 500mA$		
$C_{ISS}$	Input capacitance	-	-	70	pF	$V_{GS} = 0V,$ $V_{DS} = 20V,$ $f = 1.0MHz$		
$C_{OSS}$	Common source output capacitance	-	-	50				
$C_{RSS}$	Reverse transfer capacitance	-	-	15				
$t_{d(ON)}$	Turn-on delay time	-	3.0	5.0	ns	$V_{DD} = 20V,$ $I_D = 1.0A,$ $R_{GEN} = 25\Omega$		
$t_r$	Rise time	-	7.0	8.0				
$t_{d(OFF)}$	Turn-off delay time	-	6.0	9.0				
$t_f$	Fall time	-	5.0	8.0				
$V_{SD}$	Diode forward voltage drop	TO-92		-	V	$V_{GS} = 0V, I_{SD} = 1.0A$		
		TO-243AA		-		-	2.0	$V_{GS} = 0V, I_{SD} = 0.5A$
$t_{rr}$	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = 1.0A$		

### Notes:

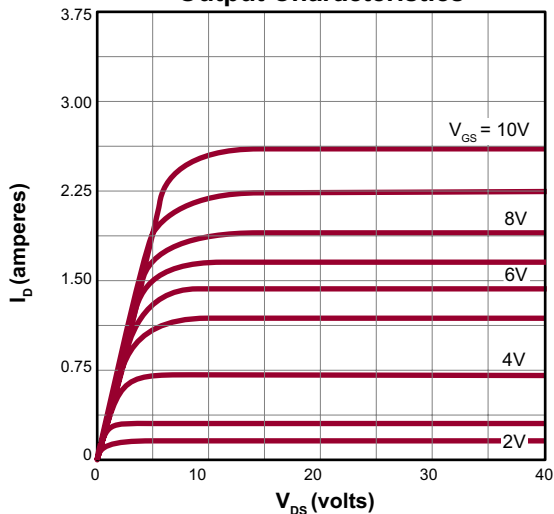
- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu s$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

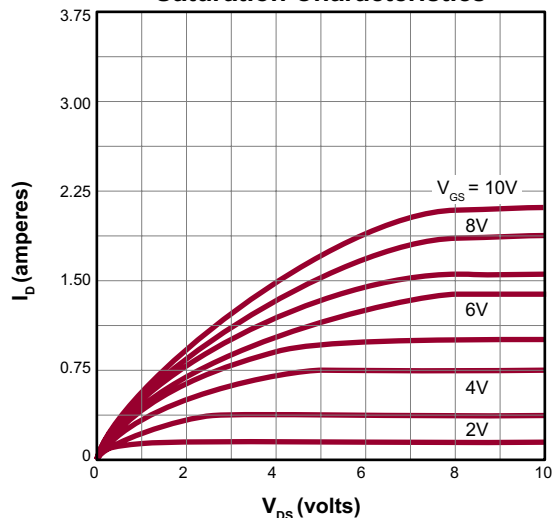


# Typical Performance Curves

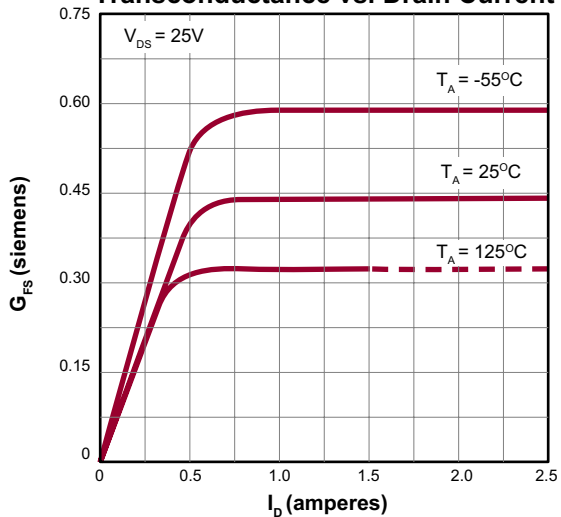
**Output Characteristics**



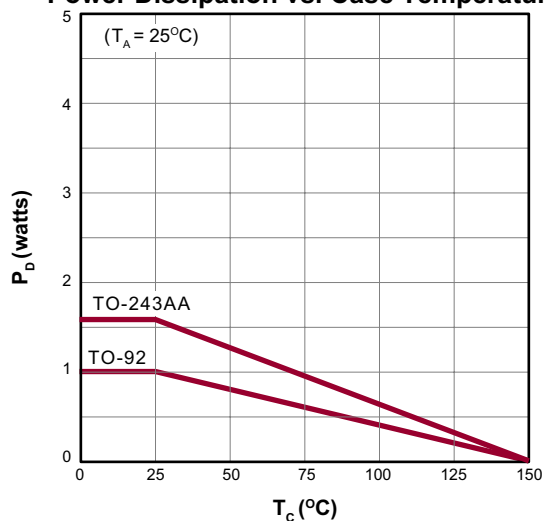
**Saturation Characteristics**



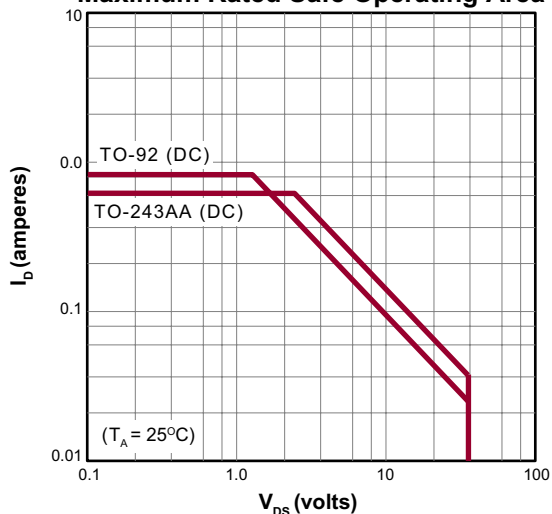
**Transconductance vs. Drain Current**



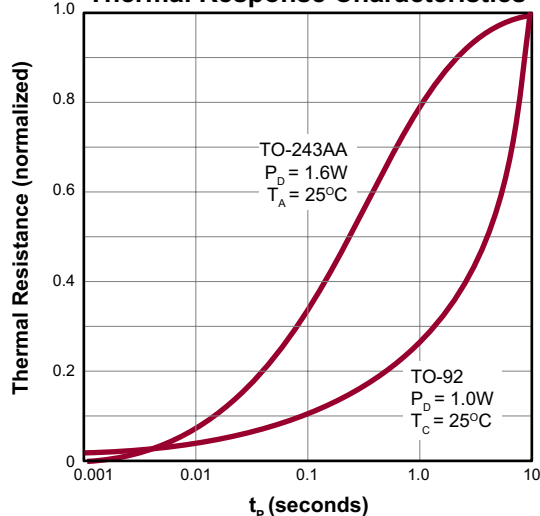
**Power Dissipation vs. Case Temperature**



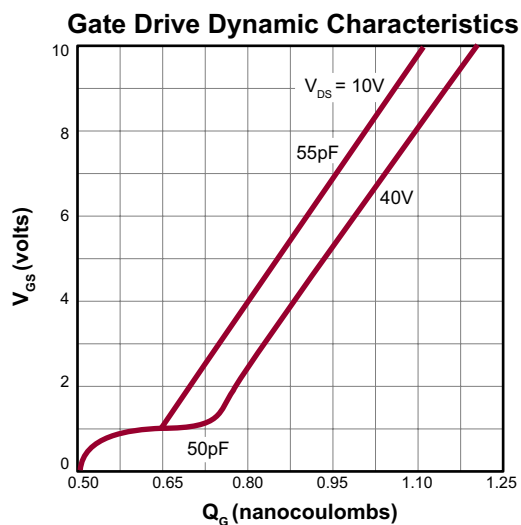
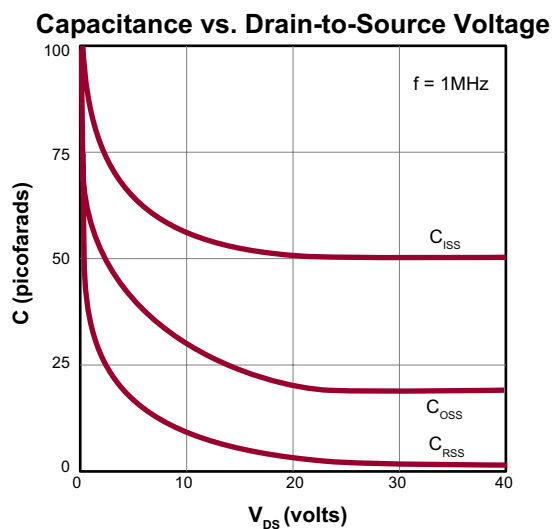
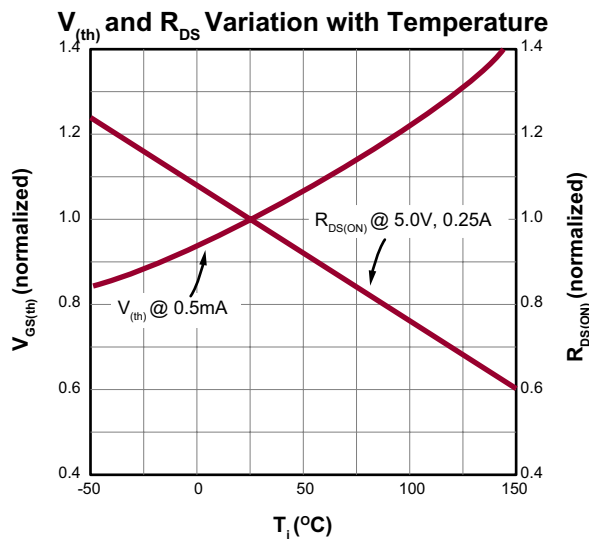
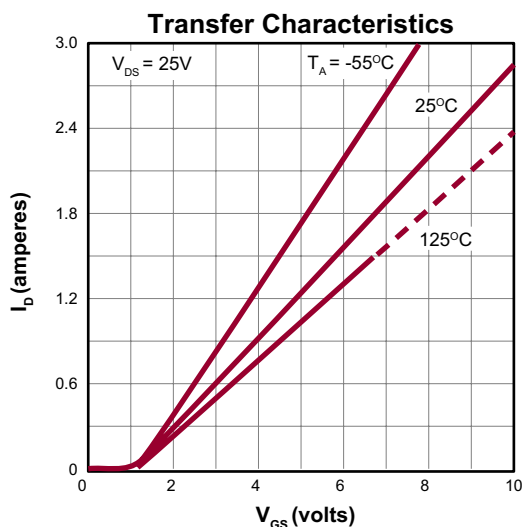
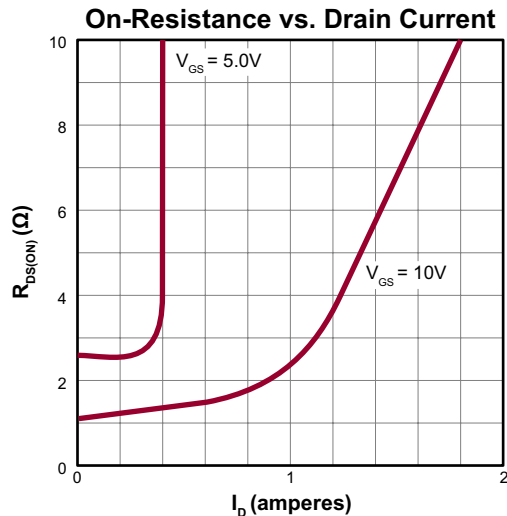
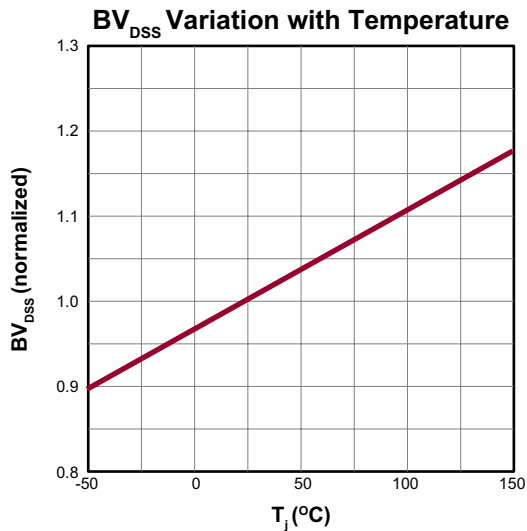
**Maximum Rated Safe Operating Area**



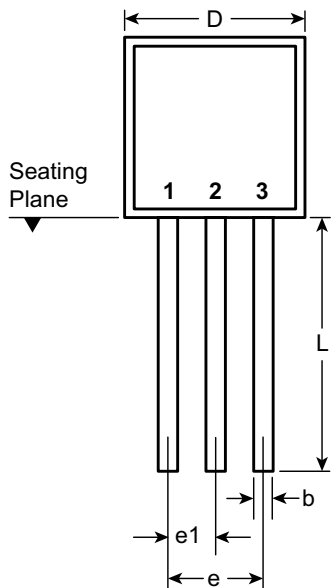
**Thermal Response Characteristics**



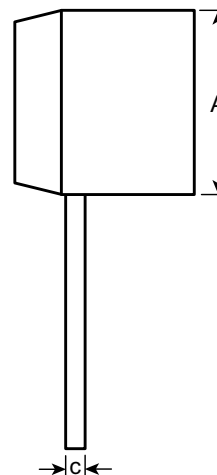
Typical Performance Curves (cont.)



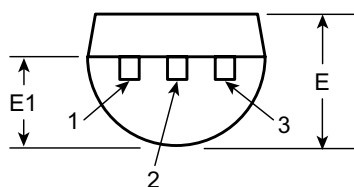
### 3-Lead TO-92 Package Outline (N3)



**Front View**



**Side View**



**Bottom View**

Symbol	A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.610*

JEDEC Registration TO-92.

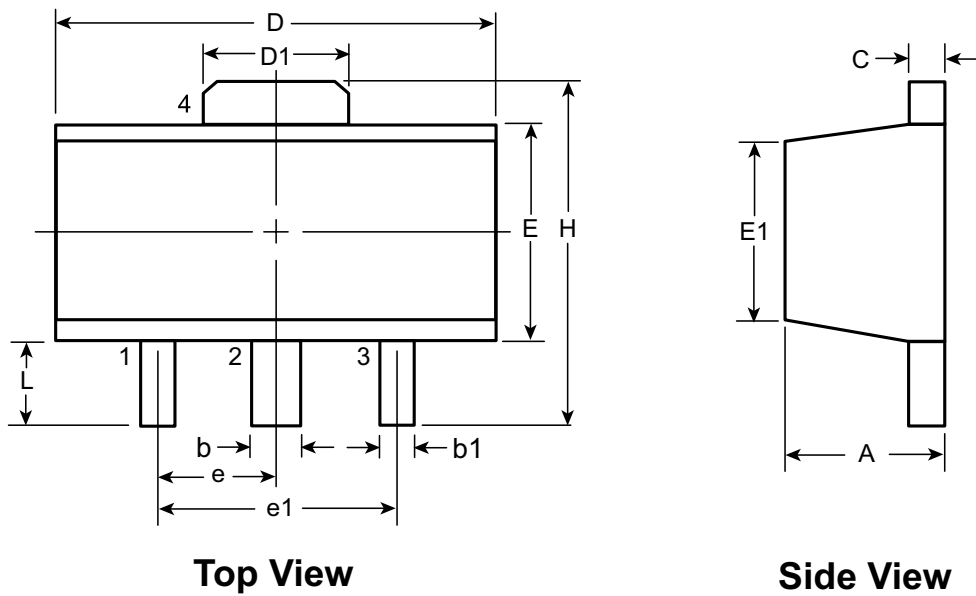
\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc.#:** DSPD-3TO92N3, Version E041009.

### 3-Lead TO-243AA (SOT-89) Package Outline (N8)



**Top View**

**Side View**

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†		
	NOM	-	-	-	-	-	-	-	-			-	-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20		

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

† This dimension differs from the JEDEC drawing

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version F111010.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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