N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- High input impedance and high gain

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Part Number	Package Option	Packing
VN10KN3-G	TO-92	1000/Bag
VN10KN3-G P002		
VN10KN3-G P003		
VN10KN3-G P005	TO-92	2000/Reel
VN10KN3-G P013		
VN10KN3-G P014		

-G denotes a lead (Pb)-free / RoHS compliant package.
Contact factory for Wafer / Die availablity.
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±30V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

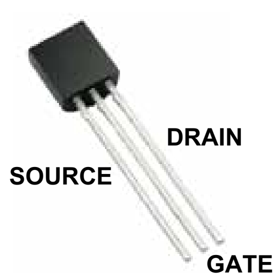
Typical Thermal Resistance

Package	θ_{ja}
TO-92	132°C/W

Product Summary

BV_{DSS}/BV_{DGS}	$R_{DS(ON)}$ (max)	I_{DSS} (min)
60V	5.0Ω	750mA

Pin Configuration



TO-92

Product Marking

SiVN
1 0 K
YYWW

YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation @T_C = 25°C	I_{DR}†	I_{DRM}
TO-92	310mA	1.0A	1.0W	310mA	1.0A

Notes:

† *I_D (continuous) is limited by max rated T_j . (VN0106N3 can be used if an I_D (continuous) of 500mA is needed.)*

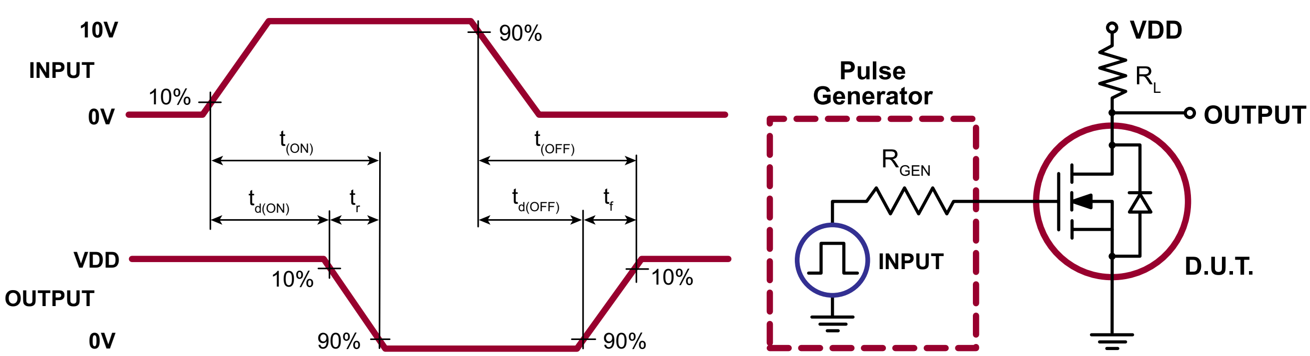
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	60	-	-	V	V_{GS} = 0V, I_D = 100µA
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.5	V	V_{GS} = V_{DS}, I_D= 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.8	-	mV/°C	V_{GS} = V_{DS}, I_D= 1.0mA
I_{GSS}	Gate body leakage	-	-	100	nA	V_{GS} = 15V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{GS} = 0V, V_{DS} = 45V
		-	-	500		V_{GS} = 0V, V_{DS} = 45V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	0.75	-	-	A	V_{GS} = 10V, V_{DS} = 10V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	7.5	Ω	V_{GS} = 5.0V, I_D = 200mA
		-	-	5.0		V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.7	-	%/°C	V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward transductance	100	-	-	mmho	V_{DS} = 10V, I_D = 500mA
C_{ISS}	Input capacitance	-	48	60	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	16	25		
C_{RSS}	Reverse transfer capacitance	-	2.0	5.0		
$t_{(ON)}$	Turn-on time	-	-	10	ns	V_{DD} = 15V, I_D = 600mA, R_{GEN} = 25Ω
$t_{(OFF)}$	Turn-off time	-	-	10		
V_{SD}	Diode forward voltage drop	-	0.8	-	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rr}	Reverse recovery time	-	160	-	ns	V_{GS} = 0V, I_{SD} = 500mA

Notes:

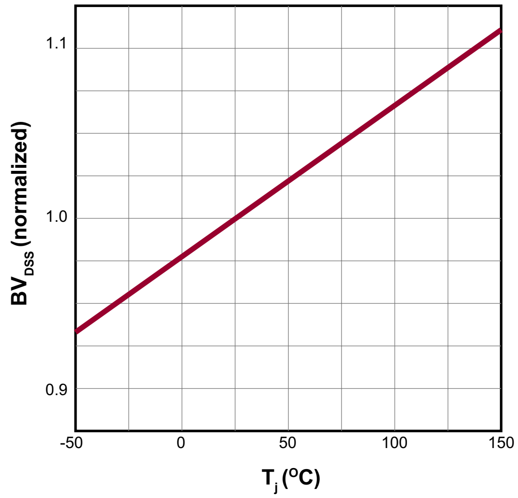
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

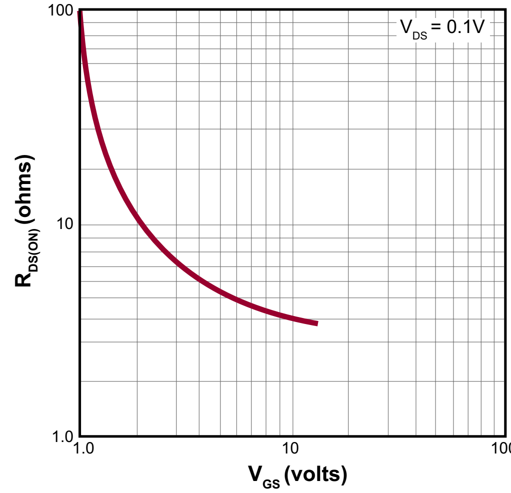


Typical Performance Curves

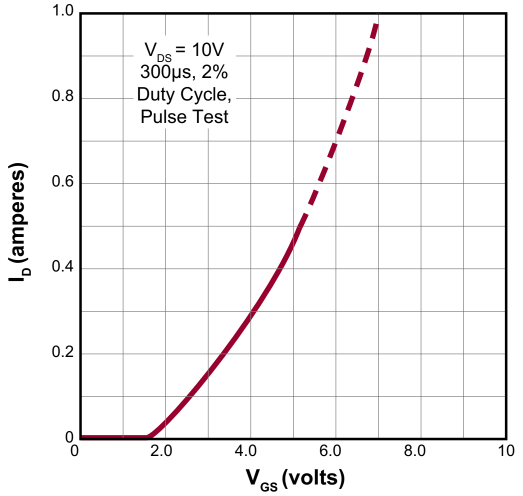
BV$_{DSS}$ Variation with Temperature



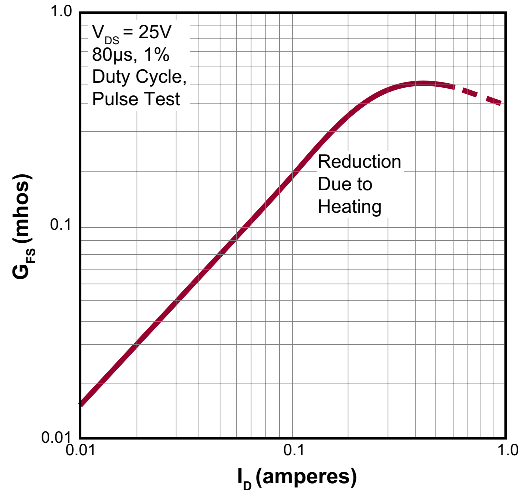
On-Resistance vs. Gate-to-Source Voltage



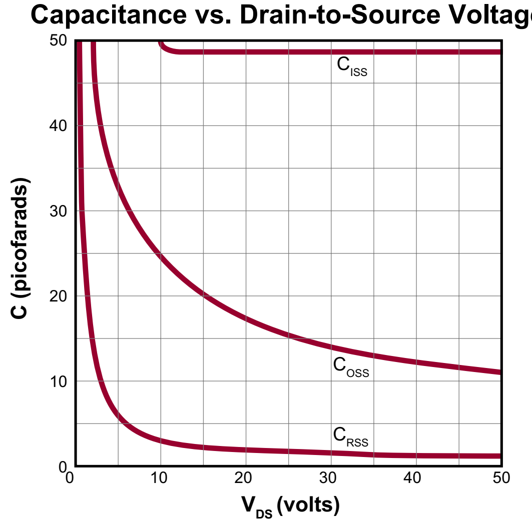
Transfer Characteristics



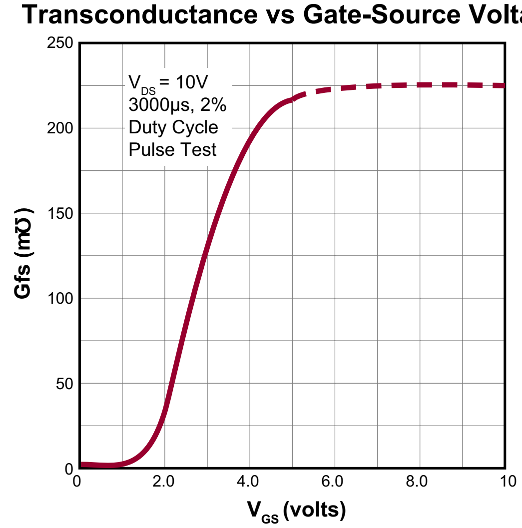
Output Conductance vs Drain Current



Capacitance vs. Drain-to-Source Voltage

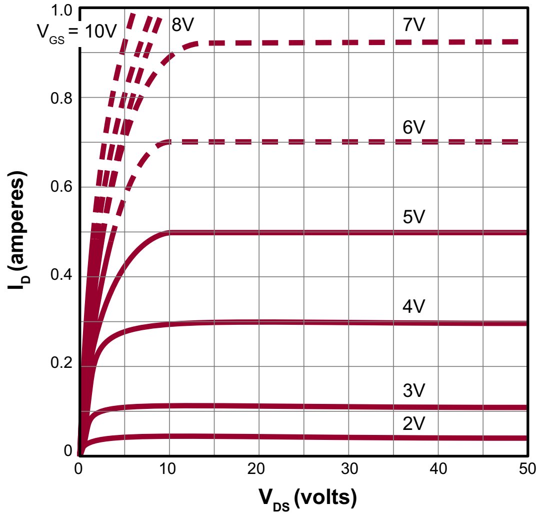


Transconductance vs Gate-Source Voltage

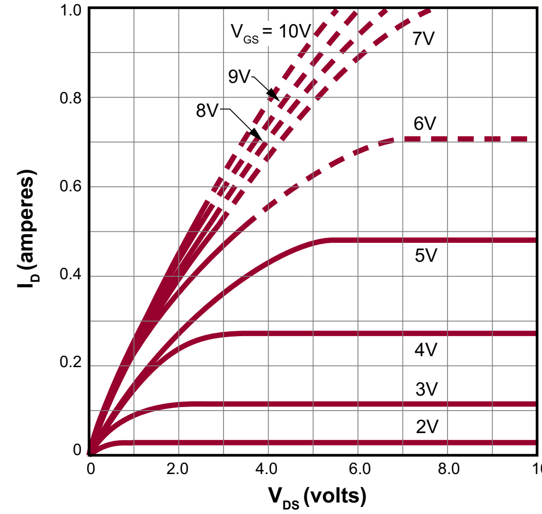


Typical Performance Curves *(cont.)*

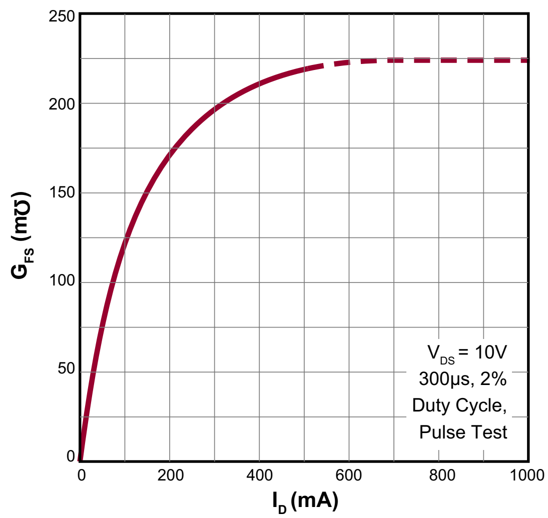
Output Characteristics



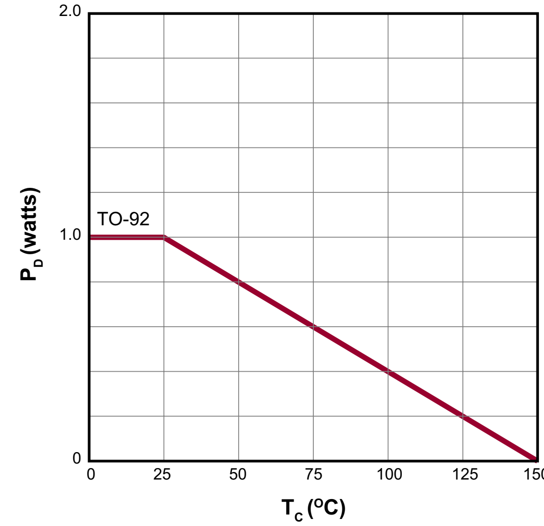
Saturation Characteristics



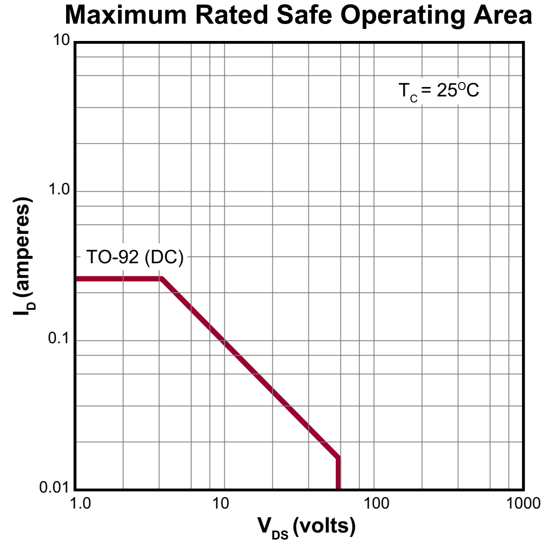
Transconductance vs. Drain Current



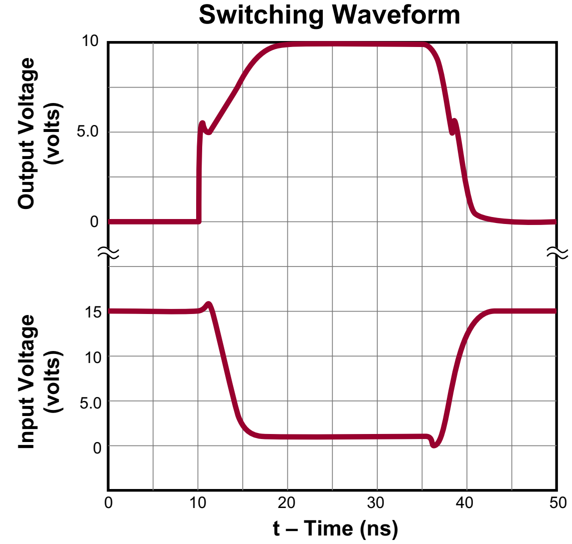
Power Dissipation vs. Case Temperature



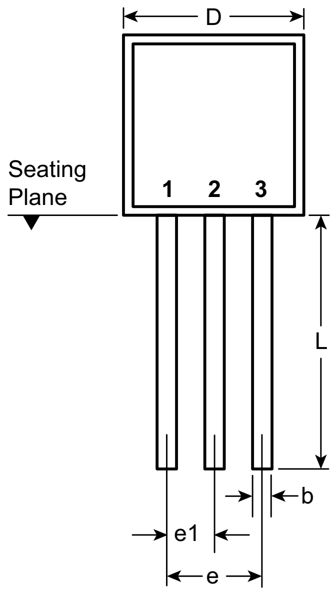
Maximum Rated Safe Operating Area



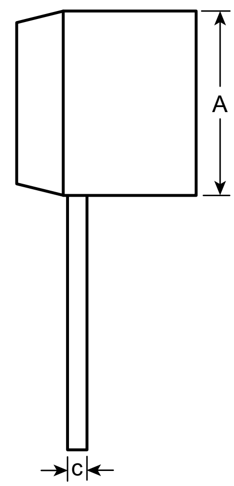
Switching Waveform



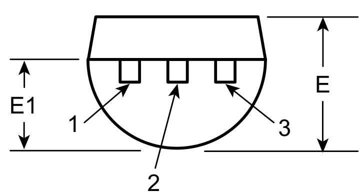
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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