BUK7618-55

N-channel TrenchMOS standard level FET

Rev. 2 — 26 April 2011 Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Electrostatically robust due to integrated protection diodes
- Low conduction losses due to low on-state resistance

1.3 Applications

- Automotive and general purpose power switching

1.4 Quick reference data

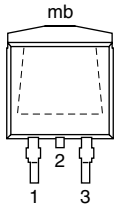
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	55	V
I_D	drain current	T_{mb} = 25 °C	-	-	57	A
P_{tot}	total power dissipation		-	-	125	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C	-	15	18	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 50 A; $V_{sup} \leq 25$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	125	mJ

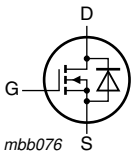
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		



SOT404 (D2PAK)



3. Ordering information

Table 3. Ordering information

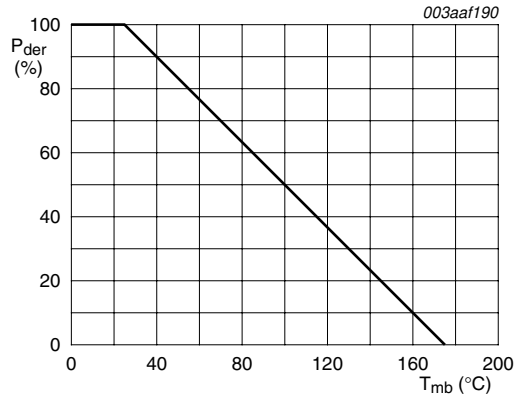
Type number	Package		
	Name	Description	Version
BUK7618-55	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

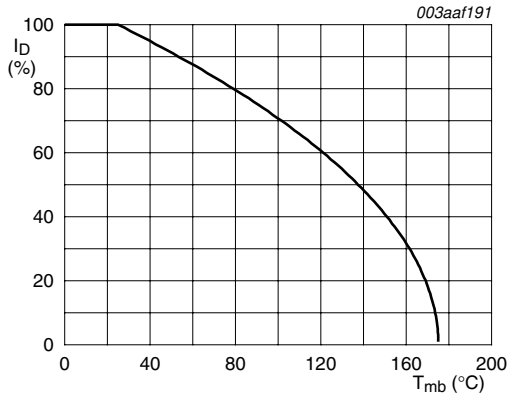
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	55	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
V_{GS}	gate-source voltage		-16	16	V
I_D	drain current	T_{mb} = 25 °C	-	57	A
		T_{mb} = 100 °C	-	40	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed	-	228	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	57	A
I_{SM}	peak source current	pulsed; T_{mb} = 25 °C	-	200	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 50 A; $V_{sup} \leq 25$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	125	mJ
Electrostatic discharge					
V_{esd}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ; (all pins)	-	2	kV



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

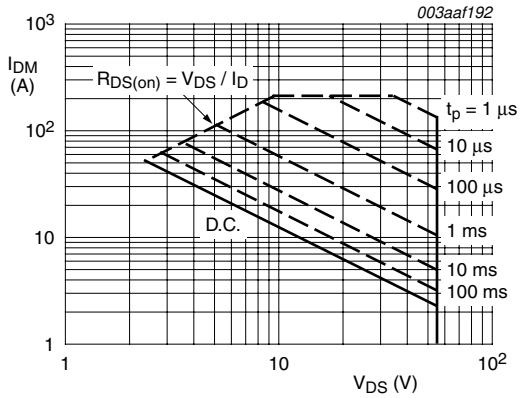
Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

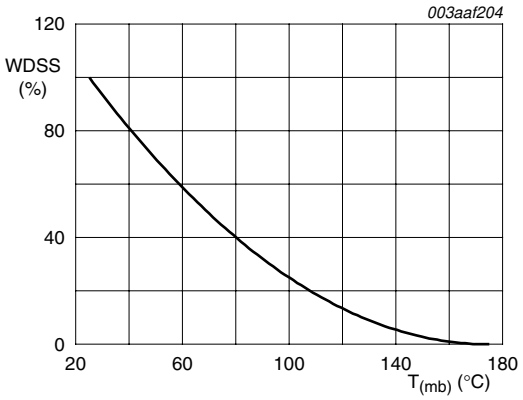
$V_{GS} \geq 5$ V

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



I_D = 75 A

Fig 4. Normalised drain-source avalanche energy as a function of mounting-base temperature.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	1.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board	-	50	-	K/W

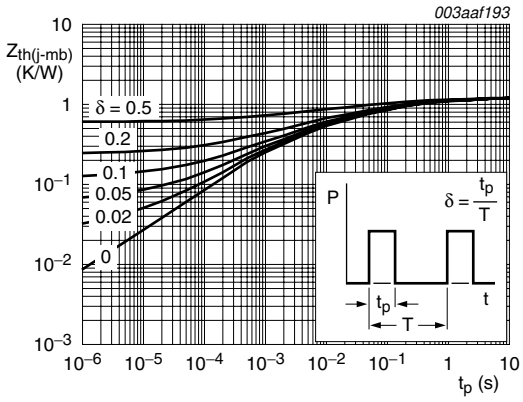
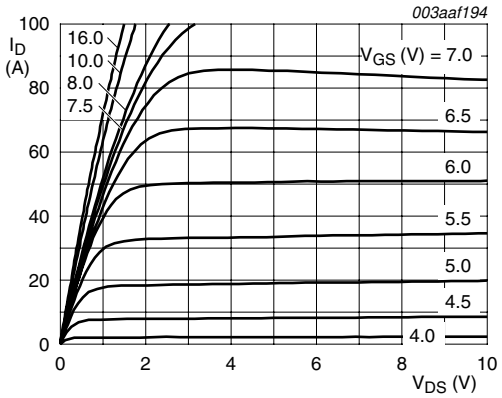


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

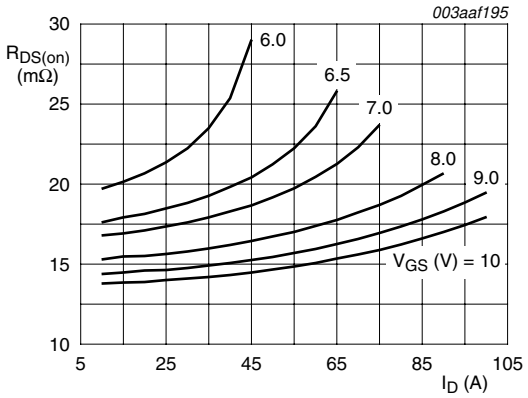
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	55	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 55 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
		V_{DS} = 55 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	10	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	0.02	1	µA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C	-	0.02	1	µA
		V_{GS} = 10 V; V_{DS} = 0 V; T_j = 175 °C	-	-	20	µA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 175 °C	-	-	20	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C	-	-	38	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C	-	15	18	mΩ
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 V; T_j = 25 °C; I_G = 1 mA	16	-	-	V
		V_{DS} = 0 V; T_j = 25 °C; I_G = -1 mA	16	-	-	V
Dynamic characteristics						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C	-	1500	2000	pF
C_{oss}	output capacitance		-	370	470	pF
C_{rss}	reverse transfer capacitance		-	170	250	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; I_D = 25 A; T_j = 25 °C	-	15	22	ns
t_r	rise time		-	30	60	ns
$t_{d(off)}$	turn-off delay time		-	35	50	ns
t_f	fall time		-	25	38	ns
L_D	internal drain inductance	measured from upper edge of drain mounting base to centre of die; T_j = 25 °C	-	2.5	-	nH
L_S	internal source inductance	measured from source lead soldering point to source bond pad; T_j = 25 °C	-	7.5	-	nH
g_{fs}	transfer conductance	V_{DS} = 25 V; I_D = 25 A; T_j = 25 °C	6	30	-	S
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 50 A; V_{GS} = 0 V; T_j = 25 °C	-	1	-	V
		I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C	-	0.95	1.2	V
t_{rr}	reverse recovery time	I_S = 50 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	48	-	ns
Q_r	recovered charge		-	0.1	-	µC



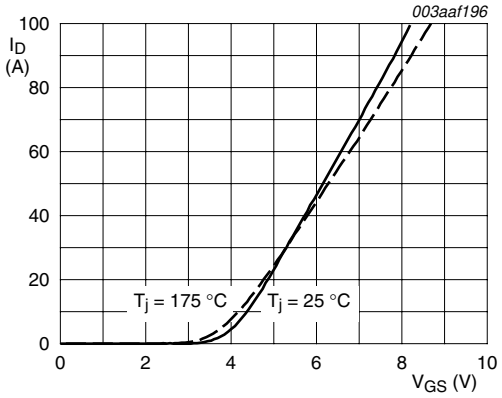
T_j = 25 °C

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



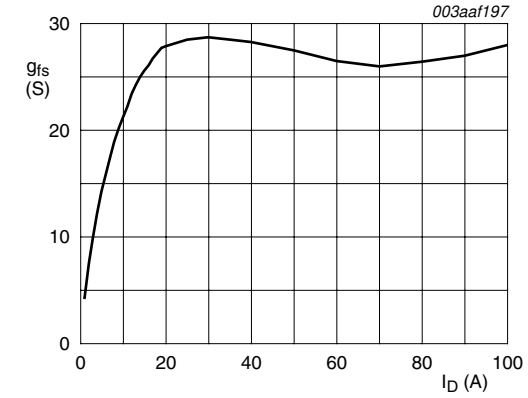
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



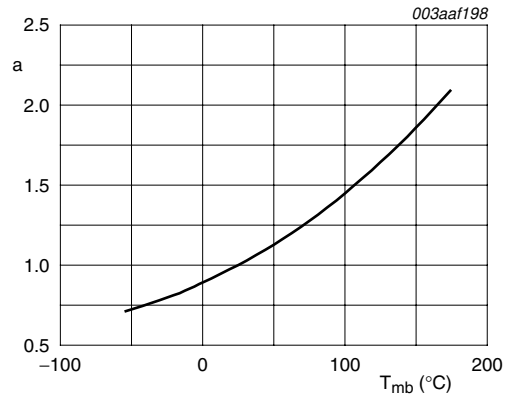
$V_{DS} > I_D \times R_{DSon}$

Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



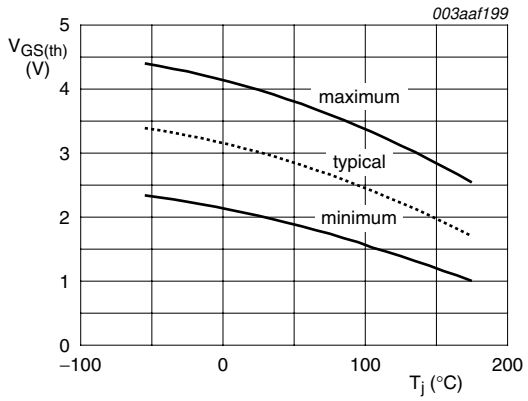
$V_{DS} > I_D \times R_{DSon}$

Fig 9. Forward transconductance as a function of drain current; typical values



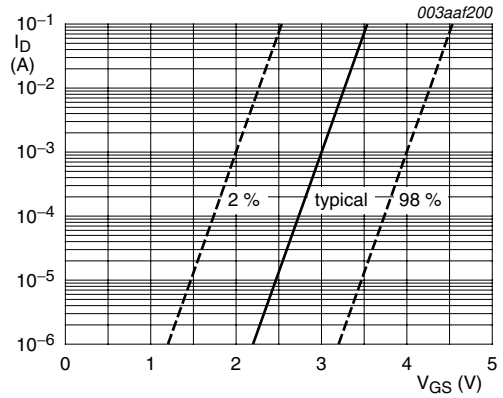
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



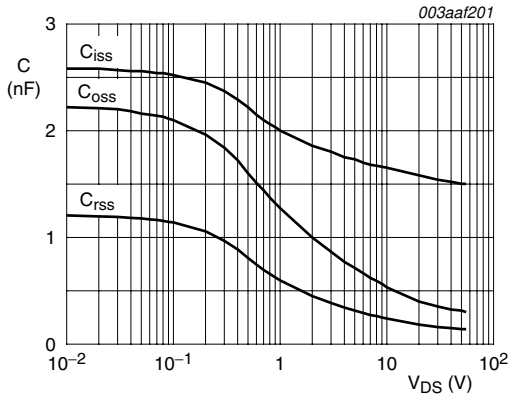
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



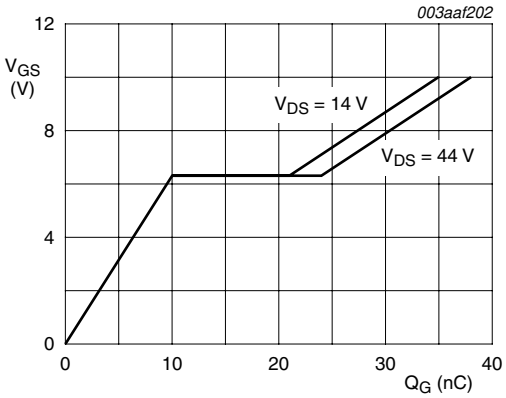
T_j = 25 °C; V_{DS} = V_{GS}

Fig 12. Sub-threshold drain current as a function of gate-source voltage



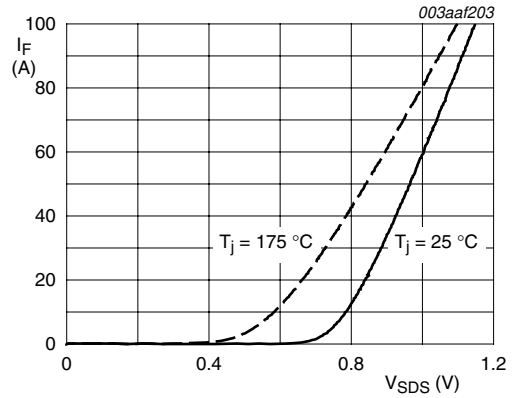
V_{GS} = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



T_j = 25 °C; I_D = 50 A

Fig 14. Gate-source voltage as a function of gate charge; typical values

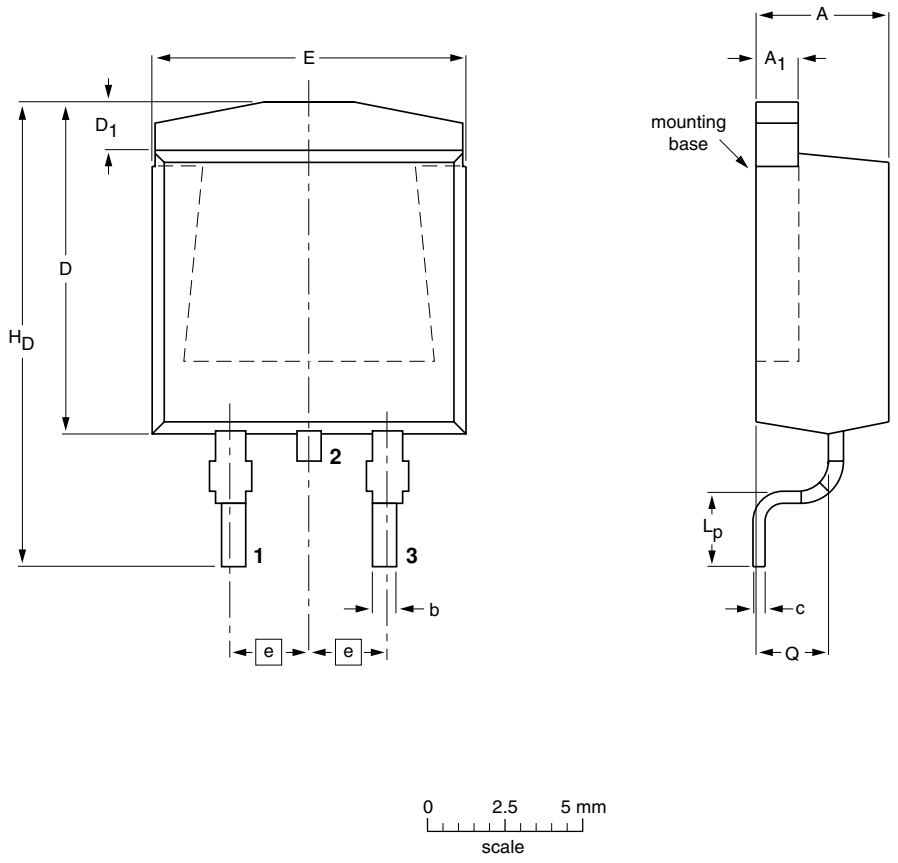


V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7618-55 v.2	20110426	Product data sheet	-	BUK7618-55_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP. • Legal texts have been adapted to the new company name where appropriate.			
BUK7618-55_1	19980401	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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11. Contents

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