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Team Nexperia

## **BUK9515-100A**



# N-channel TrenchMOS logic level FET Rev. 3 — 19 April 2011

Product data sheet

#### **Product profile** 1.

## 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

#### 1.2 Features and benefits

■ AEC Q101 compliant

Low conduction losses due to low on-state resistance

## 1.3 Applications

Automotive and general purpose power switching

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	100	V	
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C	-	-	75	Α	
P <sub>tot</sub>	total power dissipation		-	-	230	W	
T <sub>j</sub>	junction temperature		-55	-	175	°C	
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$	-	11.5	14.4	mΩ	
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$	-	12	15	mΩ	
Avalanch	Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\begin{split} &I_D = 35 \text{ A; V}_{\text{sup}} \leq 25 \text{ V;} \\ &R_{\text{GS}} = 50 \Omega\text{; V}_{\text{GS}} = 5 \text{ V;} \\ &T_{j(\text{init})} = 25 ^{\circ}\text{C; unclamped} \end{split}$	-	-	120	mJ	



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain	mb	D
3	S	source		$G \longrightarrow A$
mb	D	mounting base; connected to drain		mbb076 S
			SOT78A (TO-220AB)	)

## 3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK9515-100A	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78A		

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-10	10	V
$I_D$	drain current	T <sub>mb</sub> = 25 °C	-	75	Α
		T <sub>mb</sub> = 100 °C	-	53	Α
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; pulsed	-	313	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C	-	230	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
$V_{GSM}$	peak gate-source voltage	pulsed; t <sub>p</sub> ≤ 50 μs	-15	15	V
Source-drain	diode				
Is	source current	T <sub>mb</sub> = 25 °C	-	75	Α
I <sub>SM</sub>	peak source current	pulsed; T <sub>mb</sub> = 25 °C	-	313	Α
Avalanche ru	iggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 35 A; $V_{sup} \le$ 25 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	120	mJ

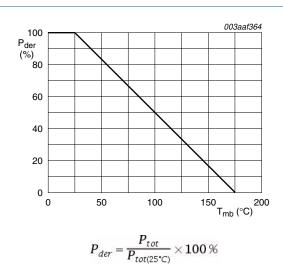


Fig 1. Normalized total power dissipation as a function of mounting base temperature

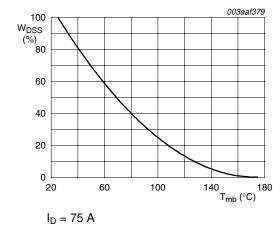
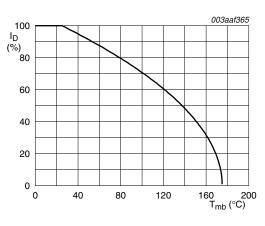


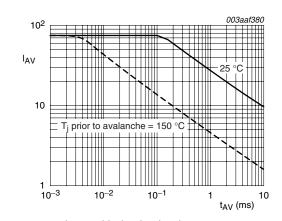
Fig 3. Normalised drain-source non-repetitive avalanche energy as a function of mounting-base temperature



$$I_{\textit{der}} = \frac{I_{\textit{D}}}{I_{\textit{D(25°C)}}} \times 100\,\%$$

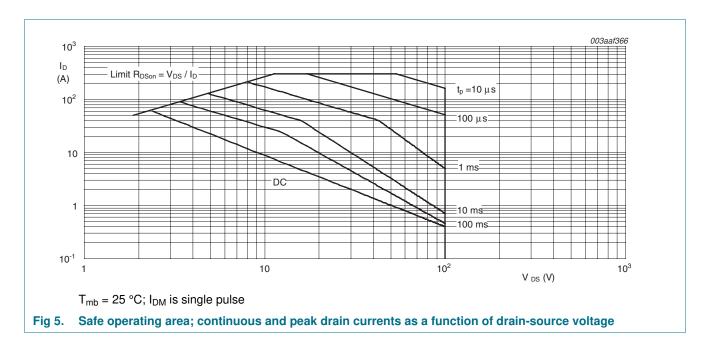
 $V_{GS} \ge 5 \text{ V}$ 

Fig 2. Normalized continuous drain current as a function of mounting base temperature



unclamped inductive load

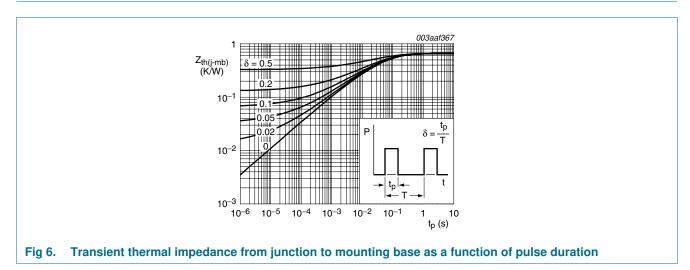
Fig 4. Single-shot avalanche rating; avalanche current as a function of avalanche period



## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.65	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	-	60	-	K/W



## 6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	100	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	89	-	-	V
V <sub>GS(th)</sub>	gate-source threshold	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1	1.5	2	V
	voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C}$	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μΑ
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		$V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
$R_{DSon}$	drain-source on-state	$V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C	-	-	16	mΩ
	resistance	$V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 175 °C	-	-	40.5	mΩ
		$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C	-	11.5	14.4	mΩ
		$V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 25 °C	-	12	15	mΩ
Dynamic	characteristics					
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	6500	8600	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C	-	550	660	pF
C <sub>rss</sub>	reverse transfer capacitance		-	325	400	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 30 V; $R_L$ = 1.2 $\Omega$ ; $V_{GS}$ = 5 V;	-	45	65	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 °C$	-	130	195	ns
t <sub>d(off)</sub>	turn-off delay time		-	400	560	ns
t <sub>f</sub>	fall time		-	130	190	ns
L <sub>D</sub>	internal drain inductance	measured from contact screw on mounting base to centre of die; $T_j = 25  ^{\circ}\text{C}$	-	3.5	-	nΗ
		measured from drain lead 6 mm from package to centre of die; $T_j = 25  ^{\circ}\text{C}$	-	4.5	-	nΗ
Ls	internal source inductance	measured from source lead to source bond pad; $T_j = 25$ °C	-	7.5	-	nΗ
Source-di	rain diode					
V <sub>SD</sub>	source-drain voltage	$I_S = 75 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	1.1	-	V
		$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 75 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	60	-	ns
Q <sub>r</sub>	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	0.24	-	μC

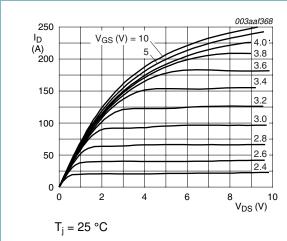


Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values

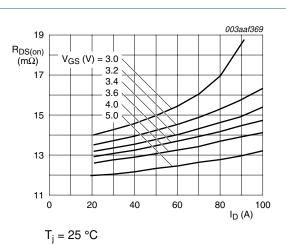


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

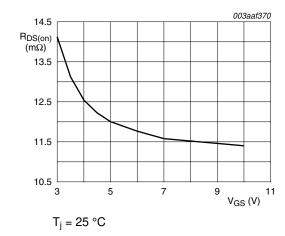


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

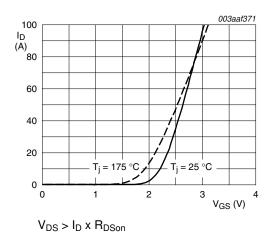


Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

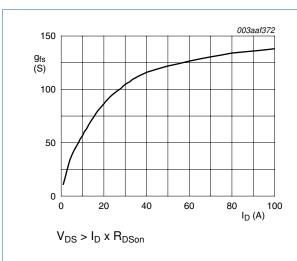
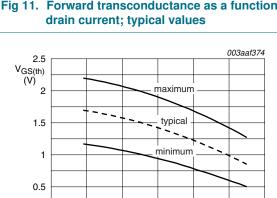


Fig 11. Forward transconductance as a function of drain current; typical values



 $I_D = 1 \text{ mA}; V_{DS} = V_{GS}$ 

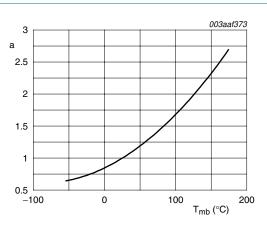
-100

Fig 13. Gate-source threshold voltage as a function of junction temperature

100

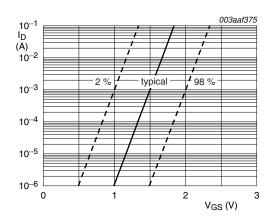
T<sub>j</sub> (°C)

200



 $I_D = 25 \text{ A}; V_{GS} = 5 \text{ V}$ 

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



 $T_i = 25 \, ^{\circ}C; \, V_{DS} = V_{GS}$ 

Fig 14. Sub-threshold drain current as a function of gate-source voltage

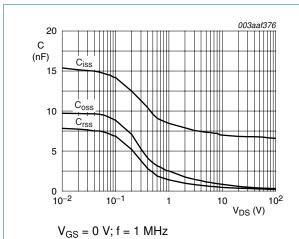
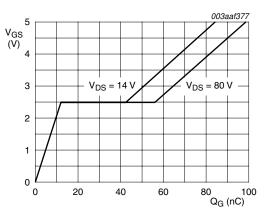
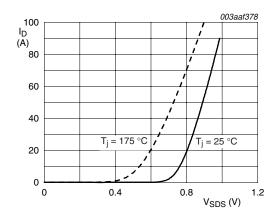


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $T_i = 25 \, ^{\circ}C; I_D = 25 \, A$ 

Fig 16. Gate-source voltage as a function of gate charge; typical values



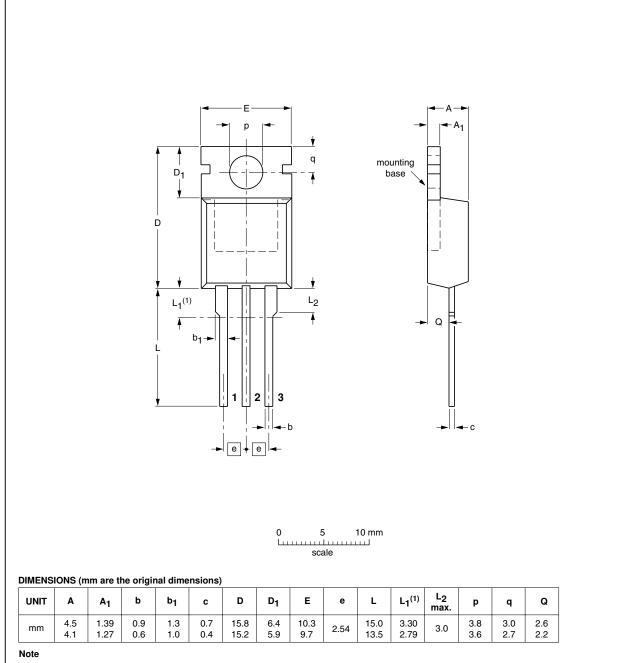
 $V_{GS} = 0 V$ 

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

## 7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78A



1. Terminals in this zone are not tinned.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	1330E DATE
SOT78A		3-lead TO-220AB	SC-46		<del>03-01-22</del> 05-03-14

Fig 18. Package outline SOT78A (TO-220AB)

BUK9515-100A

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## 8. Revision history

## Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9515-100A v.3	20110419	Product data sheet	-	BUK9515_9615-100A_2
Modifications:		t of this data sheet has b of NXP Semiconductors	•	comply with the new identity
	<ul> <li>Legal texts</li> </ul>	s have been adapted to t	he new company i	name where appropriate.
	<ul> <li>Type num</li> </ul>	ber BUK9515-100A sepa	arated from data sl	neet BUK9515_9615-100A_2.
BUK9515_9615-100A_2	19991101	Product specification	-	-

## 9. Legal information

#### 9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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#### N-channel TrenchMOS logic level FET

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