PSMN041-80YL

N-channel 80 V 41 mΩ logic level MOSFET in LFPAK56

1 May 2013 — Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in LFPAK56 package. This product has been designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive
- LFPAK56 package is footprint compatible with other Power-SO8 types
- Qualified to 175 °C

3. Applications

- DC-to-DC converters
- Load switch
- TV power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	80	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; Fig. 1		-	-	25	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 2		-	-	64	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 5$ A; $T_j = 25$ °C; Fig. 12		-	32.8	41	mΩ
		$V_{GS} = 10$ V; $I_D = 5$ A; $T_j = 175$ °C; Fig. 13; Fig. 12		-	-	103	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 5$ A; $V_{DS} = 64$ V; $T_j = 25$ °C; Fig. 14; Fig. 15		-	4.3	-	nC
$Q_{G(tot)}$	total gate charge			-	21.9	-	nC

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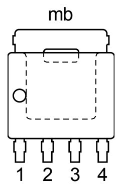
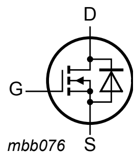
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 25 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; unclamped; Fig. 3		-	-	23.9	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN041-80YL	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN041-80YL	04180

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C		-	80	V
V_{DGR}	drain-gate voltage	T_j ≥ 25 °C; T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	80	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 1		-	18	A

Symbol	Parameter	Conditions		Min	Max	Unit
		V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 1		-	25	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 4		-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	64	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	54	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	100	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 25 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; unclamped; Fig. 3		-	23.9	mJ

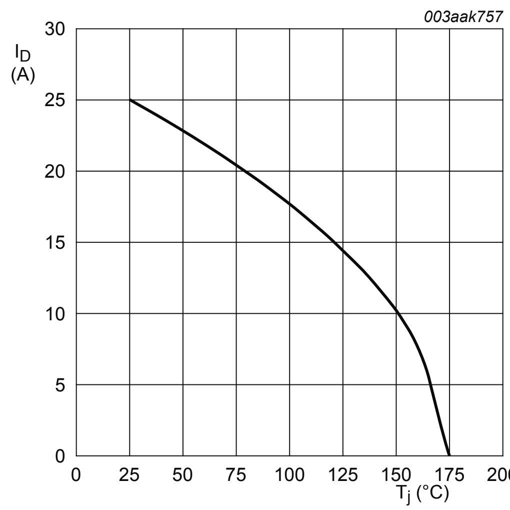


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

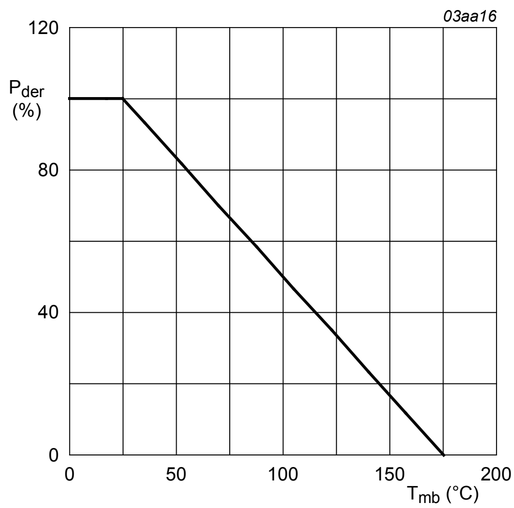


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\,\%$$

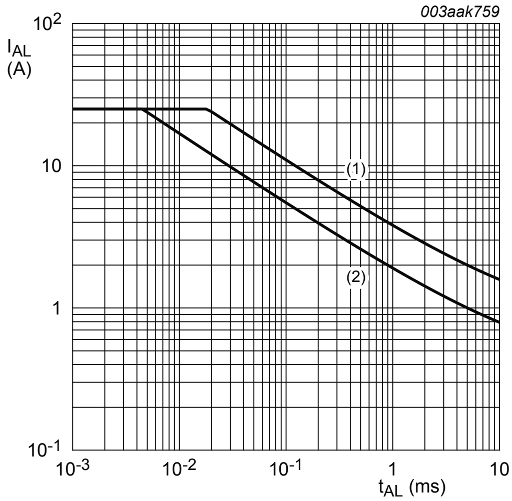


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 100°C$

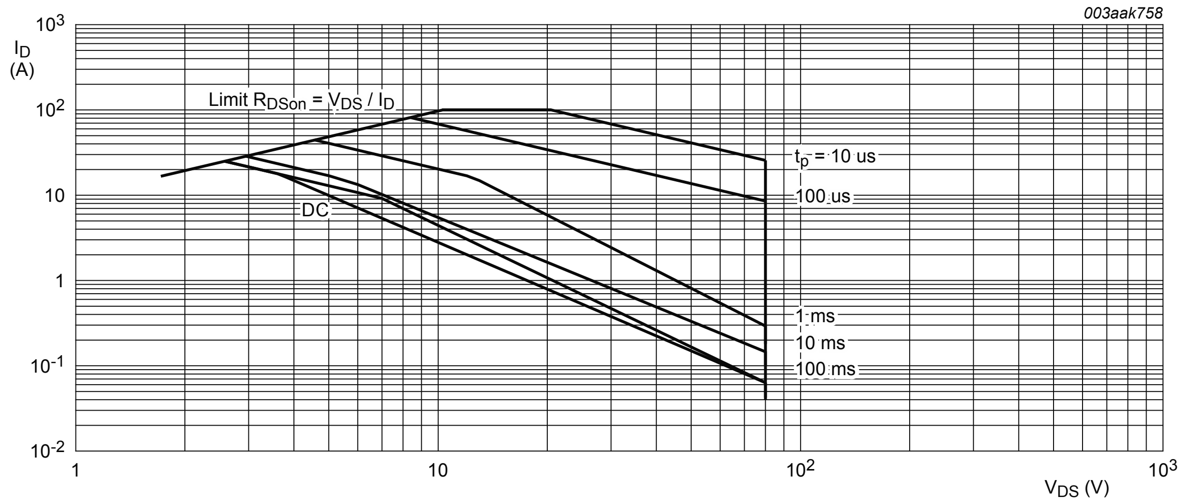


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	2.13	2.33	K/W

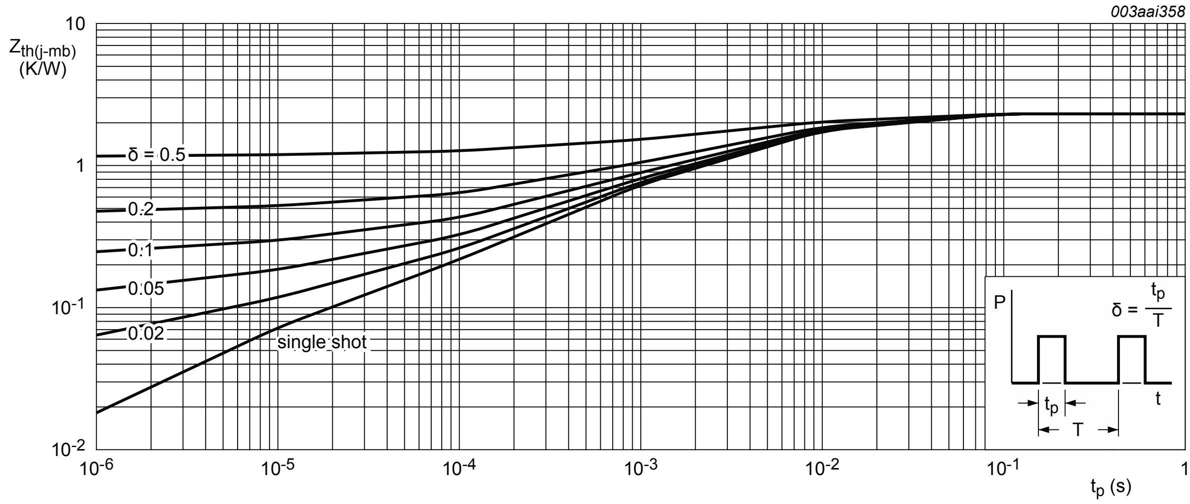


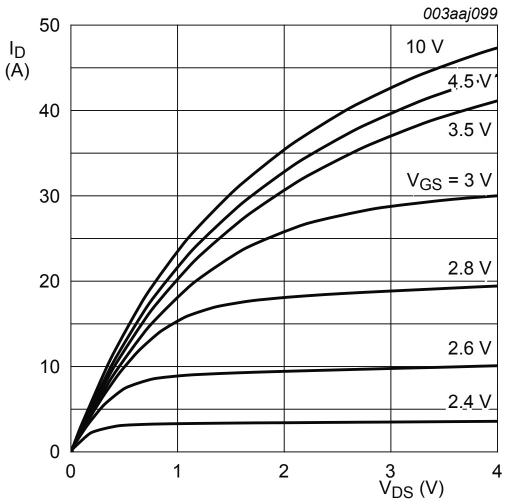
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		72	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10		0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.45	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		1.4	1.7	2.1	V
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C		-	0.02	1	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 12		-	32.8	41	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 175 °C; Fig. 13; Fig. 12		-	-	113	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 175 °C; Fig. 13; Fig. 12		-	-	103	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; Fig. 12		-	35.7	45	mΩ
R_G	gate resistance	f = 1 MHz		-	2.02	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 64 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		-	21.9	-	nC
		I_D = 5 A; V_{DS} = 64 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 14; Fig. 15		-	11.9	-	nC
Q_{GS}	gate-source charge	I_D = 5 A; V_{DS} = 64 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		-	2.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	1.7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.8	-	nC
Q_{GD}	gate-drain charge			-	4.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 5 A; V_{DS} = 64 V; T_j = 25 °C; Fig. 14; Fig. 15		-	2.4	-	V
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	1180	-	pF
C_{oss}	output capacitance			-	99	-	pF
C_{rss}	reverse transfer capacitance			-	54	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 60 V; R_L = 10 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	8.6	-	ns
t_r	rise time			-	11.2	-	ns
$t_{d(off)}$	turn-off delay time			-	16.1	-	ns
t_f	fall time			-	10.5	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C		-	21.3	-	ns
Q_r	recovered charge			-	22	-	nC



T_j = 25 °C; t_p = 300 μs

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

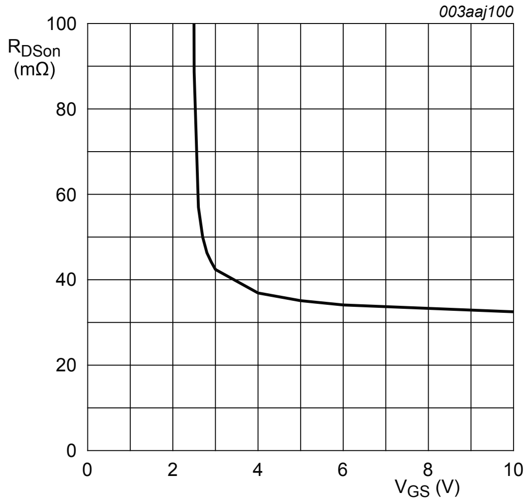


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 5A$

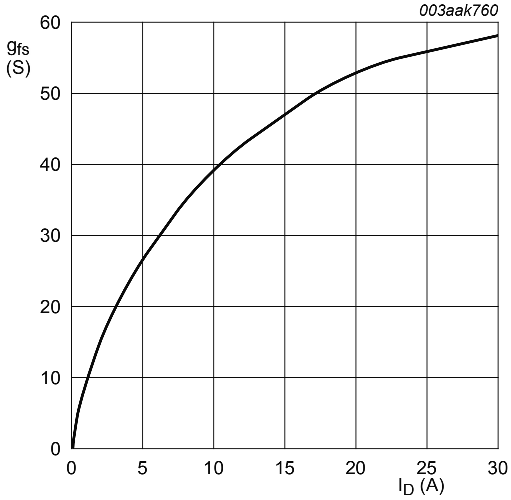


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25°C;\ V_{DS} = 10V$

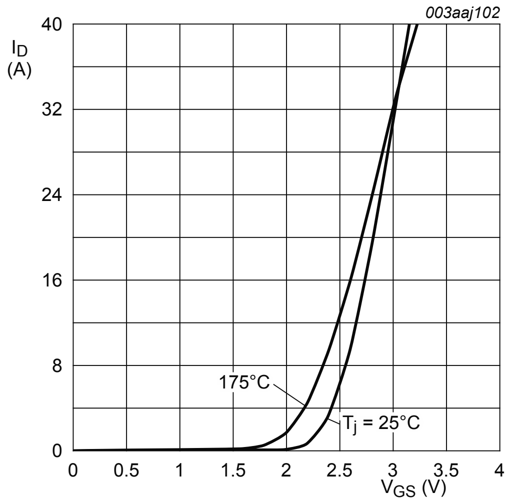


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

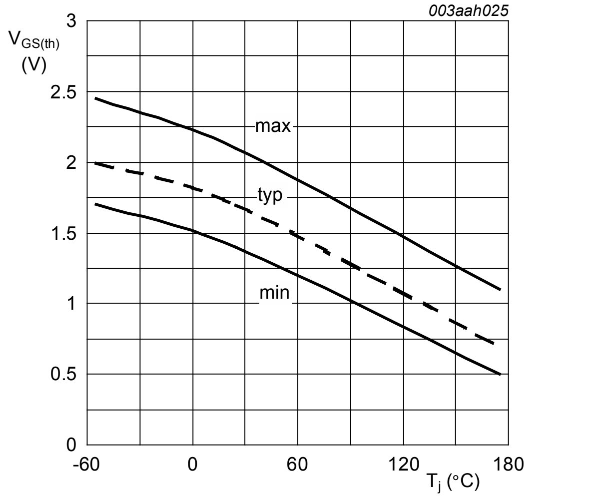


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1$ mA; $V_{DS} = V_{GS}$

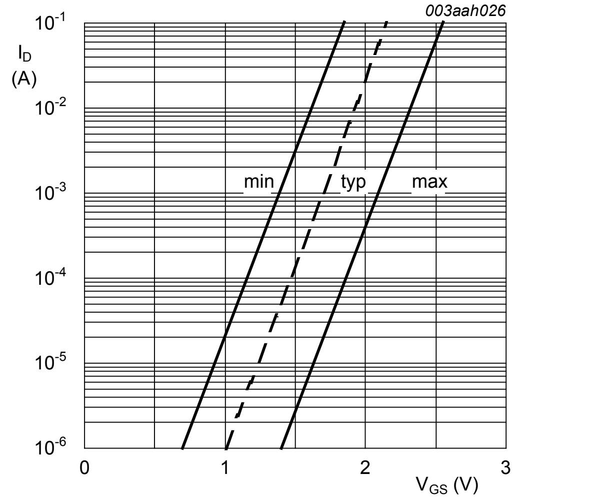
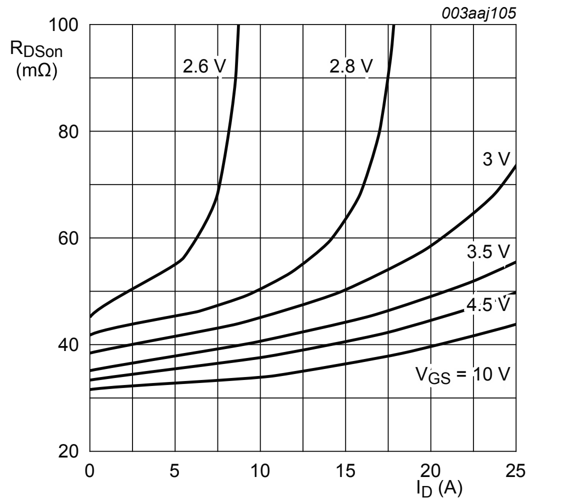


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25°C$; $V_{DS} = 5V$



$T_j = 25$ °C; $t_p = 300$ µs

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

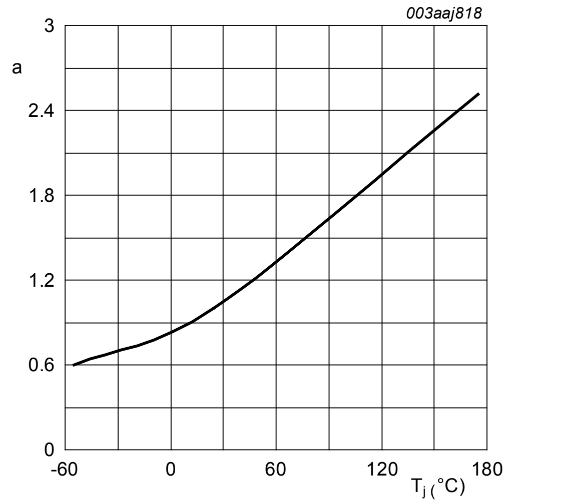


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

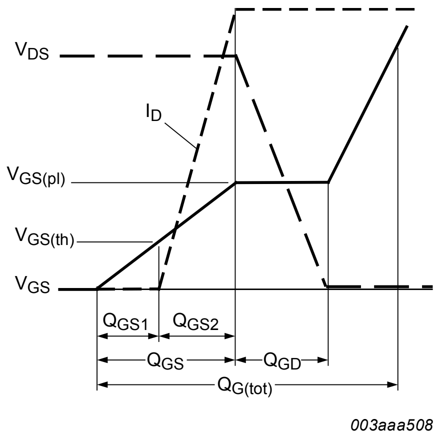


Fig. 14. Gate charge waveform definitions

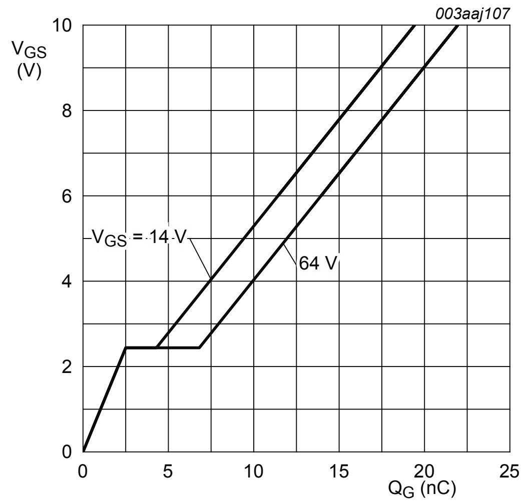


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 5A$

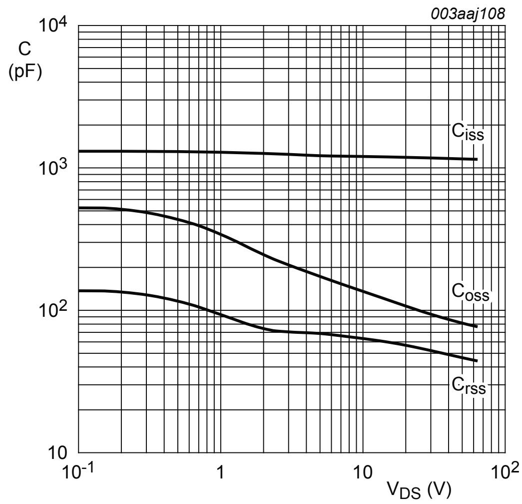


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

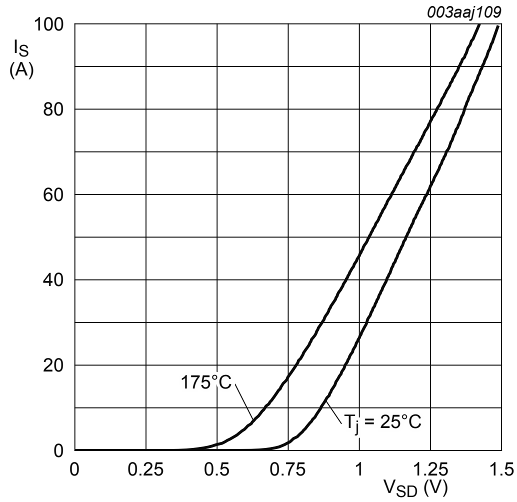
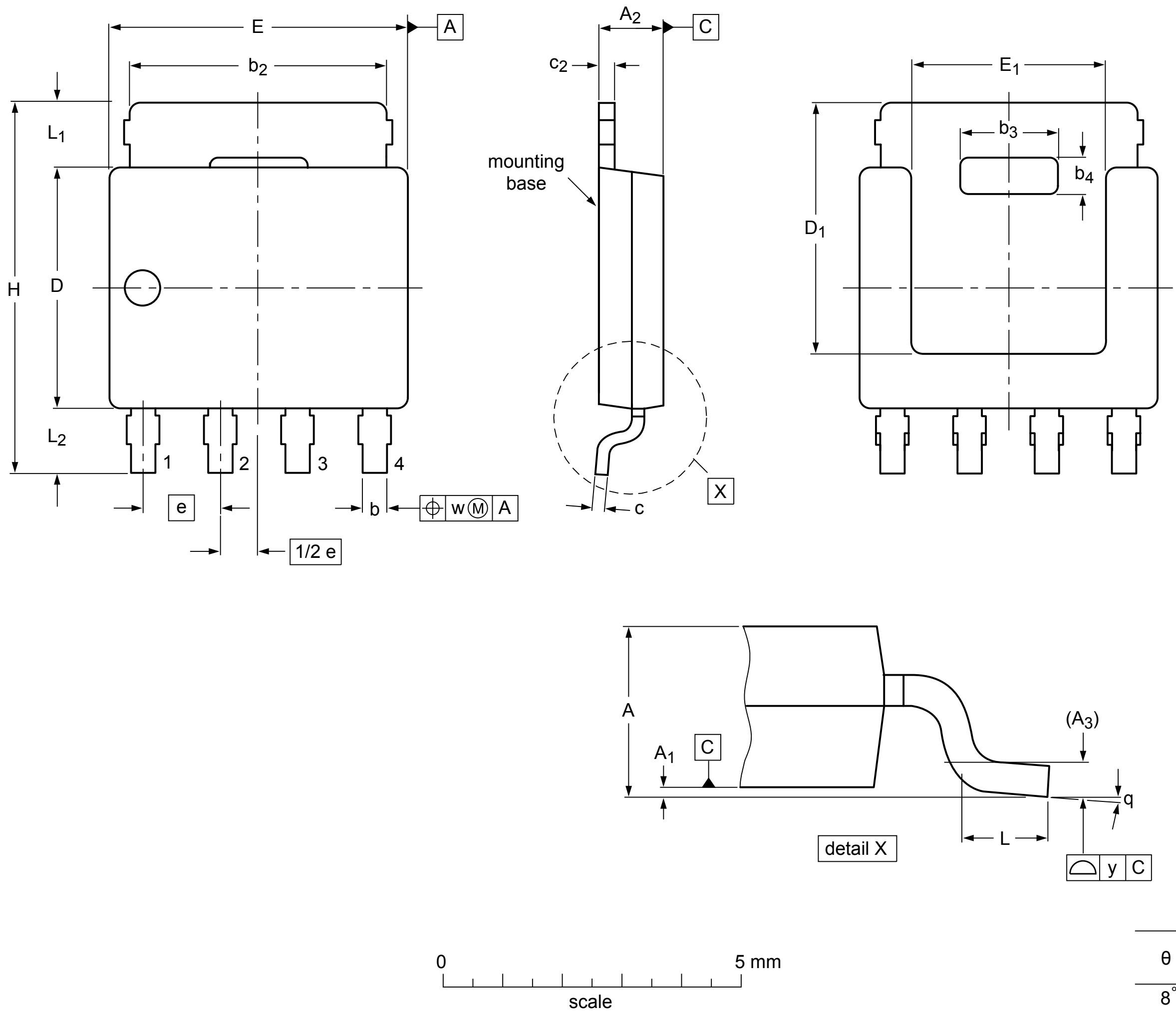


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 18. Package outline LFPAK56; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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Date of release: 01 May 2013