



# PSMN1R0-30YLC

N-channel 30 V 1.15 mΩ logic level MOSFET in LPAK using NextPower technology

15 January 2015

Product data sheet

## 1. General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low R<sub>ds(on)</sub> and low parasitic inductance

## 3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	30	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; <a href="#">Fig. 2</a>	[1]	-	-	100	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	-	272	W
T <sub>j</sub>	junction temperature			-55	-	175	°C
<b>Static characteristics</b>							
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 12</a>		-	1.1	1.4	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 12</a>		-	0.85	1.15	mΩ

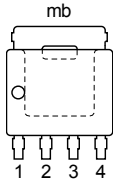
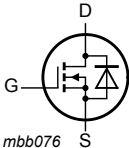
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	14.6	26	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	50	70	nC

[1] Continuous current is limited by package.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-30YLC	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-30YLC	1C030L

## 8. Limiting values

Table 5. Limiting values

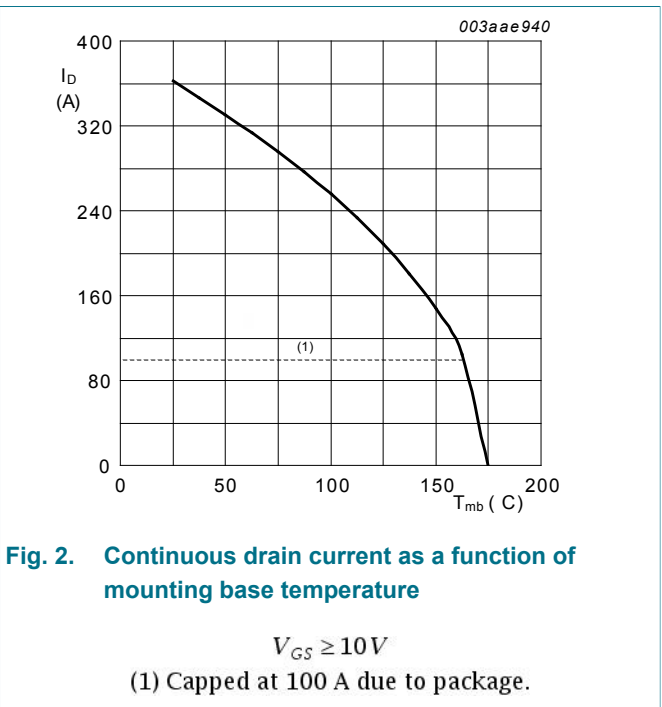
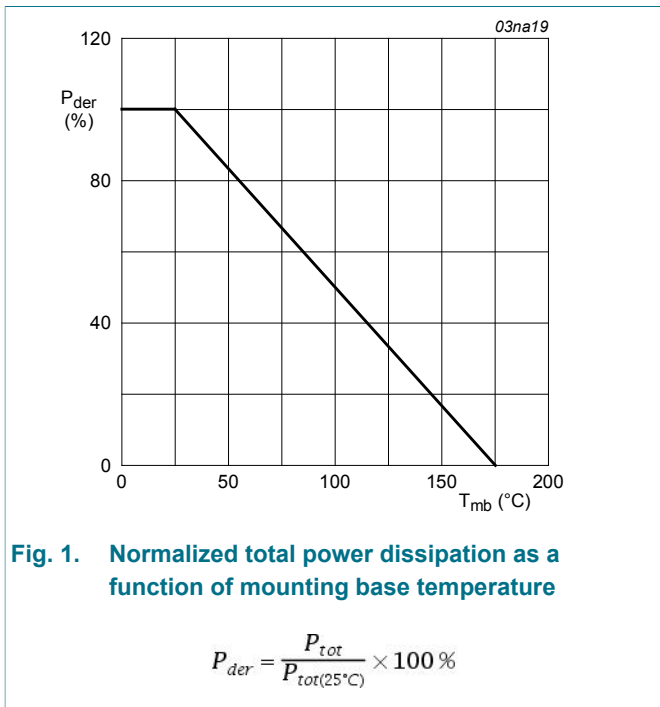
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	272	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	<a href="#">[1]</a>	-	100	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 2</a>	<a href="#">[1]</a>	-	100	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 3</a>		-	1450	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature			-	260	°C
V <sub>ESD</sub>	electrostatic discharge voltage	MM (JEDEC JESD22-A115)		960	-	V
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	<a href="#">[1]</a>	-	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	1450	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; unclamped; <a href="#">Fig. 4</a>		-	259	mJ

[1] Continuous current is limited by package.



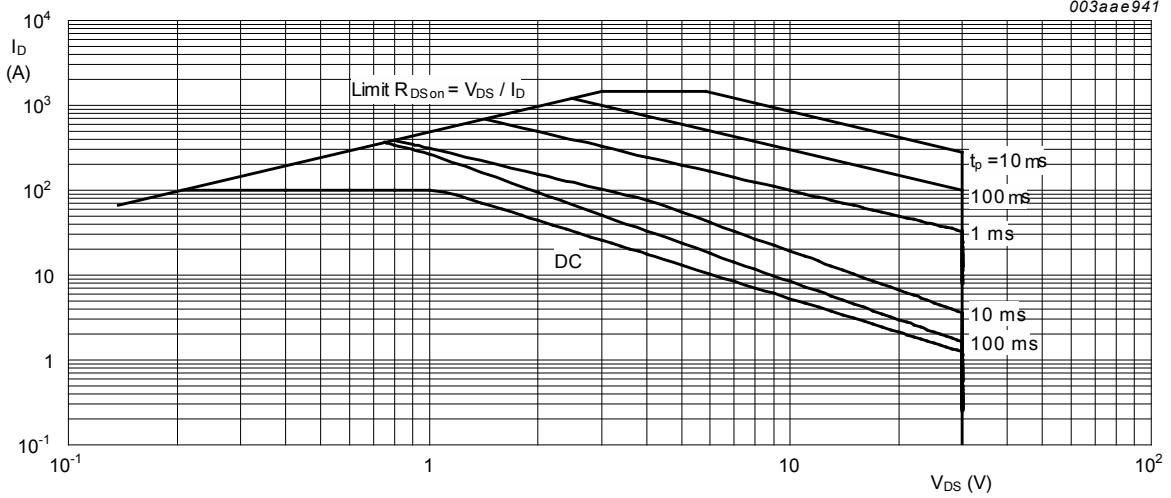


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

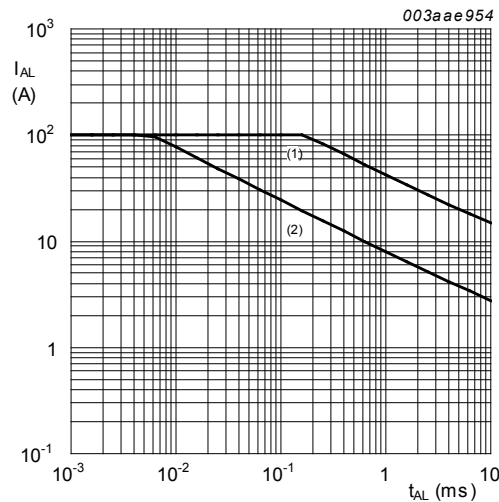


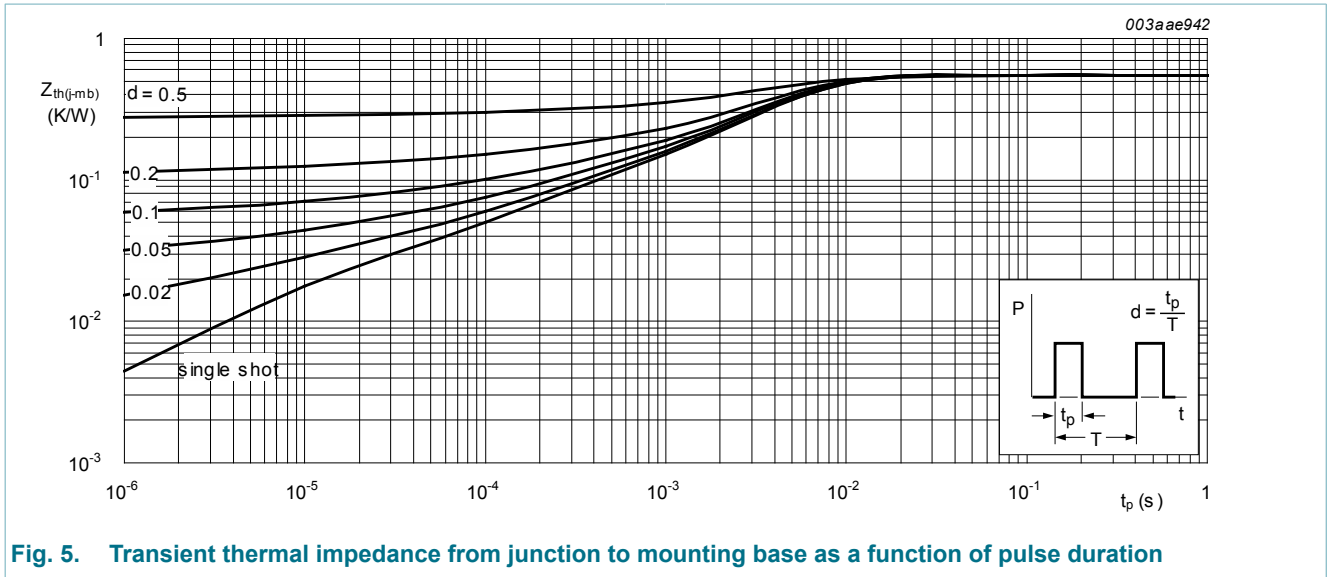
Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j(jrit)} = 25^{\circ}C$ ; (2)  $T_{j(jrit)} = 100^{\circ}C$

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.55	K/W



## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_J = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_J = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	1.05	1.41	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_J = 150 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = -55 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	2.25	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 150 \text{ }^\circ C$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_J = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	1.1	1.4	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_J = 150 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	2.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_J = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	0.85	1.15	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_J = 150 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	1.85	mΩ

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.1	2.2	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	103.5	145	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	50	70	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 15</a>	-	96.5	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	12.9	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge		-	10.1	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge		-	2.8	-	nC
$Q_{GD}$	gate-drain charge		-	14.6	26	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V};$ <a href="#">Fig. 14</a>	-	2.2	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	3322	6645	9968	pF
$C_{oss}$	output capacitance		605	1210	1815	pF
$C_{rss}$	reverse transfer capacitance		240	481	842	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.6 \text{ } \Omega; V_{GS} = 4.5 \text{ V};$ $R_{G(\text{ext})} = 4.7 \text{ } \Omega$	-	44	-	ns
$t_r$	rise time		-	77	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	108	-	ns
$t_f$	fall time		-	60	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C}$	-	35.2	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 17</a>	-	0.8	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 15 \text{ V}$	-	45	-	ns
$Q_r$	recovered charge		-	67	-	nC
$t_a$	reverse recovery rise time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 15 \text{ V};$ <a href="#">Fig. 18</a>	-	28.5	-	ns
$t_b$	reverse recovery fall time		-	16.5	-	ns

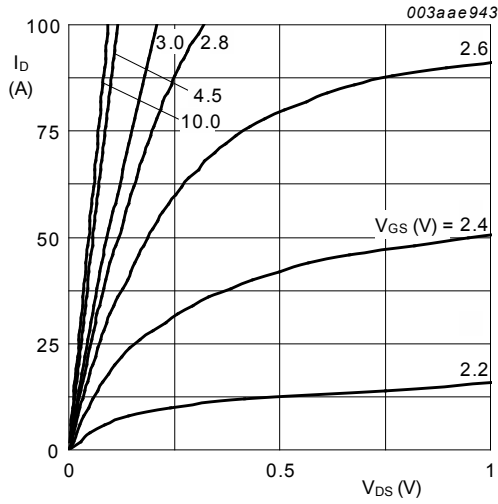


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_J = 25^\circ\text{C}$

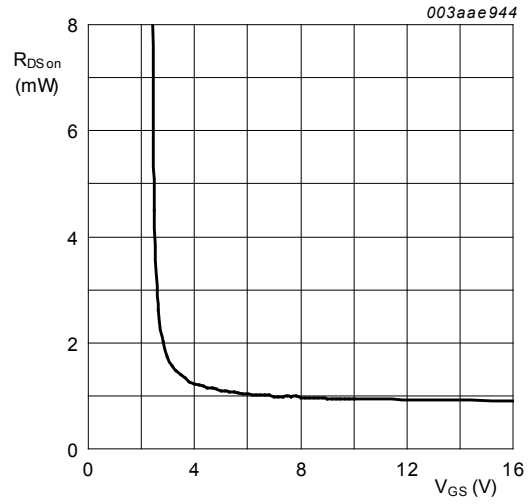


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_J = 25^\circ\text{C}; I_D = 25\text{A}$

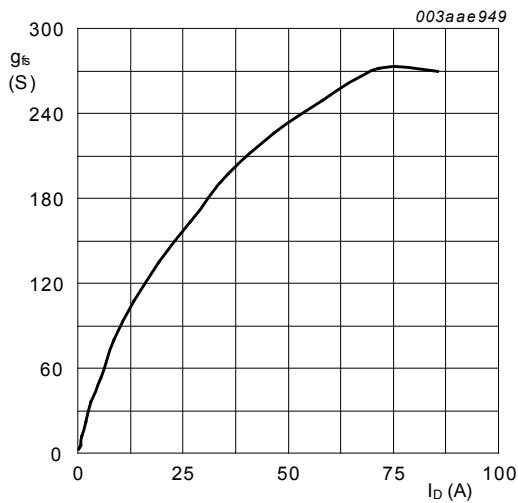


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_J = 25^\circ\text{C}; V_{DS} = 10\text{V}$

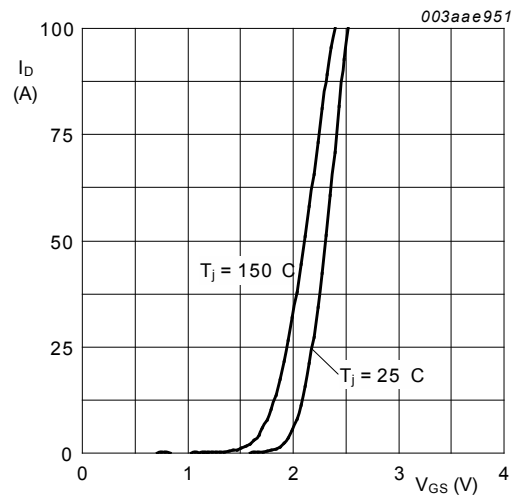


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

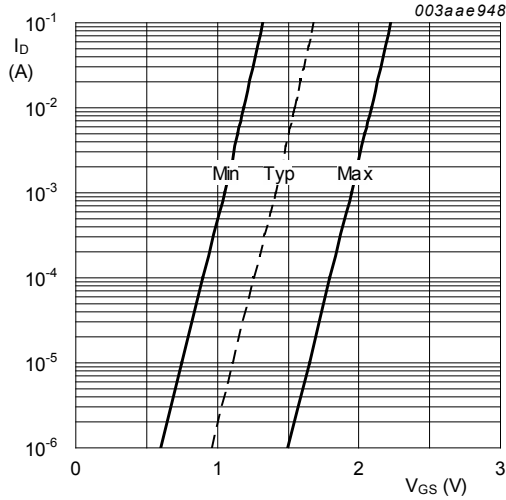


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

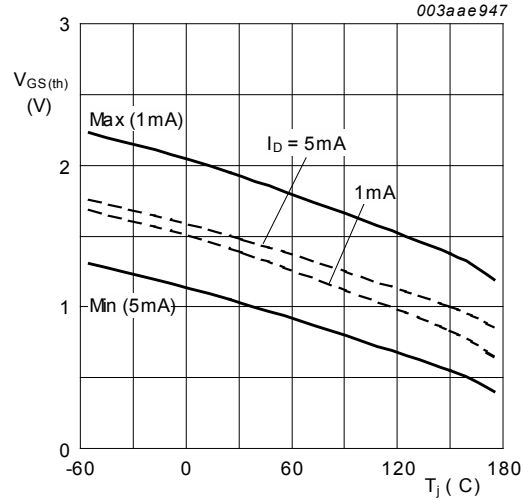


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$V_{DS} = V_{GS}$$

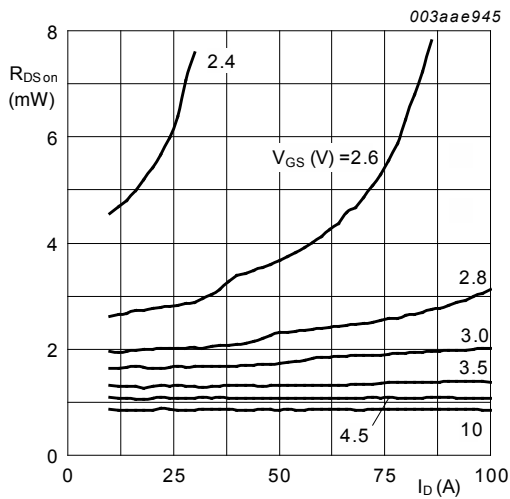


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

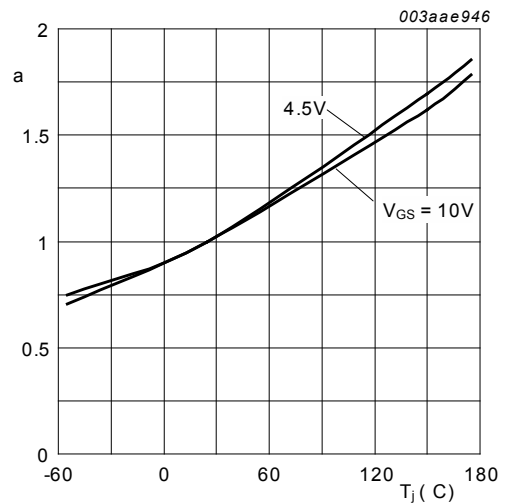


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$



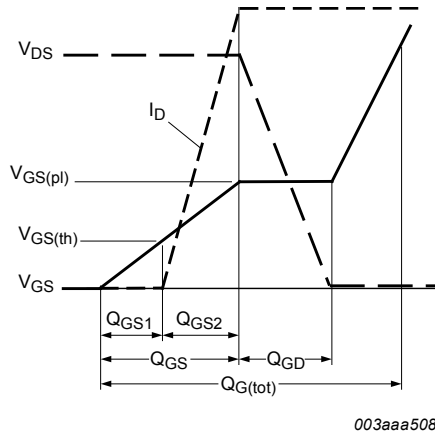


Fig. 14. Gate charge waveform definitions

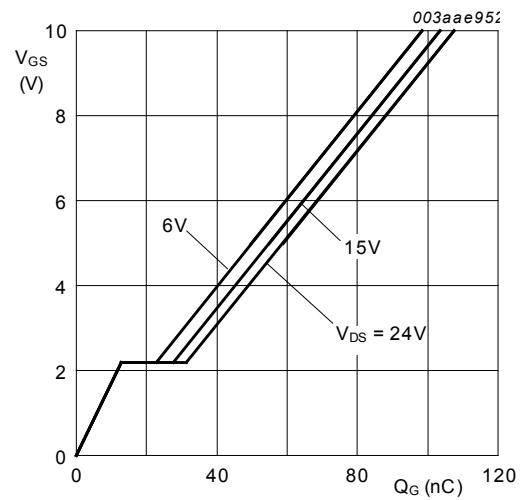


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ C; I_D = 25A$$

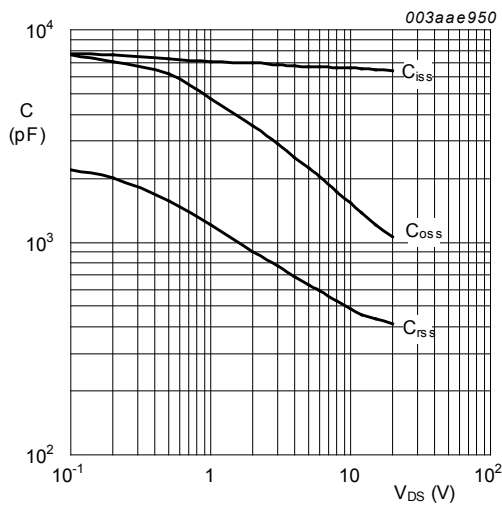


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

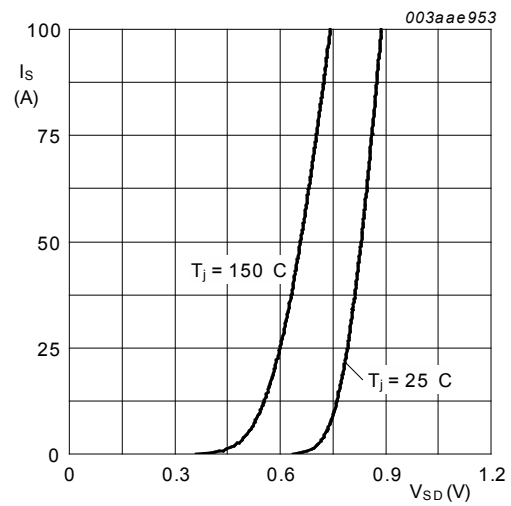


Fig. 17. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0V$$

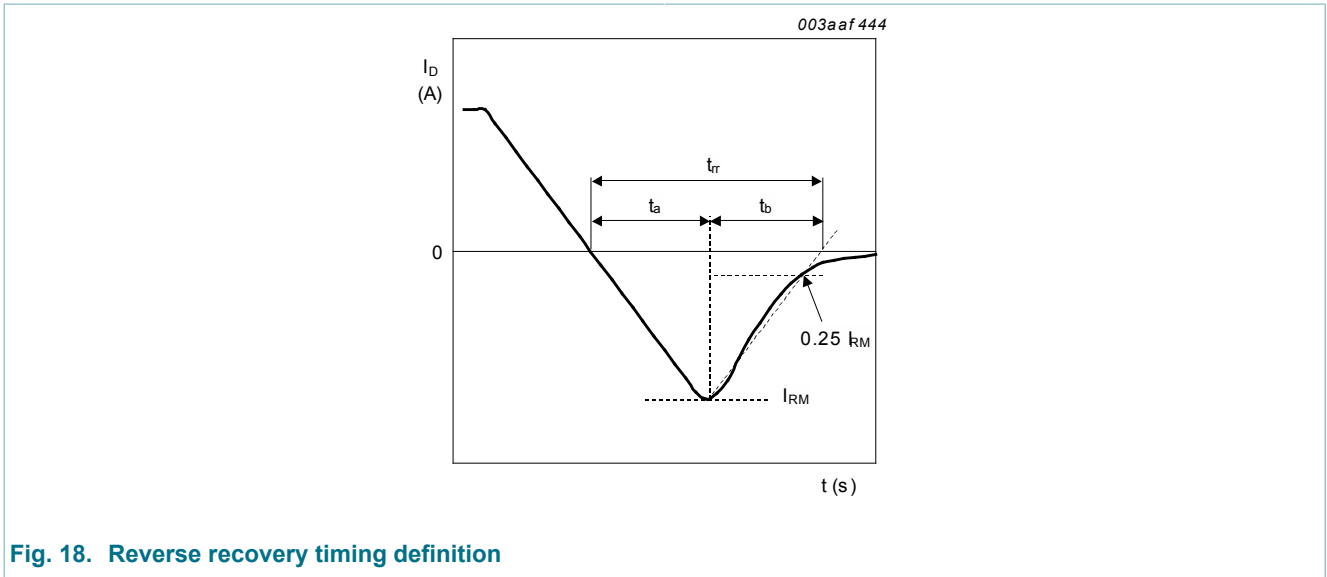


Fig. 18. Reverse recovery timing definition

### 11. Package outline

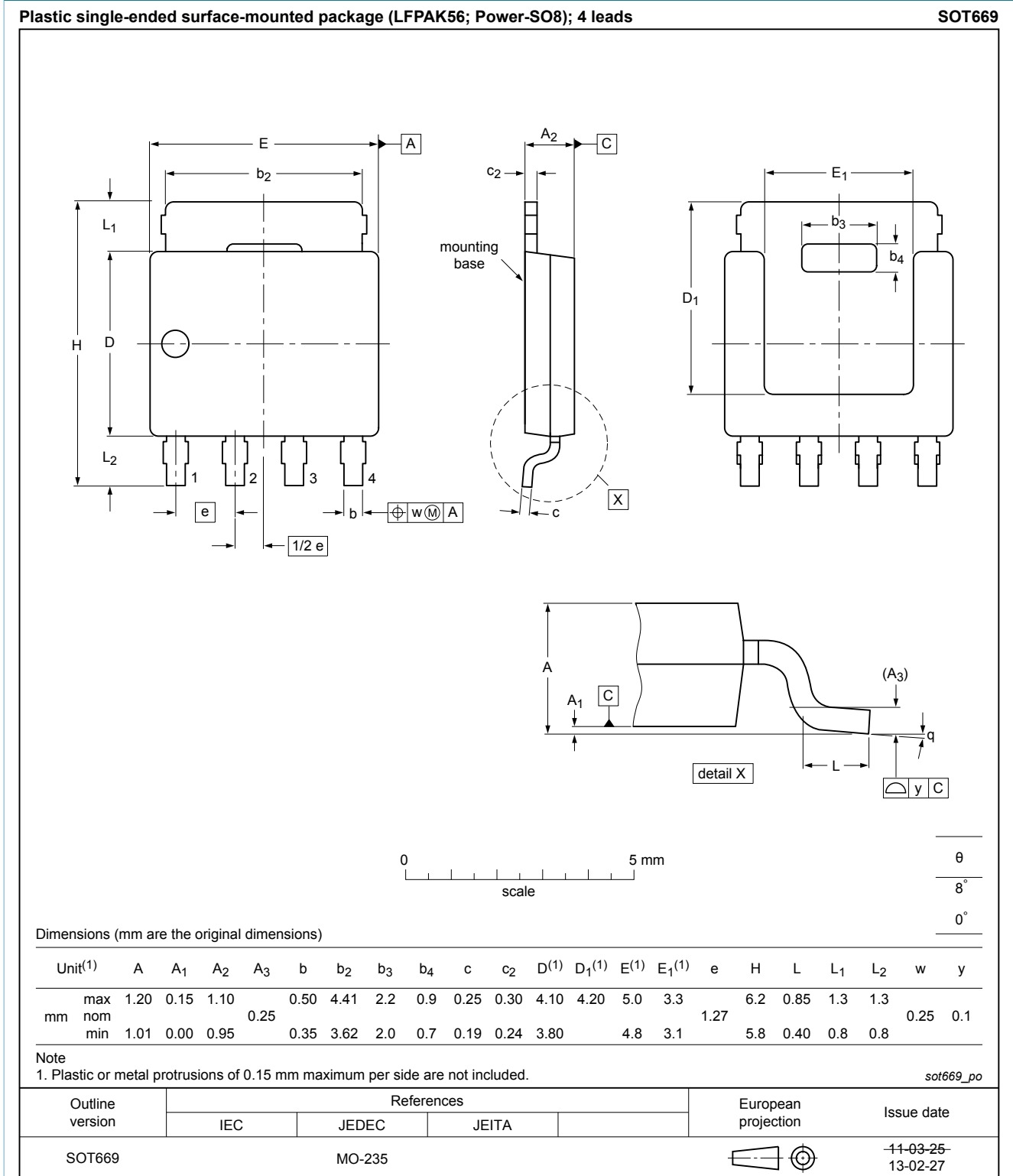


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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## 13. Contents

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