
# PSMN1R0-40YLD

## N-channel 40 V, 1.1 mΩ, 280 A logic level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology

30 November 2017 | Product data sheet

## 1. General description

280 Amp, logic level gate drive N-channel enhancement mode MOSFET in 150 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

## 2. Features and benefits

- 280 A capability
- Avalanche rated, 100% tested at $I_{AS}$ = 190 A
- NextPower-S3 technology delivers 'superfast switching with soft recovery'
- Low $Q_{RR}$, $Q_G$ and $Q_{GD}$ for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high $I_{DSS}$ leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LFPAK (Power SO8) package, copper-clip, solder die attach and qualified to 150 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

## 3. Applications

- Synchronous rectification
- DC-to-DC converters
- High performance & high efficiency server power supply
- Motor control
- Power ORing

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 150 °C | | - | - | 40 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | - | 280 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 198 | W |
| $T_j$ | junction temperature | | | -55 | - | 150 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10; Fig. 11 | | - | 1.1 | 1.4 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10; Fig. 11 | | - | 0.93 | 1.1 | mΩ |

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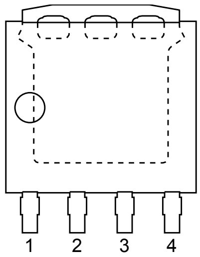
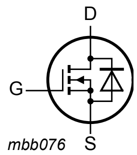
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 4.5 V; Fig. 12; Fig. 13 | | - | 17 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | | - | 59 | - | nC |

[1] 280A continuous current has been successfully demonstrated during application tests. Practically, the current will be limited by PCB, thermal design and operation temperature.

## 5. Pinning information

**Table 2. Pinning information**

<table>
<tr><th>Pin</th><th>Symbol</th><th>Description</th><th>Simplified outline</th><th>Graphic symbol</th></tr>
<tr><td>1</td><td>S</td><td>source</td><td rowspan="5">

LFPAK56; Power-SO8 (SOT1023)</td><td rowspan="5">
</td></tr>
<tr><td>2</td><td>S</td><td>source</td></tr>
<tr><td>3</td><td>S</td><td>source</td></tr>
<tr><td>4</td><td>G</td><td>gate</td></tr>
<tr><td>mb</td><td>D</td><td>mounting base; connected to drain</td></tr>
</table>

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN1R0-40YLD | LFPAK56; Power-SO8 | Plastic single-ended surface-mounted package (LFPAK56); 4 leads | SOT1023 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PSMN1R0-40YLD | 1D040L |

## 8. Limiting values

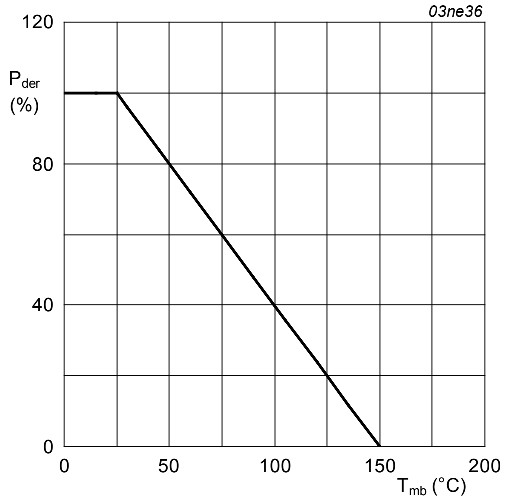
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 150 °C | | - | 40 | V |
| $V_{DSM}$ | peak drain-source voltage | $t_p$ ≤ 20 ns; f ≤ 500 kHz; $E_{DS(AL)}$ ≤ 200 nJ; pulsed | | - | 45 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | | - | 40 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 198 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | 280 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 198 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 1284 | A |
| $T_{stg}$ | storage temperature | | | -55 | 150 | °C |
| $T_j$ | junction temperature | | | -55 | 150 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | | 2 | - | kV |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 165 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | 1284 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 85 A; $V_{sup}$ ≤ 40 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 0.26 ms | [2] | - | 578 | mJ |
| | | $I_D$ = 25 A; $V_{sup}$ ≤ 40 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 3.8 ms | [2] | - | 2472 | mJ |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup}$ ≤ 40 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω | [2] | - | 190 | A |

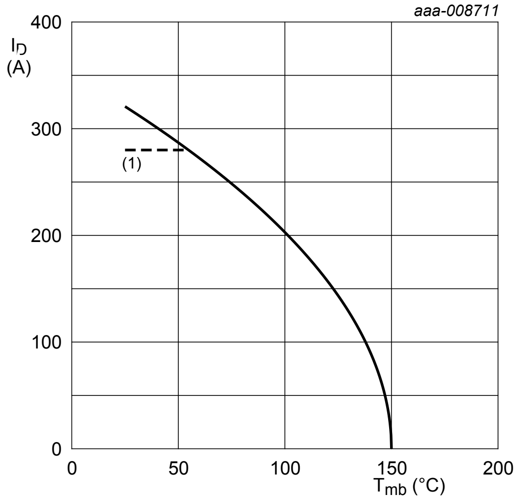
[1] 280A continuous current has been successfully demonstrated during application tests. Practically, the current will be limited by PCB, thermal design and operation temperature.

[2] Protected by 100% test




$$P_{der} = \frac{P_{(tot)}}{P_{tot(25°C)}} \times 100\,\%$$

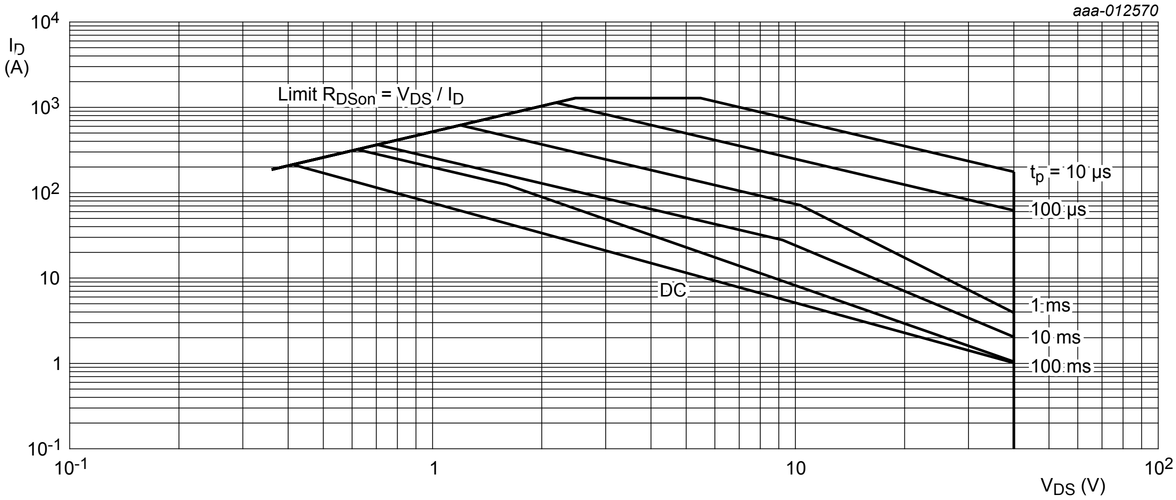
**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**




(1) 280A continuous current has been successfully demonstrated during applications tests. Practically, the current will be limited by PCB, thermal design and operating temperature.

$V_{GS} \geq 10V$

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb} = 25°C$; $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4 | | - | 0.56 | 0.63 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 5 | | - | 50 | - | K/W |
| | | Fig. 6 | | - | 125 | - | K/W |

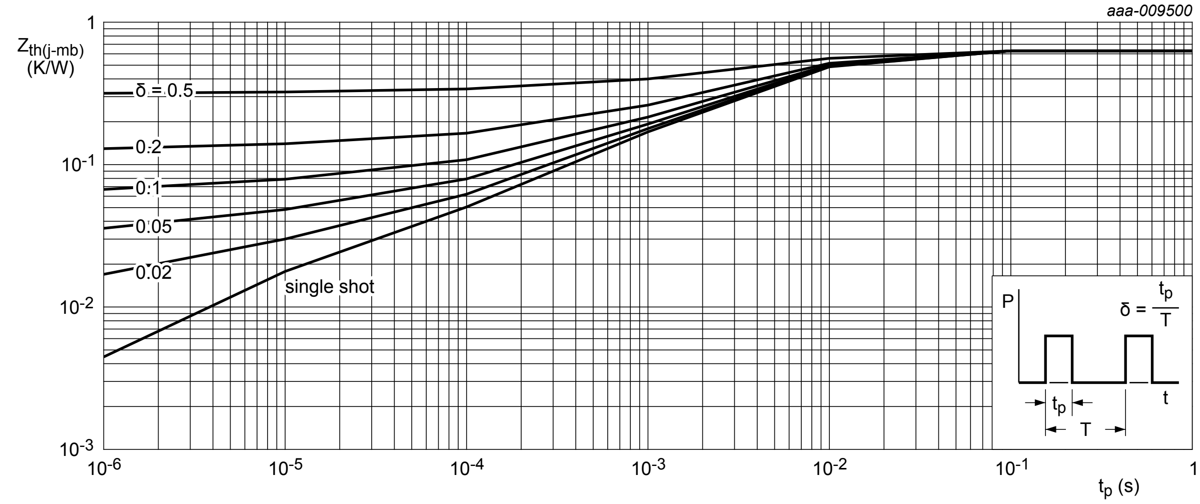



**Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

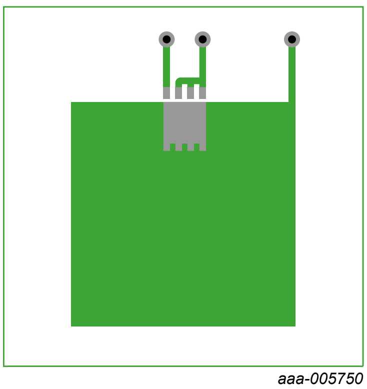



**Fig. 5. PCB layout for thermal resistance junction to ambient 1” square pad; FR4 Board; 2oz copper**

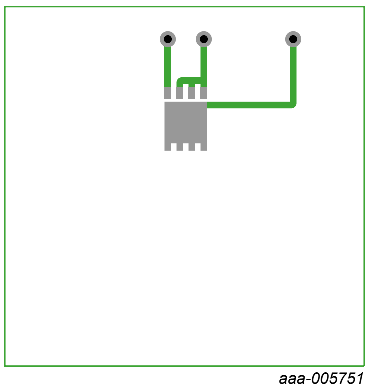



**Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper**

## 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 40 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 36 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C | | 1.05 | 1.7 | 2.2 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | 25 °C ≤ $T_j$ ≤ 150 °C | | - | -5.1 | - | mV/K |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 32 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_{DS}$ = 32 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | 9 | - | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| | | $V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10; Fig. 11 | | - | 0.93 | 1.1 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 10; Fig. 11 | | - | - | 1.93 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10; Fig. 11 | | - | 1.1 | 1.4 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 10; Fig. 11 | | - | - | 2.45 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz | | - | 1.3 | - | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 10 V; Fig. 12; Fig. 13 | | - | 127 | - | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 4.5 V; Fig. 12; Fig. 13 | | - | 59 | - | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V | | - | 115 | - | nC |
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 4.5 V; Fig. 12; Fig. 13 | | - | 19 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | - | 12 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | - | 8 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 17 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 20 V; Fig. 12; Fig. 13 | | - | 2.7 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 20 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 14 | | - | 8845 | - | pF |
| $C_{oss}$ | output capacitance | | | - | 1878 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 382 | - | pF |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 20 V; $R_L$ = 0.8 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5 Ω | | - | 52 | - | ns |
| $t_r$ | rise time | | | - | 62 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 65 | - | ns |
| $t_f$ | fall time | | | - | 38 | - | ns |
| $Q_{oss}$ | output charge | $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; f = 1 MHz; $T_j$ = 25 °C | | - | 51 | - | nC |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 15 | | - | 0.78 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; Fig. 16 | | - | 48 | - | ns |
| $Q_r$ | recovered charge | | [1] | - | 67 | - | nC |
| $t_a$ | reverse recovery rise time | | | - | 28.6 | - | ns |
| $t_b$ | reverse recovery fall time | | | - | 23.8 | - | ns |

[1] includes capacitive recovery

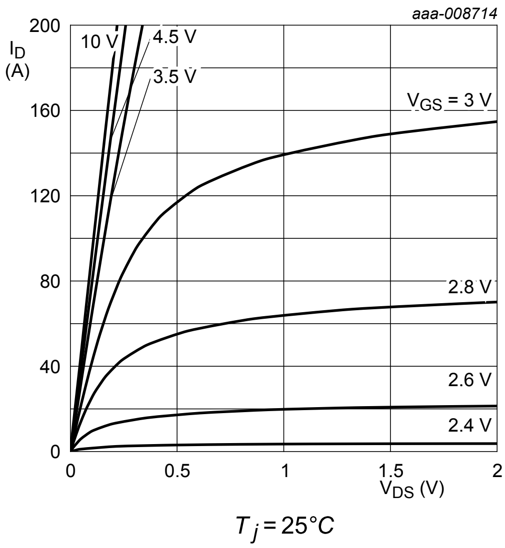



**Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values**

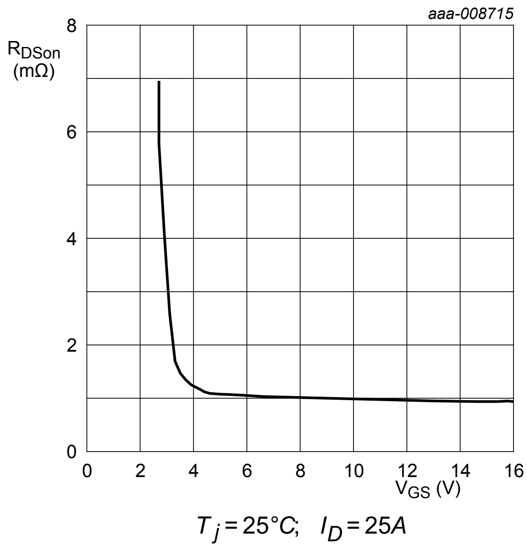
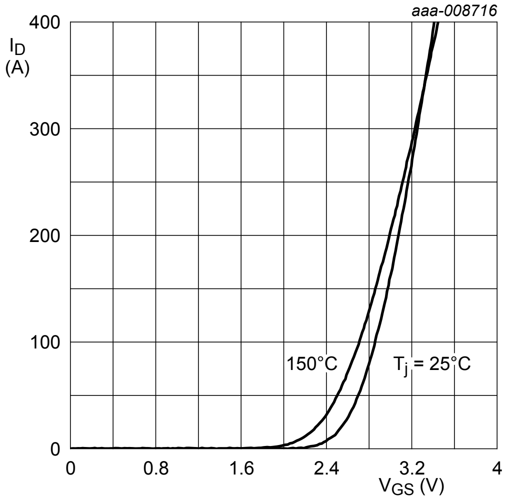
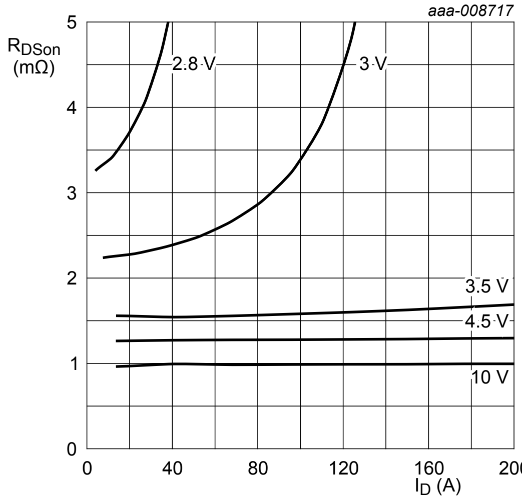



**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**



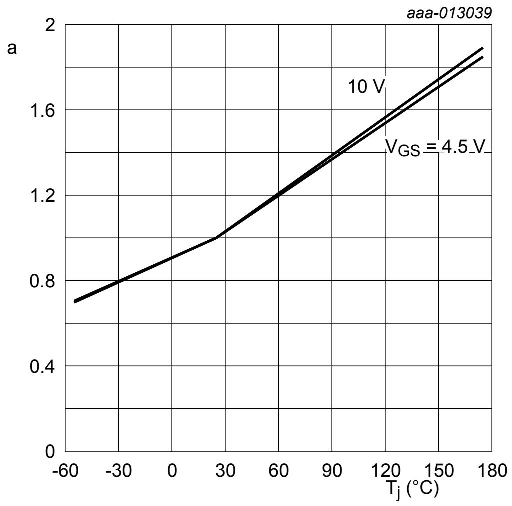

$V_{DS} = 12V$

**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**




$T_j = 25°C$

**Fig. 10. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

**Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature**

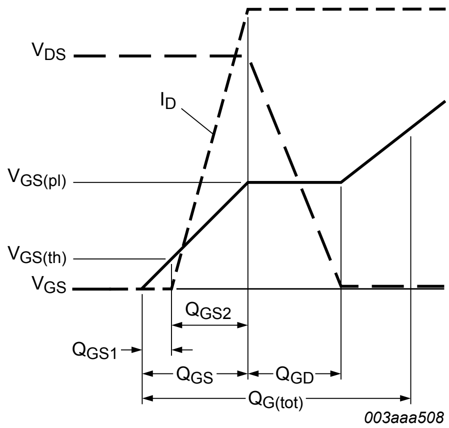



**Fig. 12. Gate charge waveform definitions**

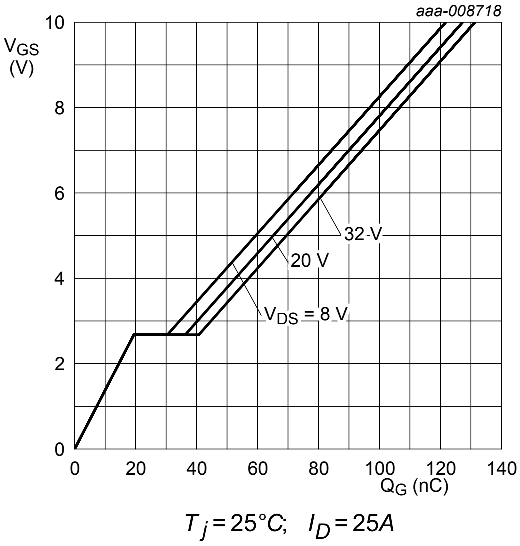



**Fig. 13. Gate-source voltage as a function of gate charge; typical values**

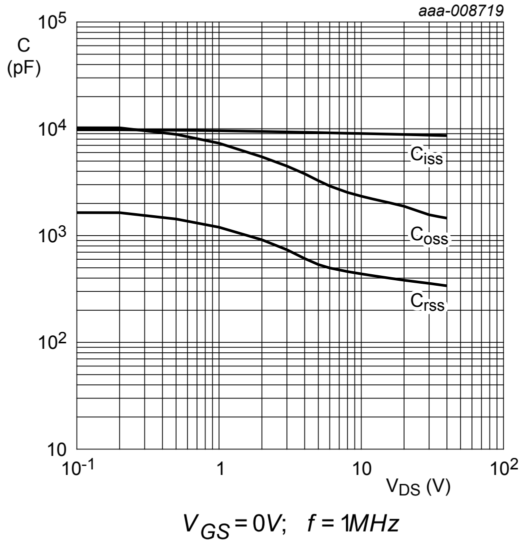



**Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

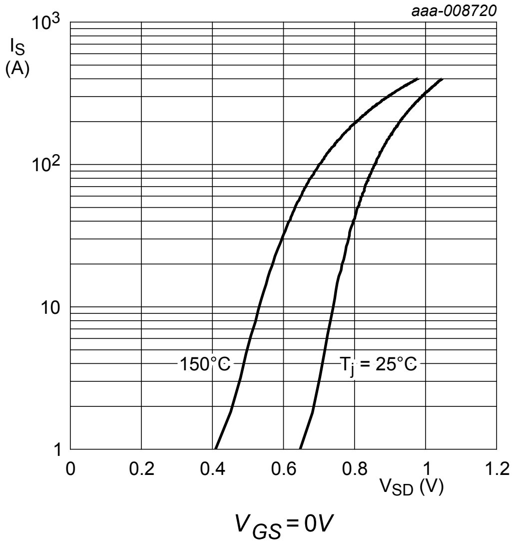



**Fig. 15. Source current as a function of source-drain voltage; typical values**

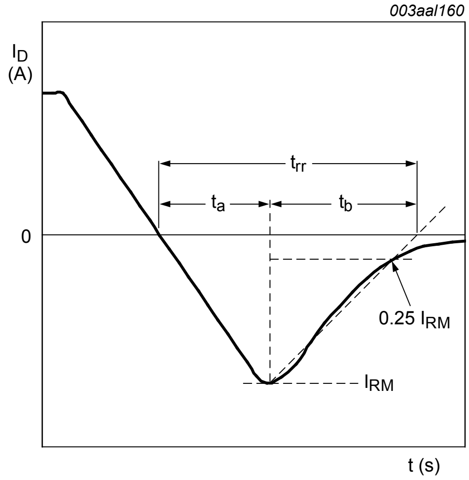
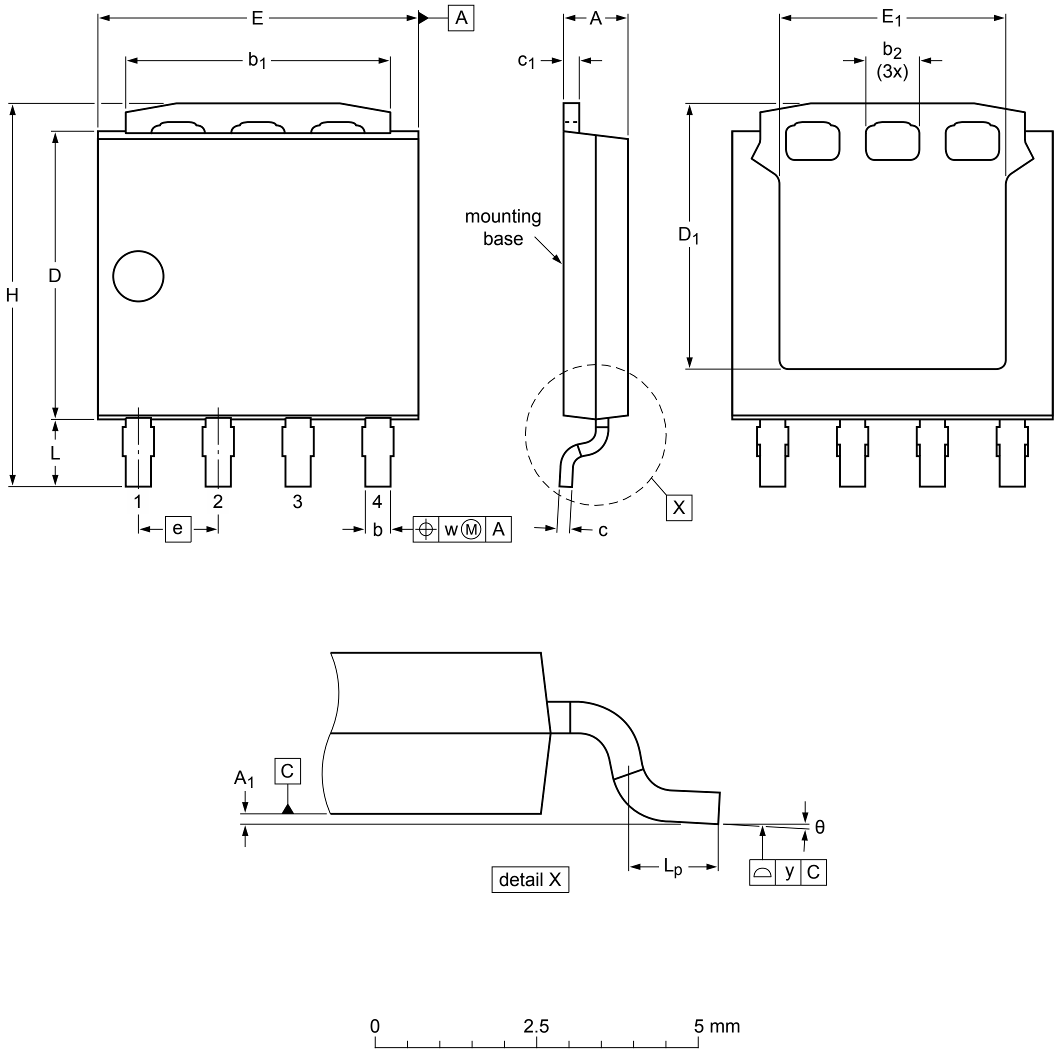



**Fig. 16. Reverse recovery timing definition**

## 11. Package outline

**Plastic single-ended surface-mounted package (LFPAK56E); 4 leads** **SOT1023**




Dimensions

| Unit | | A | $A_1$ | b | $b_1$ | $b_2$ | c | $c_1$ | $D^{(1)}$ | $D_1^{(1)}$ | $E^{(1)}$ | $E_1^{(1)}$ | e | H | L | $L_p$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.10 | 0.15 | 0.50 | 4.41 | | 0.25 | 0.30 | 4.70 | 4.45 | 5.30 | 3.7 | | 6.2 | 1.3 | 0.85 | | | 8° |
| | nom | | | | | 0.85 | | | | | | | 1.27 | | | | 0.25 | 0.1 | |
| | min | 0.95 | 0.00 | 0.35 | 3.62 | | 0.19 | 0.24 | 4.45 | | 4.95 | 3.5 | | 5.9 | 0.8 | 0.40 | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

*sot1023_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1023 | | | | | | ~~13-03-05~~<br>17-07-31 |

**Fig. 17. Package outline LFPAK56; Power-SO8 (SOT1023)**

## 12. Soldering

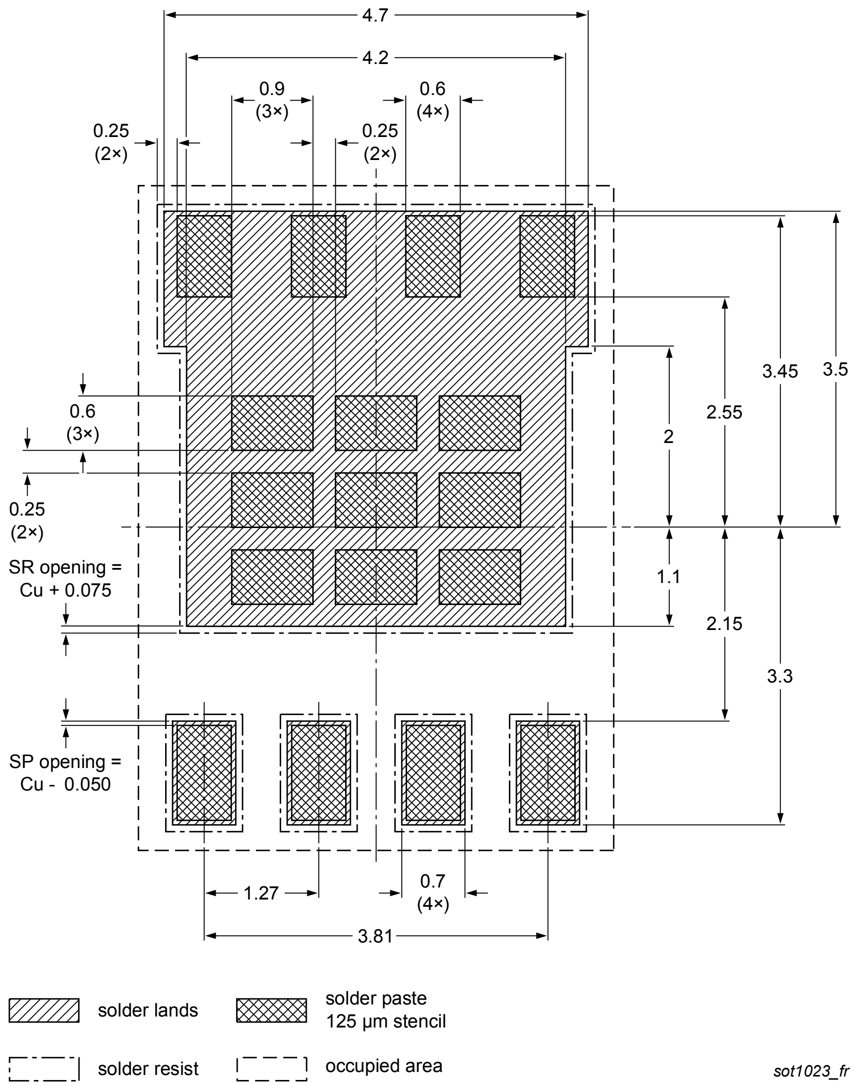



**Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT1023)**

# 13. Legal information

### Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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