

PSMN1R5-30YLC

N-channel 30 V 1.55m Ω logic level MOSFET in LFPAK using NextPower technology

Rev. 2 — 17 May 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, and QOSS for high system efficiencies at low and high loads
- Ultra low Rdson and low parasitic inductance

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching

- Power OR-ing
- Server power supplies
- Sync rectifier

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	30	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	[1]	-	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	179	W
Tj	junction temperature			-55	-	175	°C
Static cha	aracteristics						
R _{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see <u>Figure 12</u>		-	1.65	2.05	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 12		-	1.3	1.55	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 15 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	8.6	-	nC
Q _{G(tot)}	total gate charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 15 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	30	-	nC

^[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		5
2	S	source	mb (D
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	1 2 3 4	mbb076 S

SOT669 (LFPAK; Power-SO8)

3. Ordering information

Table 3. Ordering information

Type number	Package			
	Name	Description	Version	
PSMN1R5-30YLC	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669	

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PSMN1R5-30YLC	1C530L

[1] % = placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	25 °C \leq T _j \leq 175 °C; R _{GS} = 20 k Ω		-	30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{M}}$	[1]	-	100	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 100 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure 1}}{}$	[1]	-	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$; see Figure 4		-	1008	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	179	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)		1000	-	V
Source-drain	diode					
Is	source current	T _{mb} = 25 °C	[1]	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	1008	Α
Avalanche rug	ggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω; unclamped; see Figure 3		-	147	mJ

[1] Continuous current is limited by package.

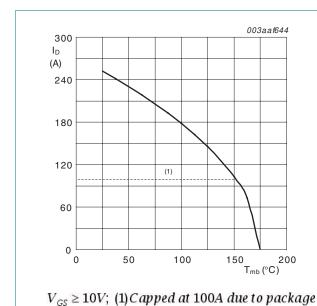


Fig 1. Continuous drain current as a function of mounting base temperature

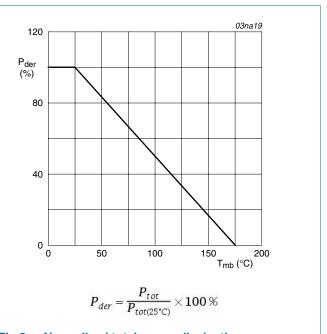


Fig 2. Normalized total power dissipation as a function of mounting base temperature

PSMN1R5-30YLC

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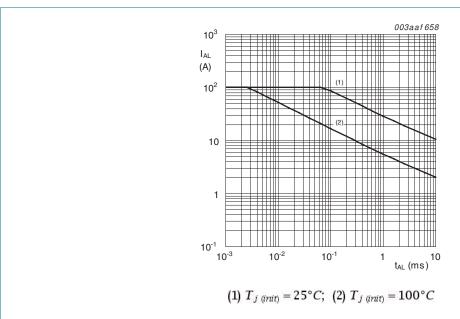
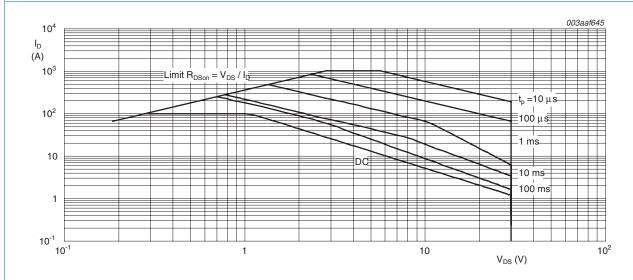


Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



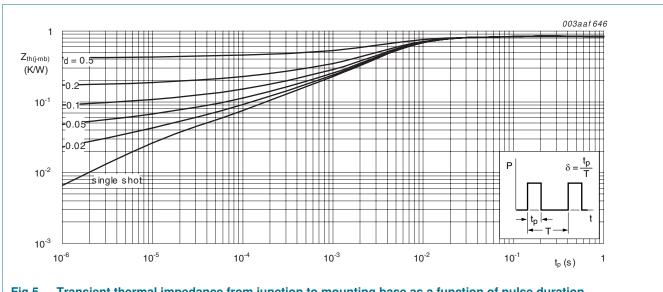
 $T_{mb} = 25$ °C; I_{DM} is a single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

Thermal characteristics

Table 6. **Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	0.71	0.84	K/W



Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Table 7.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source breakdown	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}C$	30	-	-	V
	voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^{\circ}C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see <u>Figure 10</u> ; see <u>Figure 11</u>	1.05	1.51	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ °C}$	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$	-	-	2.25	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 12</u>	-	1.65	2.05	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	-	3.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 12</u>	-	1.3	1.55	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	-	2.6	mΩ
R_G	gate resistance	f = 1 MHz	-	1.05	2.1	Ω
Dynamic	characteristics					
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	65	-	nC
		I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	30	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	53	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	9.7	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	see Figure 14; see Figure 15	-	6.6	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	3.1	-	nC
Q _{GD}	gate-drain charge		-	8.6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 15 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	2.53	-	V
C _{iss}	input capacitance	V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz;	-	4044	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	860	-	pF
C _{rss}	reverse transfer capacitance		-	287	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.6 \Omega; V_{GS} = 4.5 \text{ V};$	-	33	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	62	-	ns
t _{d(off)}	turn-off delay time		-	62	-	ns
t _f	fall time		-	38	-	ns

Table 7. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	23	-	nC
Source-drain	diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see Figure 17	-	0.8	1.1	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	41	-	ns
Q _r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}$	-	43	-	nC
ta	reverse recovery rise time	$V_{GS} = 0 \text{ V}; I_S = 25 \text{ A};$	-	24	-	ns
t _b	reverse recovery fall time	$dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{DS} = 15 \text{ V}$; see Figure 18	-	17	-	ns

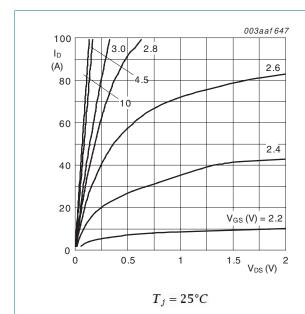


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

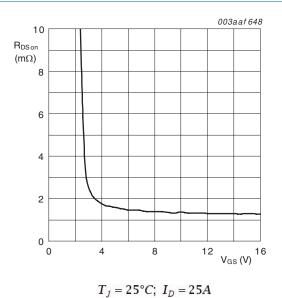


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

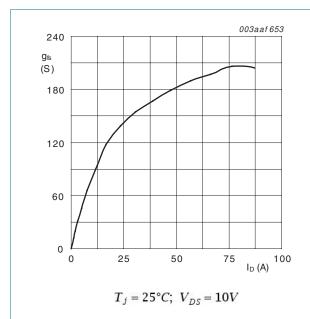


Fig 8. Forward transconductance as a function of drain current; typical values

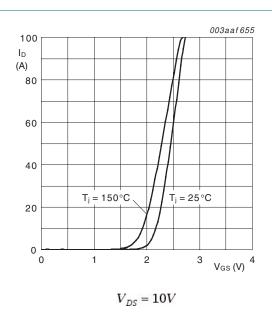


Fig 9. Transfer characteristics; drain-source current as a function of gate-source voltage; typical values

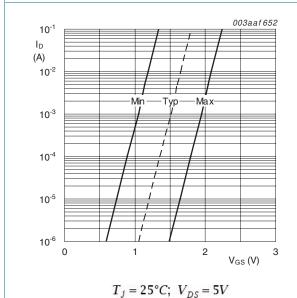


Fig 10. Sub-threshold drain current as a function of gate-source voltage

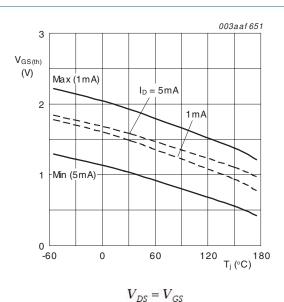


Fig 11. Gate-source threshold voltage as a function of junction temperature

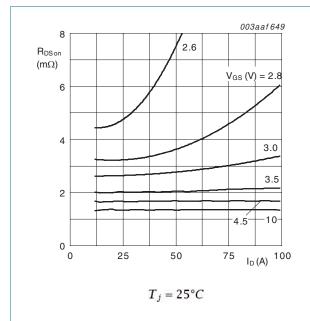


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

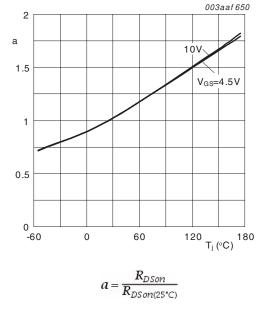


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

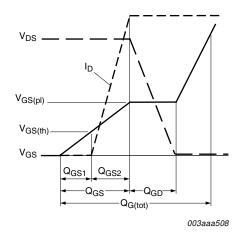


Fig 14. Gate charge waveform definitions

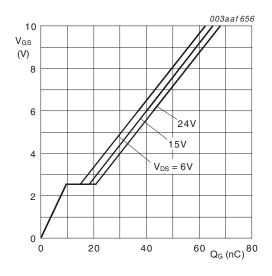
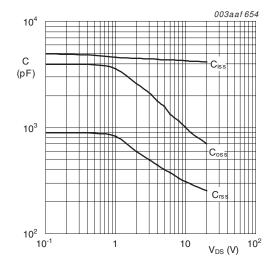


Fig 15. Gate-source voltage as a function of gate charge; typical values

 $T_j = 25^{\circ}C; I_D = 25A$



 $V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

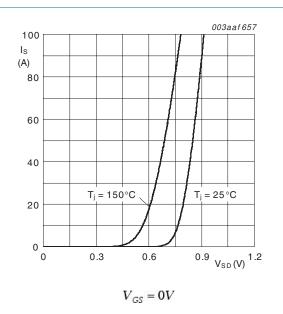


Fig 17. Source current as a function of source-drain voltage; typical values

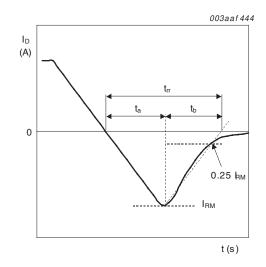


Fig 18. Reverse recovery timing definition

Package outline

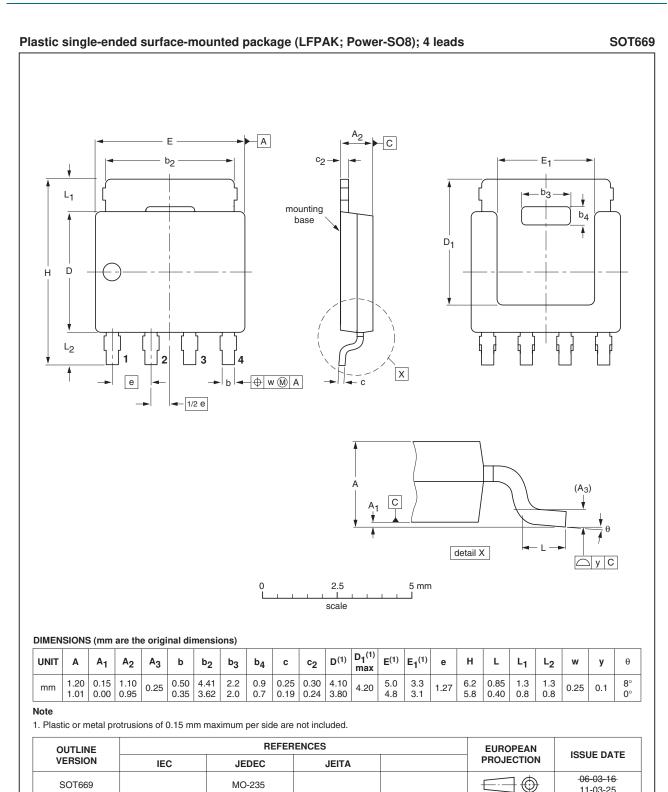


Fig 19. Package outline SOT669 (LFPAK; Power-SO8)

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11-03-25

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R5-30YLC v.2	20110517	Product data sheet	-	PSMN1R9-25YLC v.1
Modifications:	 Various changes to 	content.		
PSMN1R9-25YLC v.1	20110502	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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N-channel 30 V 1.55mΩ logic level MOSFET in LFPAK using NextPower

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