

PSMN4R5-40BS

N-channel 40 V 4.5 m Ω standard level MOSFET in D2PAK

Rev. 1 — 22 March 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in SOT404 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC convertors
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	40	V
I _D	drain current	$T_{mb} = 25 ^{\circ}C; V_{GS} = 10 V; \text{see } \underline{\text{Figure 1}}$	[1]	-	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	148	W
Tj	junction temperature			-55	-	175	°C
Static cha	racteristics						
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; see <u>Figure 13</u> ; see <u>Figure 5</u>		-	5.5	6.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 5</u>		-	3.79	4.5	mΩ
Dynamic (characteristics						
Q_GD	gate-drain charge	$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $V_{DS} = 20 \text{ V}$; see Figure 14; see Figure 15		-	8.8	-	nC
Q _{G(tot)}	total gate charge	$V_{GS} = 10 \text{ V}; I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}$		-	35	-	nC
Avalanche	ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 40 V; unclamped; R_{GS} = 50 Ω		-	-	152	mJ

[1] Continuous current is limited by package



2. Pinning information

Table 2. Pinning information

	-			
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain[1]	mb	D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

^[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R5-40BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R5-40BS	PSMN4R5-40BS

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	40	V
V_{DGR}	drain-gate voltage	$T_j \ge 25$ °C; $T_j \le 175$ °C; $R_{GS} = 20$ kΩ		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see <u>Figure 1</u>	<u>[1]</u>	-	96	Α
		V _{GS} = 10 V; T _{mb} = 25 °C; see <u>Figure 1</u>	<u>[1]</u>	-	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 3		-	545	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	148	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-dra	ain diode					
Is	source current	T _{mb} = 25 °C	<u>[1]</u>	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	545	Α
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 40 V; unclamped; R_{GS} = 50 Ω		-	152	mJ

[1] Continuous current is limited by package

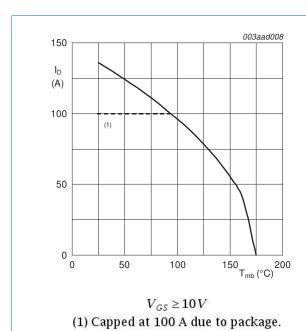


Fig 1. Continuous drain current as a function of mounting base temperature

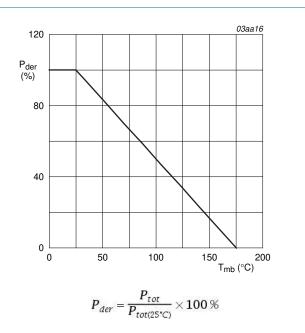


Fig 2. Normalized total power dissipation as a function of mounting base temperature

PSMN4R5-40BS

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3 of 15

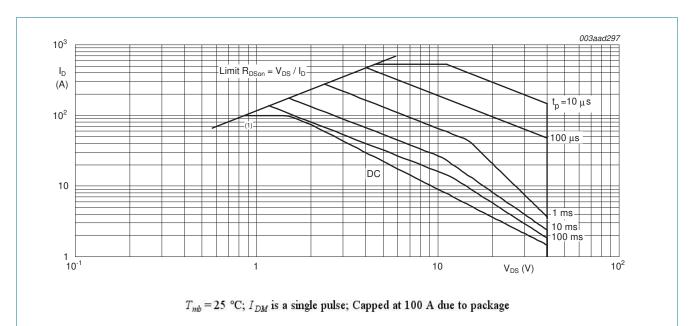


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.65	1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

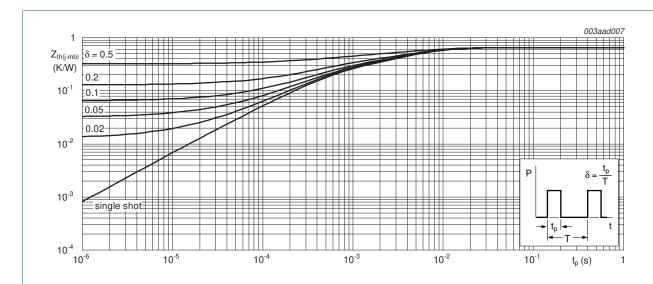


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	40	-	-	V
$V_{GS(th)}$ gate-source threshold volt	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ °C}$; see Figure 11; see Figure 12	-	-	4.6	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; see Figure 11; see Figure 12	1	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see Figure 11; see Figure 12	2	3	4	V
I _{DSS} drain le	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	3	μΑ
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ °C}$	-	-	60	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
R _{DSon} drai	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 13; see Figure 5	-	7.41	8.7	Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ °C};$ see Figure 13; see Figure 5	-	5.5	6.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 5	-	3.79	4.5	mΩ
R _G	internal gate resistance (AC)	f = 1 MHz	-	0.97	-	Ω
Dynamic c	haracteristics					
Q _{G(tot)}	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	35	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V};$	-	42.3	-	nC
Q _{GS}	gate-source charge	see Figure 14; see Figure 15	-	13.8	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	7.9	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	5.9	-	nC
Q_{GD}	gate-drain charge		-	8.8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 20 \text{ V}$; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	4.8	-	V
C _{iss}	input capacitance	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	2683	-	рF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	660	-	pF
C _{rss}	reverse transfer capacitance		-	290	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 10 \text{ V};$	-	19	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	23	-	ns
t _{d(off)}	turn-off delay time		-	30	-	ns
t _f	fall time		-	9	-	ns

6 of 15

 Table 7.
 Characteristics ...continued

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-dra	ain diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 17	-	0.75	1.2	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; \ V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}$	-	40	-	ns
Q _r	recovered charge	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$ $V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 \text{ °C}$	-	33	-	nC

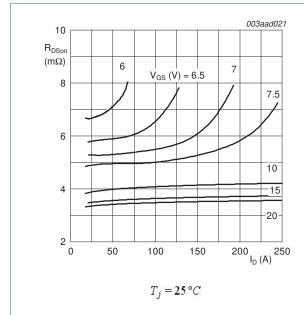


Fig 5. Drain-source on-state resistance as a function of drain current; typical values

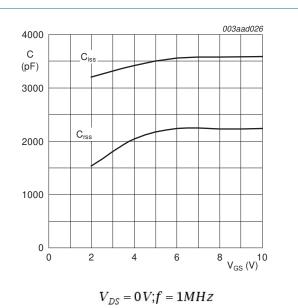


Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

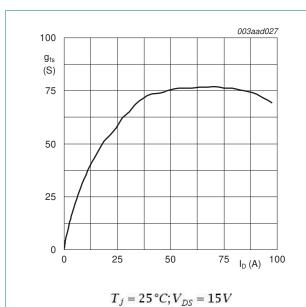


Fig 7. Forward transconductance as a function of drain current; typical values

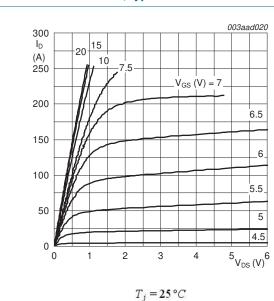
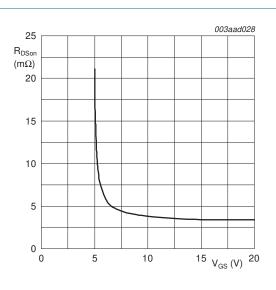
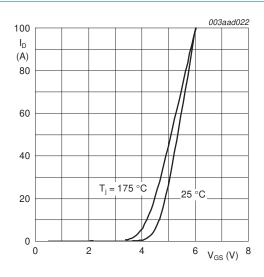


Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



 $T_j = 25 \,^{\circ}C; I_D = 25A$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $V_{DS} > I_D \times R_{DSon}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

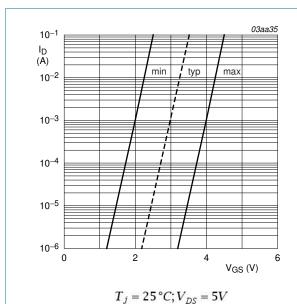


Fig 11. Sub-threshold drain current as a function of gate-source voltage

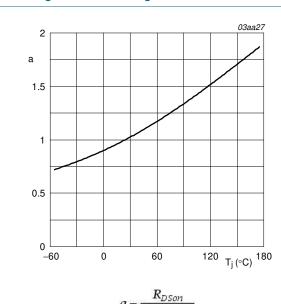
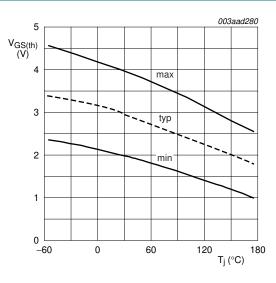


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



 $I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature

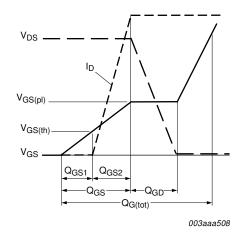


Fig 14. Gate charge waveform definitions

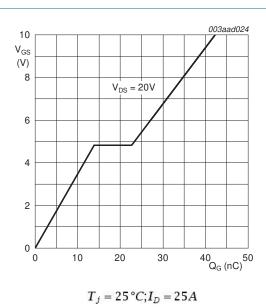
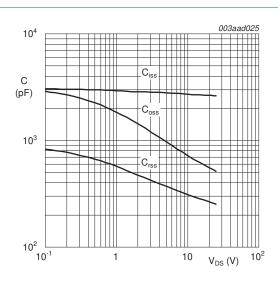


Fig 15. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

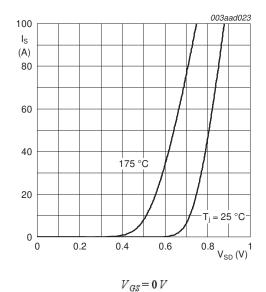


Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

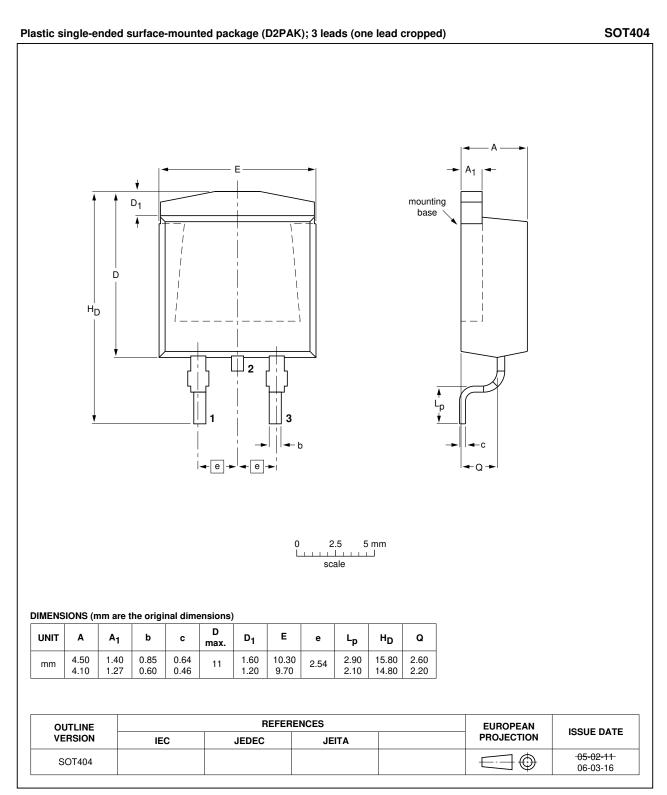


Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R5-40BS v.1	20120322	Product data sheet	-	-

10. Legal information

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Document status[1] [2]	Product status[3]	Definition
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Product [short] data sheet	Production	This document contains the product specification.

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PSMN4R5-40BS

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PSMN4R5-40BS

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12. Contents

1	Product profile
1.1	General description
1.2	Features and benefits
1.3	Applications
1.4	Quick reference data
2	Pinning information
3	Ordering information
4	Marking
5	Limiting values
6	Thermal characteristics
7	Characteristics
8	Package outline
9	Revision history12
10	Legal information1
10.1	Data sheet status
10.2	Definitions13
10.3	Disclaimers
10.4	Trademarks14
11	Contact information 1/