

# PHP112N06T; PHB112N06T

N-channel enhancement mode field-effect transistor

Rev. 01 — 07 March 2001

Product specification

## 1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™<sup>1</sup> technology.

Product availability:

PHP112N06T in SOT78 (TO-220AB)

PHB112N06T in SOT404 (D<sup>2</sup>-PAK).

## 2. Features

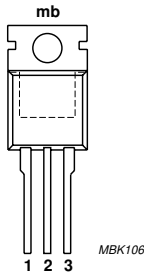
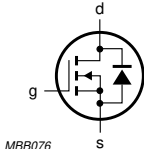
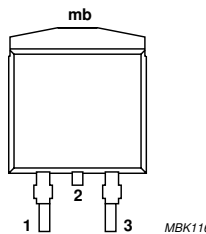
- Fast switching
- Very low on-state resistance.

## 3. Applications

- General purpose switching
- Switched mode power supplies.

## 4. Pinning information

Table 1: Pinning - SOT78 and SOT404, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) <sup>[1]</sup>		
3	source (s)		
mb	mounting base; connected to drain (d)	 MBK116	
		<b>SOT78 (TO-220AB)</b>	<b>SOT404 (D<sup>2</sup>-PAK)</b>

[1] It is not possible to make connection to pin 2 of the SOT404 package.

1. TrenchMOS is a trademark of Royal Philips Electronics.

## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $175$ °C	–	55	V
$I_D$	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V	–	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C	–	200	W
$T_j$	junction temperature		–	175	°C
$R_{DS(on)}$	drain-source on-state resistance	$T_j = 25$ °C; $V_{GS} = 10$ V; $I_D = 25$ A	7.2	8	mΩ

## 6. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

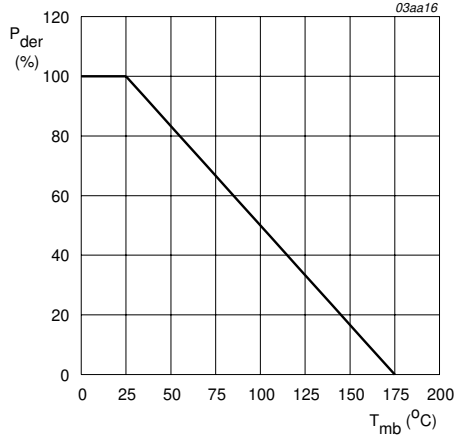
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $175$ °C	–	55	V
$V_{DGR}$	drain-gate voltage (DC)	$T_j = 25$ to $175$ °C; $R_{GS} = 20$ kΩ	–	55	V
$V_{GS}$	gate-source voltage (DC)		–	±20	V
$I_D$	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V Figure 2 and 3	–	75	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V Figure 2 and 3	–	52.5	A
$I_{DM}$	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	400	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C; Figure 1	–	200	W
$T_{stg}$	storage temperature		–55	175	°C
$T_j$	operating junction temperature		–55	175	°C

### Source-drain diode

$I_S$	source (diode forward) current (DC)	$T_{mb} = 25$ °C	–	75	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	400	A

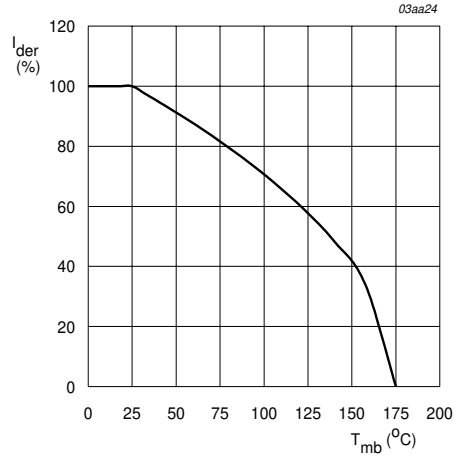
### Avalanche ruggedness

$E_{AS}$	non-repetitive avalanche energy	unclamped inductive load; $I_{AS} = 60$ A; $t_p = 0.1$ ms; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; starting $T_j = 25$ °C; Figure 4	–	360	mJ
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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

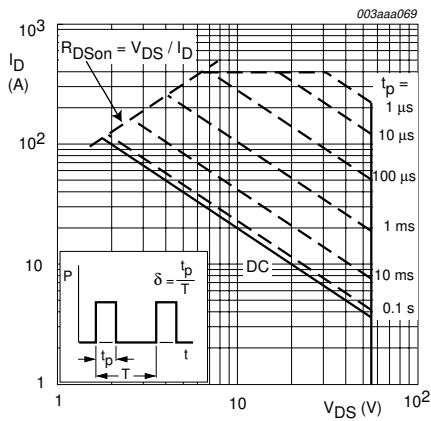
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 10 \text{ V}$$

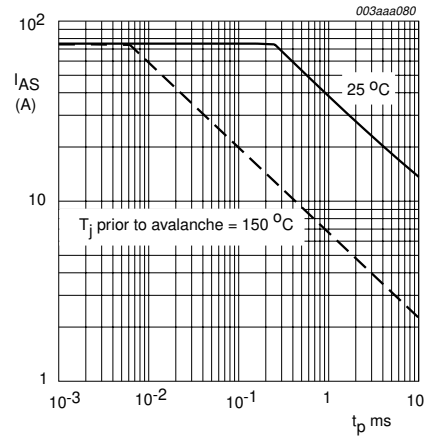
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Unclamped inductive load; V<sub>DD</sub> ≤ 15 V; R<sub>GS</sub> = 50 Ω; V<sub>GS</sub> = 5 V; starting T<sub>j</sub> = 25 °C and 150 °C.

Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 5	0.75	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOT78 package; vertical in still air	60	K/W
		SOT404 package; mounted on printed circuit board; minimum footprint.	50	K/W

### 7.1 Transient thermal impedance

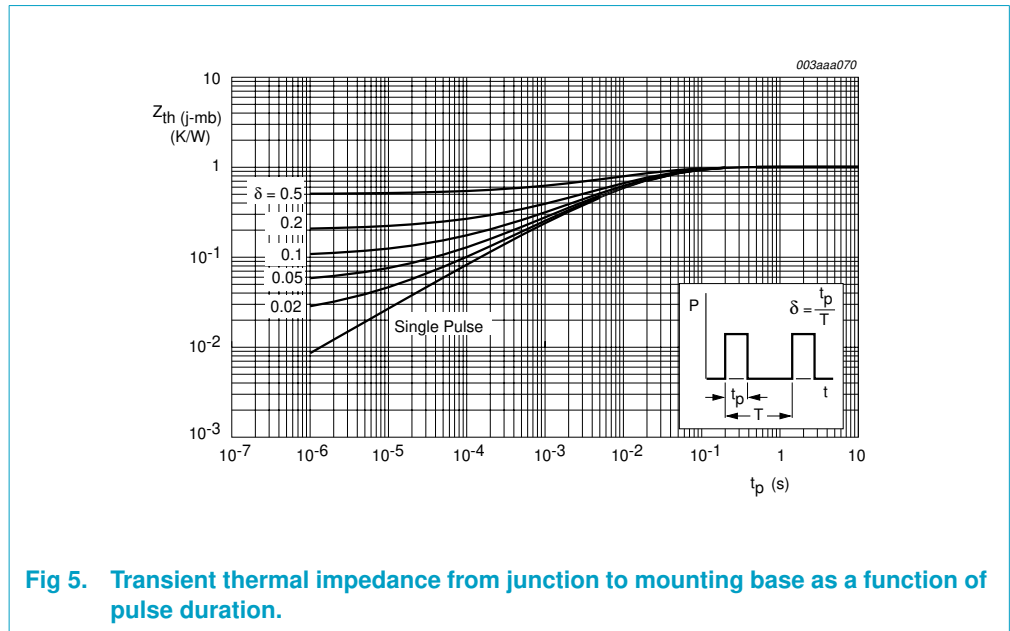
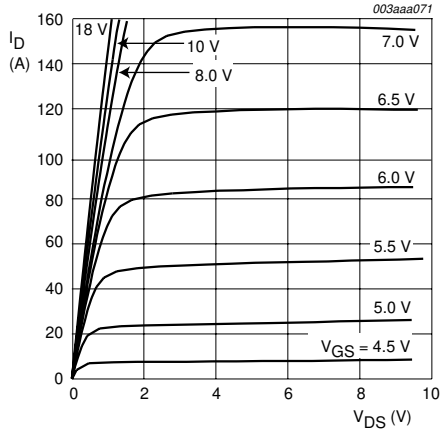


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 8. Characteristics

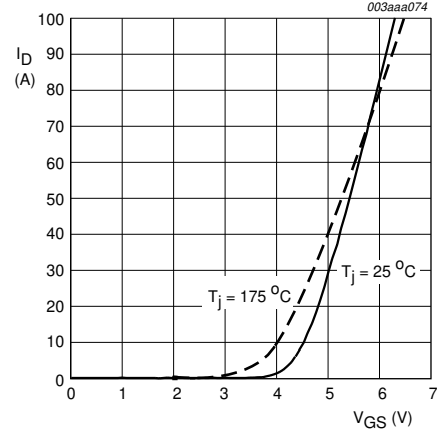
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V	55	–	–	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; Figure 10				
		T <sub>j</sub> = 25 °C	2.0	3.0	4.0	V
		T <sub>j</sub> = 175 °C	1.0	–	–	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 55 V				
		T <sub>j</sub> = 25 °C	–	0.05	10	μA
		T <sub>j</sub> = 175 °C	–	–	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>DS</sub> = 0 V; V <sub>GS</sub> = ±20 V	–	2	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; Figure 8 and 9				
		T <sub>j</sub> = 25 °C	–	7.2	8.0	mΩ
		T <sub>j</sub> = 175 °C	–	–	16	mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 50 A; V <sub>DD</sub> = 44 V;	–	87	–	nC
Q <sub>gs</sub>	gate-source charge	V <sub>GS</sub> = 10 V; Figure 15	–	24	–	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		–	29		nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V;	–	3264	4352	pF
C <sub>oss</sub>	output capacitance	f = 1 MHz; Figure 13	–	720	863	pF
C <sub>rss</sub>	reverse transfer capacitance		–	389	533	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 30 V; R <sub>D</sub> = 1.2 Ω;	–	24	36	ns
t <sub>r</sub>	rise time	V <sub>GS</sub> = 5 V; R <sub>G</sub> = 10 Ω	–	94	141	ns
t <sub>d(off)</sub>	turn-off delay time		–	100	140	ns
t <sub>f</sub>	fall time		–	80	112	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; Figure 14	–	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 75 A;	–	65	–	ns
Q <sub>r</sub>	recovered charge	dI <sub>S</sub> /dt = –100 A/μs; V <sub>GS</sub> = –10 V; V <sub>R</sub> = 30 V	–	0.17	–	μC



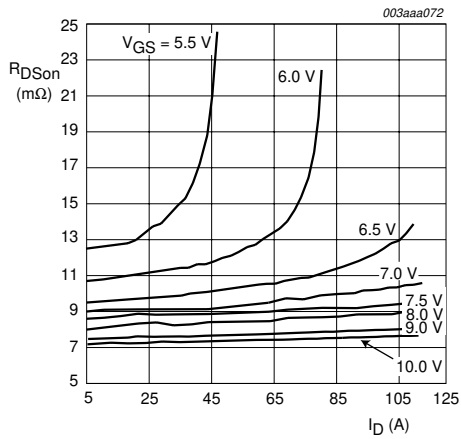
$T_j = 25\text{ }^\circ\text{C}$

**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.**



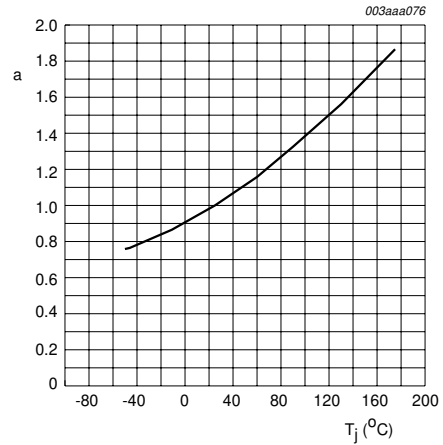
$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



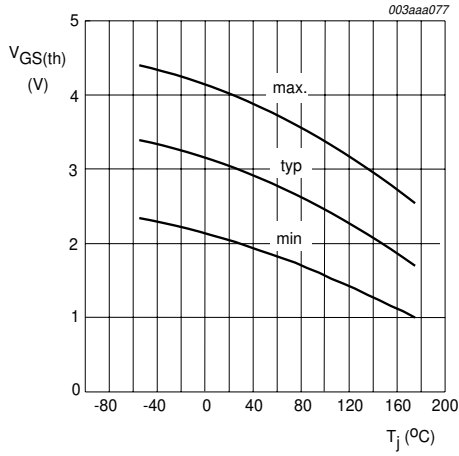
$T_j = 25\text{ }^\circ\text{C}$

**Fig 8. Drain-source on-state resistance as a function of drain current; typical values.**



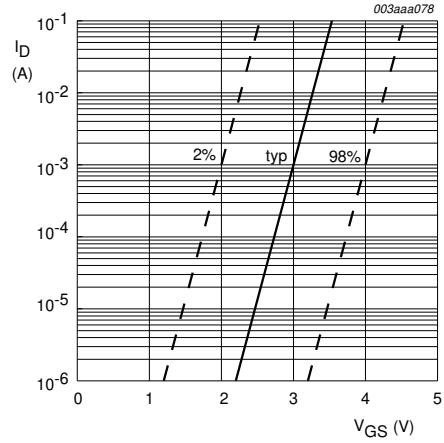
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.**



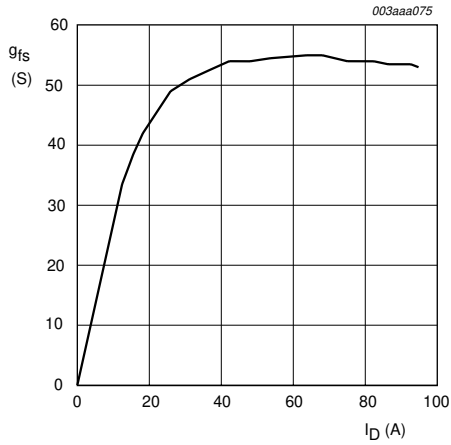
$I_D = 1 \text{ mA}$ ;  $V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature.



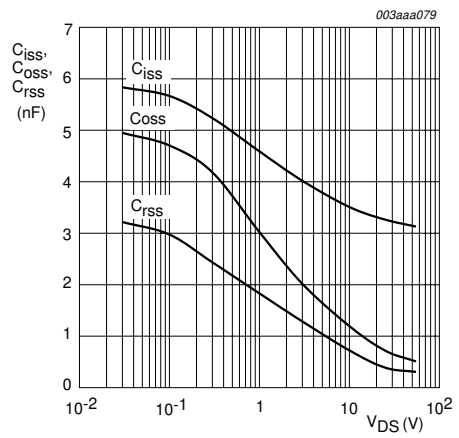
$T_j = 25 \text{ }^{\circ}C$

Fig 11. Sub-threshold drain current as a function of gate-source voltage.



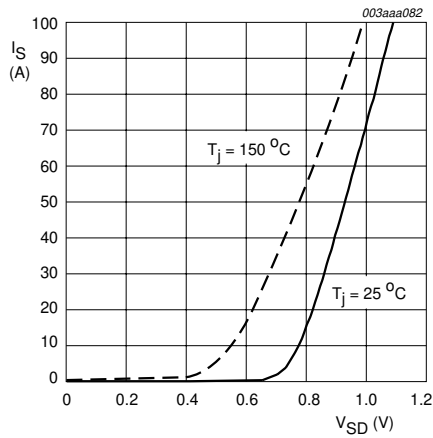
$T_j = 25 \text{ }^{\circ}C$ ;  $V_{DS} = 25 \text{ V}$

Fig 12. Forward transconductance as a function of drain current; typical values.



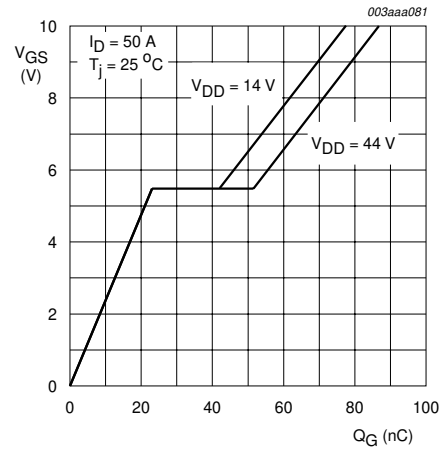
$V_{GS} = 0 \text{ V}$ ;  $f = 1 \text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 50\text{ A}$ ;  $V_{DD} = 14\text{ V}$  and  $44\text{ V}$

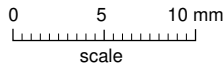
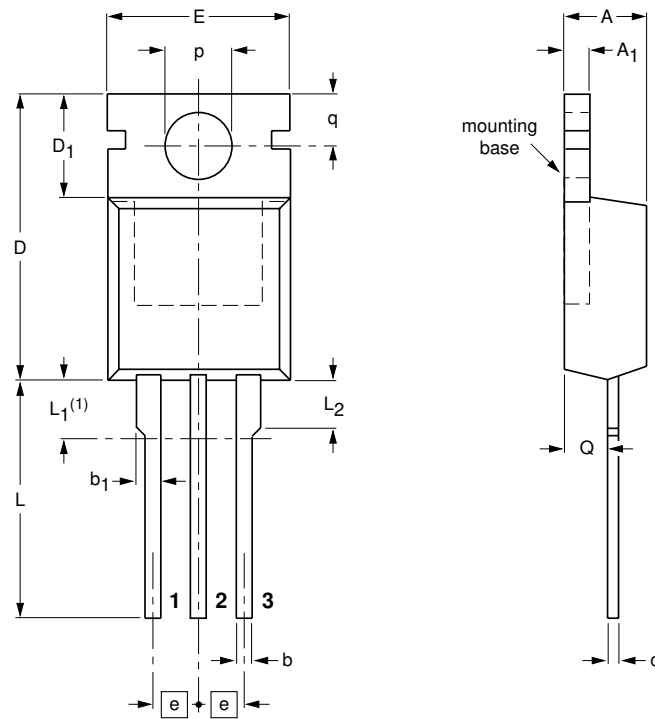
**Fig 15. Gate-source voltage as a function of gate charge; typical values.**



9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub> <sup>(1)</sup>	L <sub>2</sub> max.	p	q	Q
mm	4.5	1.39	0.9	1.3	0.7	15.8	6.4	10.3	2.54	15.0	3.30	3.0	3.8	3.0	2.6
	4.1	1.27	0.7	1.0	0.4	15.2	5.9	9.7		13.5	2.79		3.6	2.7	2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			00-09-07- 01-02-16

Fig 16. SOT78

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404

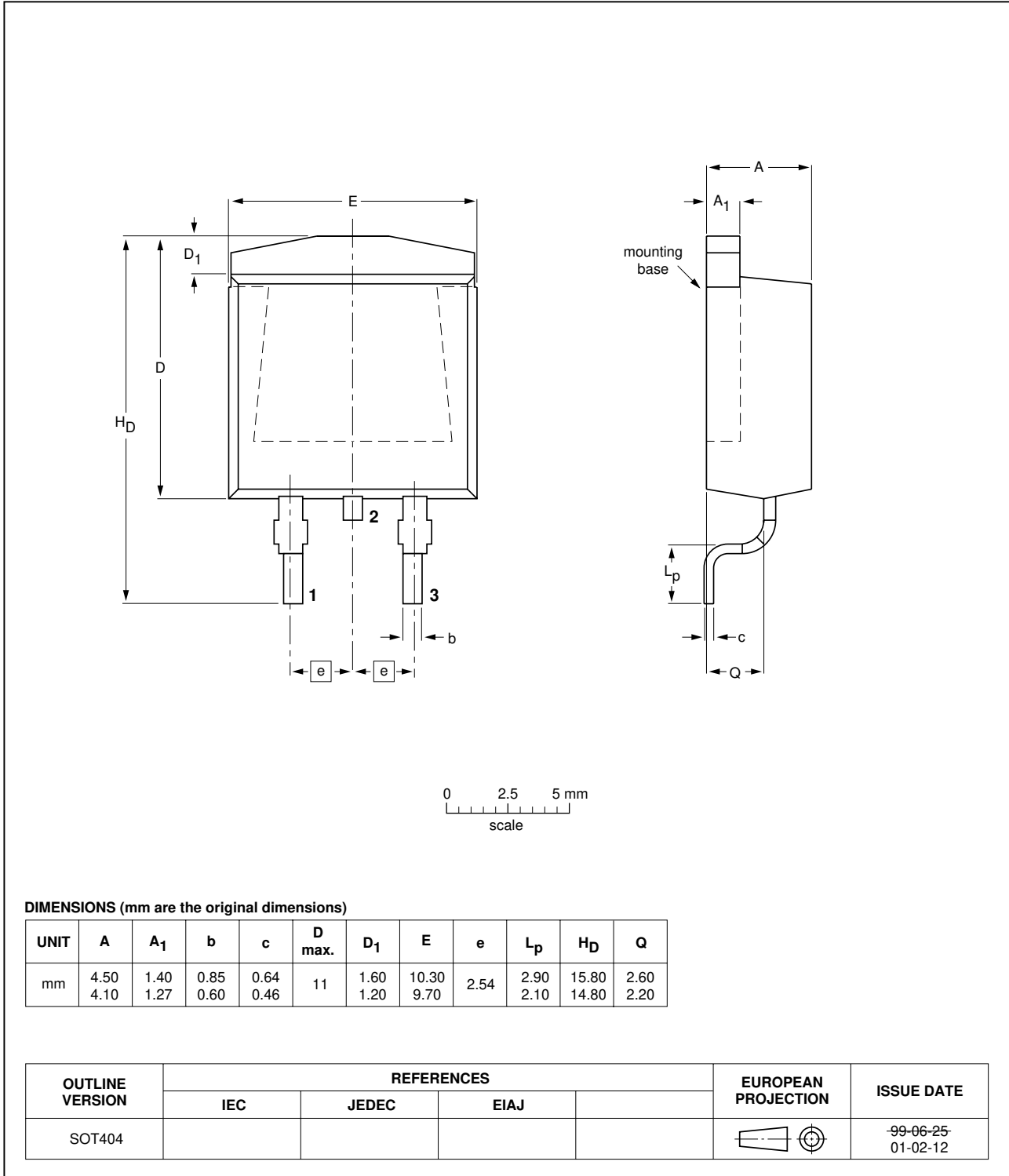


Fig 17. SOT404 (D<sup>2</sup>-PAK).

## 10. Revision history

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Table 6: Revision history

Rev	Date	CPCN	Description
01	20010307	-	Product specification. Initial version.

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## 11. Data sheet status

Datasheet status	Product status	Definition <sup>[1]</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

## 12. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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(SCA71)

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