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**FDMC2610** 

## **July 2016**

# N-Channel UltraFET Trench<sup>®</sup> MOSFET 200V, 9.5A, 200m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 200m $\Omega$  at  $V_{GS}$  = 10V,  $I_D$  = 2.2A
- Max  $r_{DS(on)}$  = 215m $\Omega$  at  $V_{GS}$  = 6V,  $I_D$  = 1.5A
- Low Profile 1mm Max in a Power 33
- RoHS Compliant

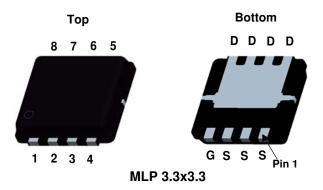


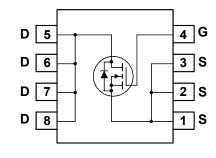
#### **General Description**

This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications.

## **Application**

■ DC - DC Conversion





## **MOSFET Maximum Ratings** $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter			Ratings	Units
$V_{DS}$	Drain to Source Voltage			200	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous (Silicon limited)	T <sub>C</sub> = 25°C		9.5	
I <sub>D</sub>	-Continuous	T <sub>A</sub> = 25°C	(Note 1a)	2.2	Α
	-Pulsed			15	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	6	mJ
В	Power Dissipation	T <sub>C</sub> = 25°C		42	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25°C	(Note 1a)	2.1	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature R	ange		-55 to +150	°C

#### **Thermal Characteristics**

$R_{ heta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC2610	FDMC2610	MLP 3.3x3.3	13 "	12 mm	3000 units

## **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	200			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		199		mV/°C
I <sub>DSS</sub> Zero Gate Voltage Drain Current	V <sub>DS</sub> = 160V,			1	μА	
	Zero Gate Voltage Drain Gurrent	$V_{GS} = 0V$ $T_J = 125^{\circ}C$			100	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		-9.9		mV/°C
r <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.2A		175	200	
		$V_{GS} = 6V, I_D = 1.5A$		188	215	mΩ
		$V_{GS} = 10V$ , $I_D = 2.2A$ , $T_J = 125$ °C		347	397	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5V, I_{D} = 2.2A$		7		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, f = 1MHz	720	960	pF
C <sub>oss</sub>	Output Capacitance		41	55	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		12	20	pF
$R_g$	Gate Resistance	f = 1MHz	0.7		Ω

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		17	31	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 100V, I_{D} = 2.2A$ $V_{GS} = 10V, R_{GEN} = 24\Omega$	13	24	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		29	47	ns
t <sub>f</sub>	Fall Time		16	29	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V$ $V_{DD} = 100V$	12.3	18	nC
$Q_{gs}$	Gate to Source Gate Charge	I <sub>D</sub> = 2.2A	3		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		3.6		nC

#### **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2.2A (Note 2)	0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 2.2A, di/dt = 100A/μs	69	104	ns
$Q_{rr}$	Reverse Recovery Charge		114	171	nC

#### Notes:

Notes: 1.  $R_{\theta JA}$  is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $60^{\circ}$ C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 135°C/W when mounted on a minimum pad of 2 oz copper

- 2: Pulse Test: Pulse Width < 300 $\mu$ s, Duty cycle < 2.0%.
- 3. Starting T  $_J$  = 25 °C; N-ch: L = 3 mH, I  $_{AS}$  = 2 A, V  $_{DD}$  = 200 V, V  $_{GS}$  = 10 V.

## **Typical Characteristics** T<sub>J</sub> = 25°C unless otherwise noted.

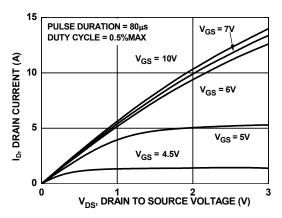


Figure 1. On-Region Characteristics

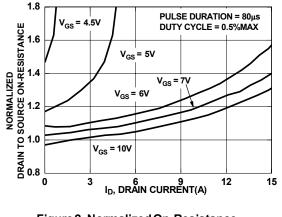


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

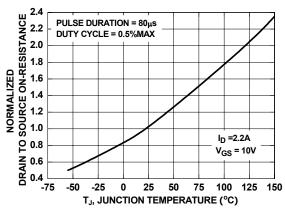


Figure 3. Normalized On-Resistance vs Junction Temperature

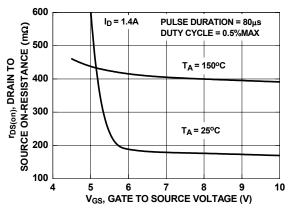


Figure 4. On-Resistance vs Gate to Source Voltage

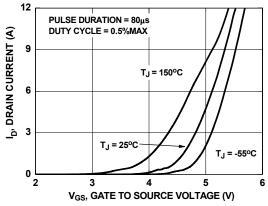


Figure 5. Transfer Characteristics

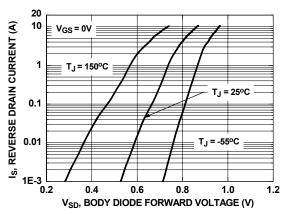


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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### **Typical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted.

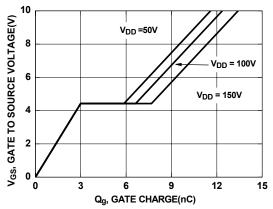


Figure 7. Gate Charge Characteristics

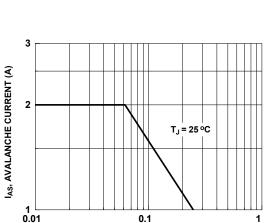


Figure 9. Unclamped Inductive **Switching Capability** 

0.1

t<sub>AV</sub>, TIME IN AVALANCHE (ms)

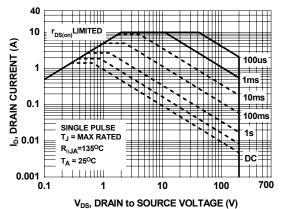


Figure 11. Forward Bias Safe **Operating Area** 

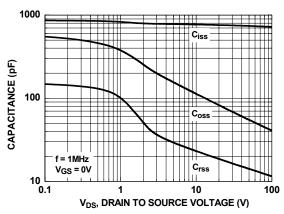


Figure 8. Capacitance vs Drain to Source Voltage

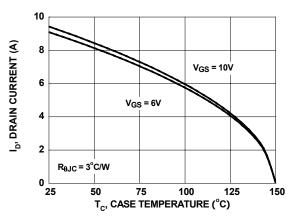


Figure 10. Maximum Continuous Drain **Current vs Case Temperature** 

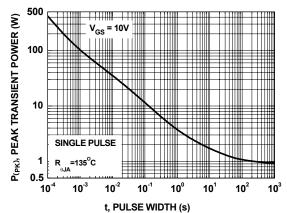


Figure 12. Single Pulse Maximum **Power Dissipation** 

## **Typical Characteristics** T<sub>J</sub> = 25°C unless otherwise noted.

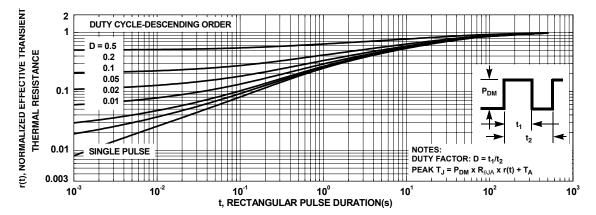
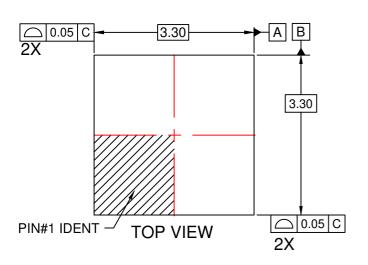
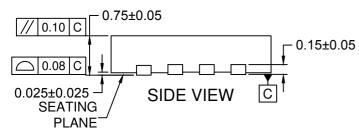
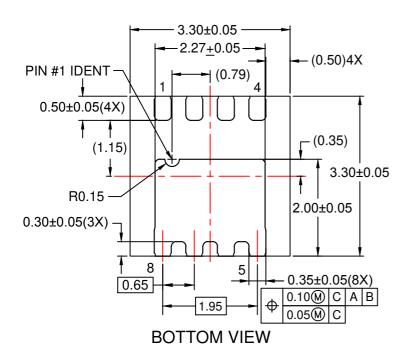
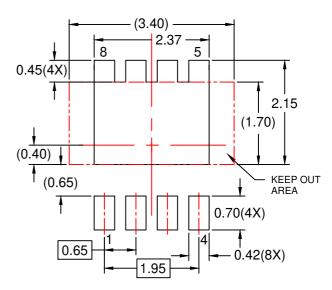


Figure 13. Transient Thermal Response Curve









RECOMMENDED LAND PATTERN

#### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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