

FDMC8010DC

MOSFET – N-Channel, DUAL COOL[®] 33, POWERTRENCH[®] 30 V, 157 A, 1.28 mΩ



ON Semiconductor[®]

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General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Features

- DUAL COOL Top Side Cooling PQFN Package
- Max $r_{DS(on)}$ = 1.28 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 37\text{ A}$
- Max $r_{DS(on)}$ = 1.74 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 32\text{ A}$
- High Performance Technology for Extremely Low $r_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Load Switch
- Motor Bridge Switch
- Synchronous Rectifier

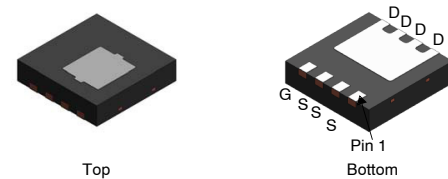
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	± 20	V
I_D	Drain Current		A
	–Continuous $T_C = 25^\circ\text{C}$ (Note 6)	157	
	–Continuous $T_C = 100^\circ\text{C}$ (Note 6)	99	
	–Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	37	
	–Pulsed (Note 5)	788	
EAS	Single Pulse Avalanche Energy (Note 3)	337	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	50	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

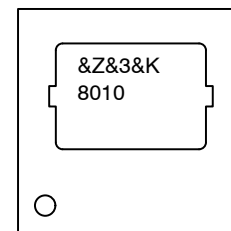
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	

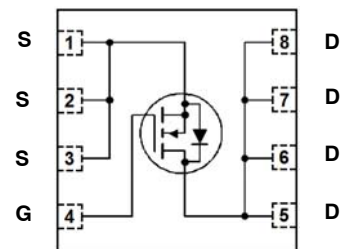


PQFN8 3.3X3.3, 0.65P
CASE 483AY
DUAL COOL 33

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
8010 = Specific Device Code



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

FDMC8010DC

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8010	FDMC8010DC	DUAL COOL 33	13"	12 mm	3000 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	30			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		15		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			10	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.4	3.0	V
ΔV _{GS(th)} /ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		-5		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 37 A		0.91	1.28	mΩ
		V _{GS} = 4.5 V, I _D = 32 A		1.2	1.74	
		V _{GS} = 10 V, I _D = 37 A, T _J = 125°C		1.34	1.89	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 37 A		231		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		4720	7080	pF
C _{oss}	Output Capacitance			1540	2310	pF
C _{rss}	Reverse Transfer Capacitance			136	205	pF
R _g	Gate Resistance		0.1	0.5	1.1	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 37 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		15	26	ns
t _r	Rise Time			7	14	ns
t _{d(off)}	Turn-Off Delay Time			40	64	ns
t _f	Fall Time			5	10	ns
Q _{g(TOT)}	Total Gate Charge at 10 V	V _{DD} = 15 V I _D = 37 A		67	94	nC
Q _{g(TOT)}	Total Gate Charge at 4.5 V			32	44	nC
Q _{gs}	Total Gate Charge			10		nC
Q _{gd}	Gate to Drain "Miller" Charge			7.5		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.3 A (Note 2)		0.7	1.2	V
		V _{GS} = 0 V, I _S = 37 A (Note 2)		0.8	1.3	
t _{rr}	Reverse Recovery Time	I _F = 37 A, di/dt = 100 A/μs		55	88	ns
Q _{rr}	Reverse Recovery Charge			48	76	nC

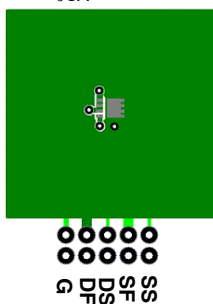
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THERMAL CHARACTERISTICS

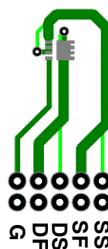
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	5.0	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	29	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	30	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	79	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	12	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	16	

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42°C/W when mounted on a 1 in² pad of 2 oz copper



b. 105°C/W when mounted on a minimum pad of 2 oz copper

- Still air, 20.9x10.4x12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper.
 - Still air, 20.9x10.4x12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper.
 - Still air, 45.2x41.4x11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper.
 - Still air, 45.2x41.4x11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper.
 - 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper.
 - 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper.
 - 200FPM Airflow, 20.9x10.4x12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper.
 - 200FPM Airflow, 20.9x10.4x12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper.
 - 200FPM Airflow, 45.2x41.4x11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper.
 - 200FPM Airflow, 45.2x41.4x11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper.
- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
 - E_{AS} of 337 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3 \text{ mH}$, $I_{AS} = 15 \text{ A}$, $V_{DD} = 30 \text{ V}$, $V_{GS} = 10 \text{ V}$, 100% test at $L = 0.1 \text{ mH}$, $I_{AS} = 49 \text{ A}$.
 - As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
 - Pulse I_d measured at 250 μs, refer to Figure 11 SOA graph for more details.
 - Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted

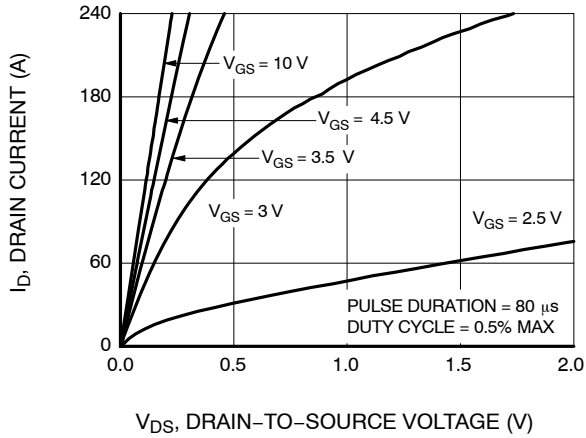


Figure 1. On-Region Characteristics

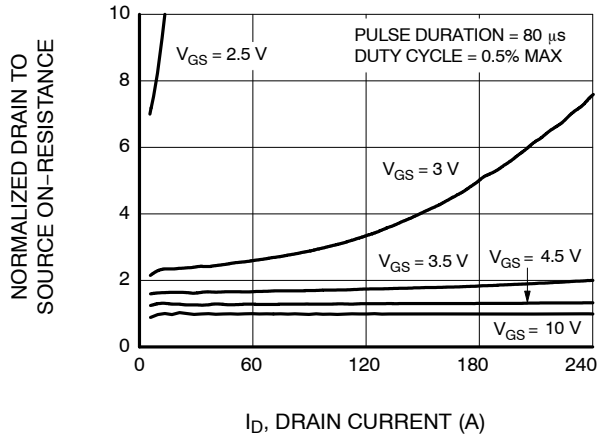


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

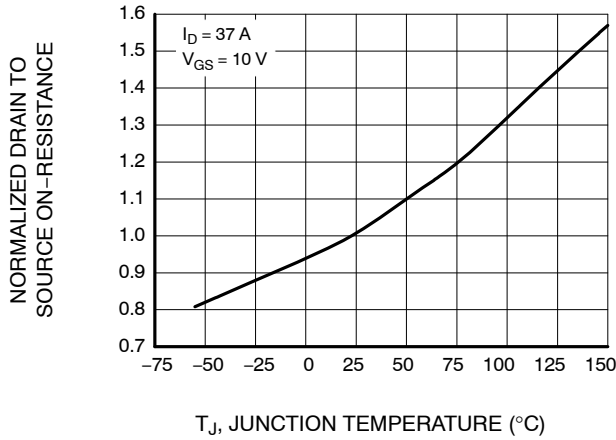


Figure 3. Normalized On Resistance vs Junction Temperature

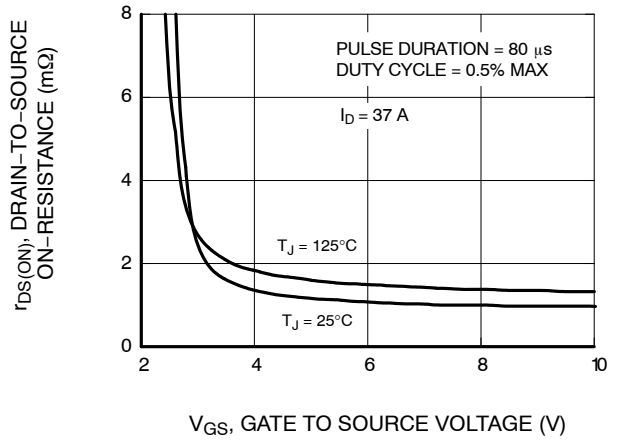


Figure 4. On-Resistance vs Gate to Source Voltage

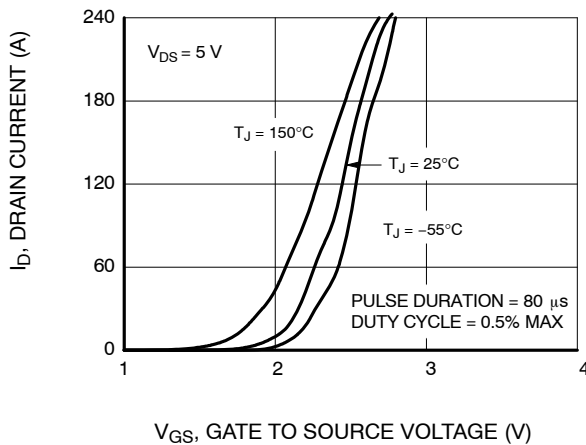


Figure 5. Transfer Characteristics

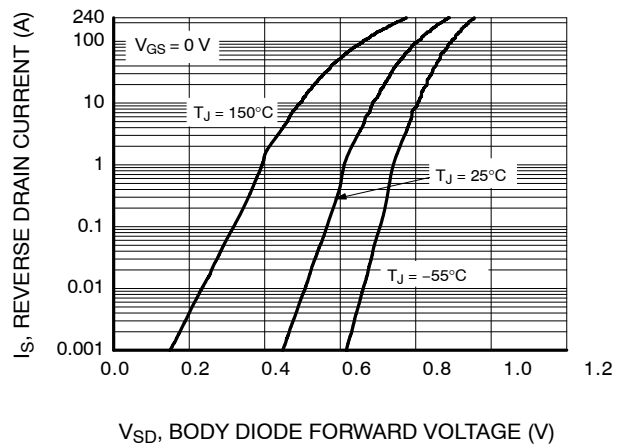


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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TYPICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted

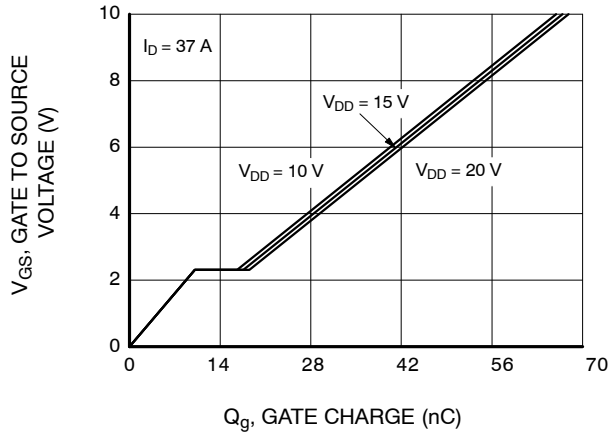


Figure 7. Gate Charge Characteristics

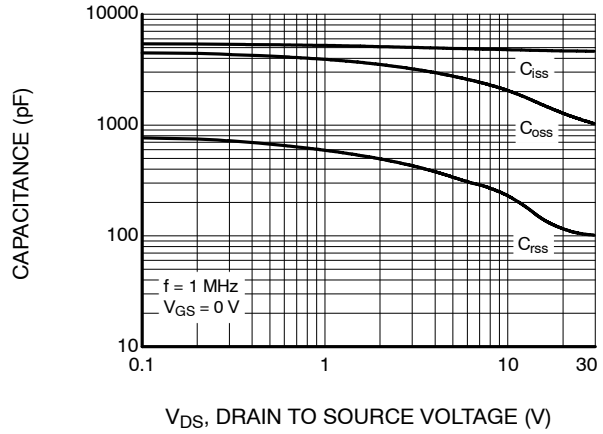


Figure 8. Capacitance vs Drain to Source Voltage

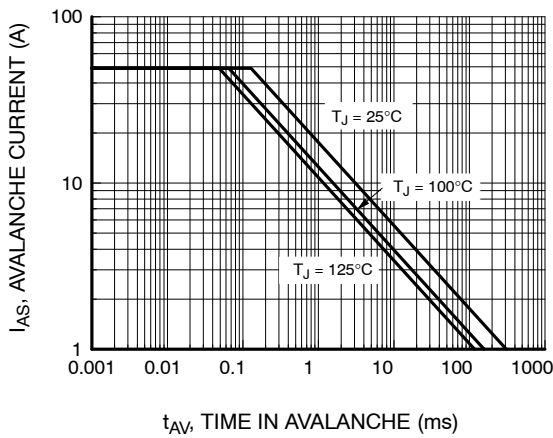


Figure 9. Unclamped Inductive Switching Capability

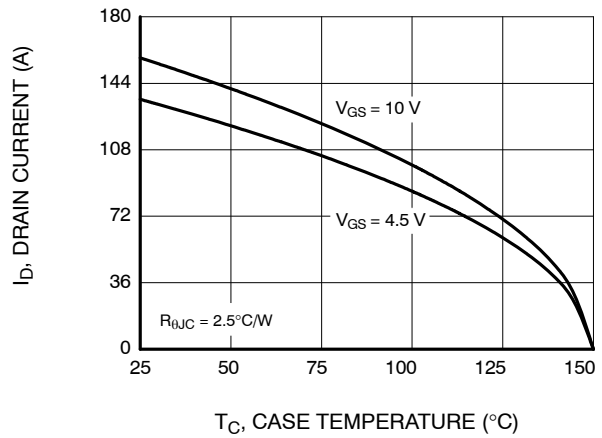


Figure 10. Maximum Continuous Drain Current vs Case Temperature

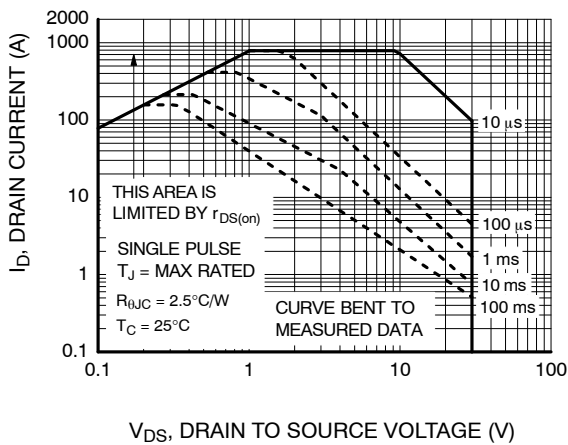


Figure 11. Forward Bias Safe Operating Area

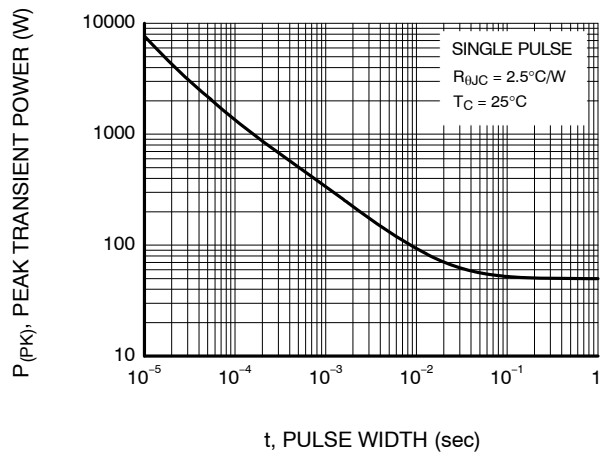
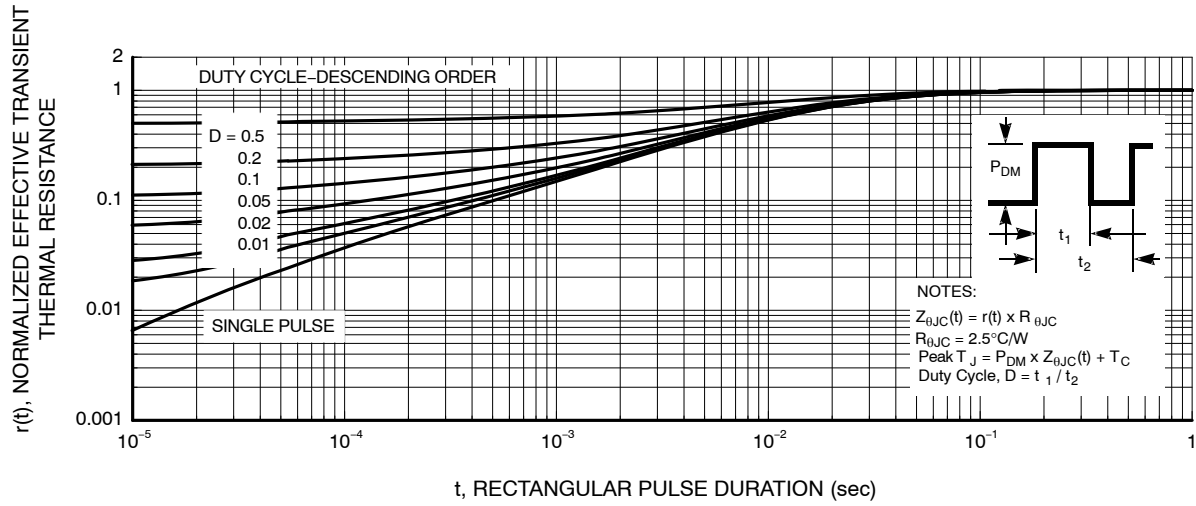


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted



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MECHANICAL CASE OUTLINE

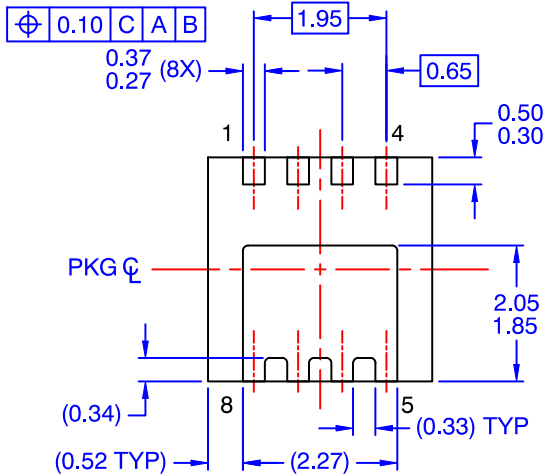
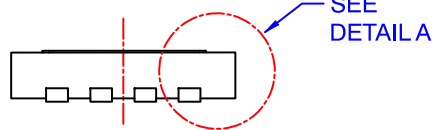
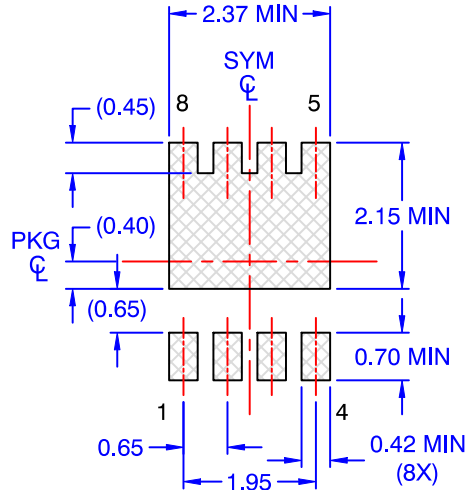
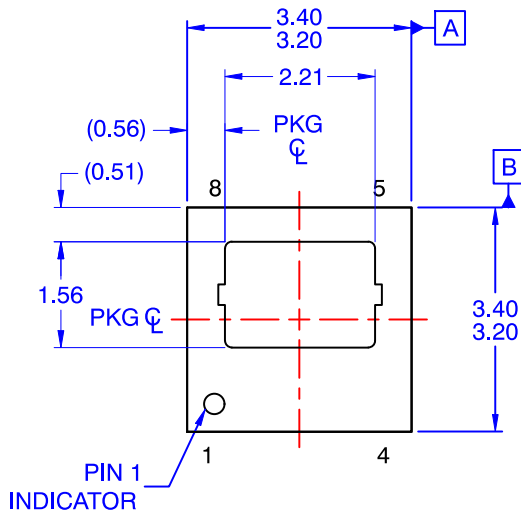
PACKAGE DIMENSIONS

ON Semiconductor®



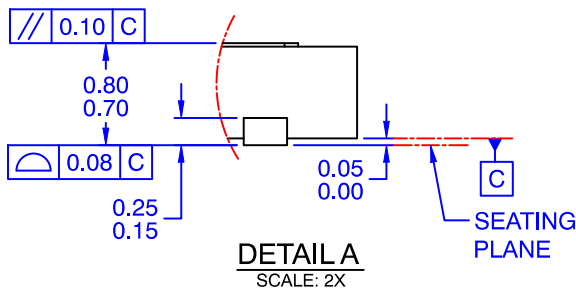
PQFN8 3.3X3.3, 0.65P
CASE 483AY
ISSUE O

DATE 30 SEP 2016



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.



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