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# FDMC86570LET60

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

60 V, 87 A, 4.3 mΩ

### Features

- Extended T<sub>J</sub> rating to 175°C
- Shielded Gate MOSFET Technology
- Max r<sub>DS(on)</sub> = 4.3 mΩ at V<sub>GS</sub> = 10 V, I<sub>D</sub> = 18 A
- Max r<sub>DS(on)</sub> = 6.5 mΩ at V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 15 A
- High performance technology for extremely low r<sub>DS(on)</sub>
- Termination is Lead-free
- RoHS Compliant

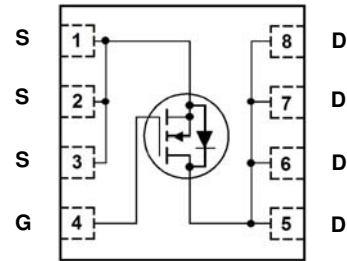
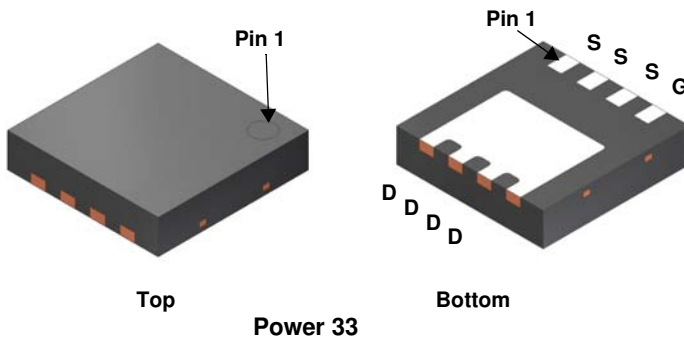


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Application

- DC-DC Conversion



### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Rated	Units
V <sub>DS</sub>	Drain to Source Voltage	60	V
V <sub>GS</sub>	Gate to Source Voltage	±20	V
I <sub>D</sub>	Drain Current -Continuous	T <sub>C</sub> = 25 °C (Note 5)	87
	-Continuous	T <sub>C</sub> = 100 °C (Note 5)	62
	-Continuous	T <sub>A</sub> = 25 °C (Note 1a)	18
	-Pulsed	(Note 4)	436
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 3)	253
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25 °C	65
	Power Dissipation	T <sub>A</sub> = 25 °C (Note 1a)	2.8
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +175	°C

### Thermal Characteristics

R <sub>θJC</sub>	Thermal Resistance, Junction to Case	(Note 1)	2.3	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86570LT	FDMC86570LET60	Power33	13 "	12 mm	3000 units

FDMC86570LET60 N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		30		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 18\text{ A}$		3.1	4.3	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 15\text{ A}$		4.7	6.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 18\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		5.0	6.9	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 18\text{ A}$		75		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		4790		pF
$C_{oss}$	Output Capacitance			821		pF
$C_{rss}$	Reverse Transfer Capacitance			19		pF
$R_g$	Gate Resistance		0.1	0.9	2.7	$\Omega$

### Switching Characteristics

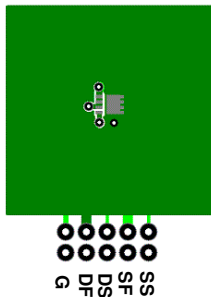
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}$ , $I_D = 18\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		19	34	ns	
$t_r$	Rise Time			6.2	12	ns	
$t_{d(off)}$	Turn-Off Delay Time			38	61	ns	
$t_f$	Fall Time			3.9	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		63	88	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 30\text{ V}$ , $I_D = 18\text{ A}$		29	41	nC
$Q_{gs}$	Gate to Source Charge				14		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				6.3		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 18\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}$ , $I_S = 1.9\text{ A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		43	69	ns
$Q_{rr}$	Reverse Recovery Charge			26	42	nC

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a. 53  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

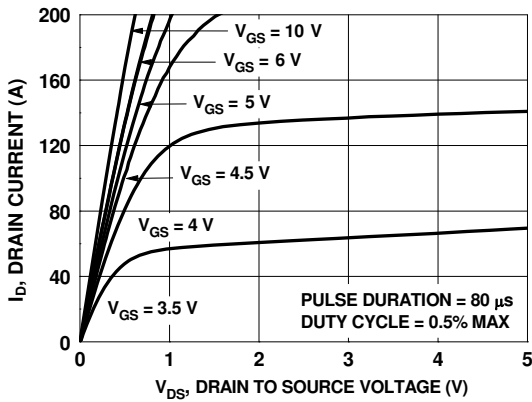
2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 253 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 13\text{ A}$ ,  $V_{DD} = 60\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 43\text{ A}$ .

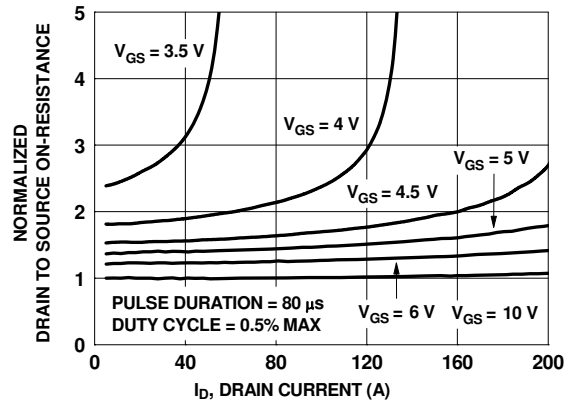
4. Pulsed  $I_D$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

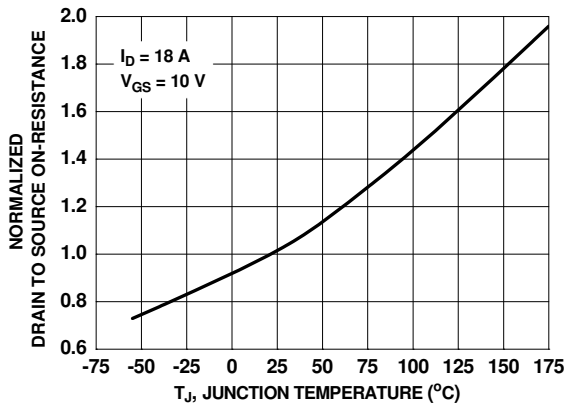
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



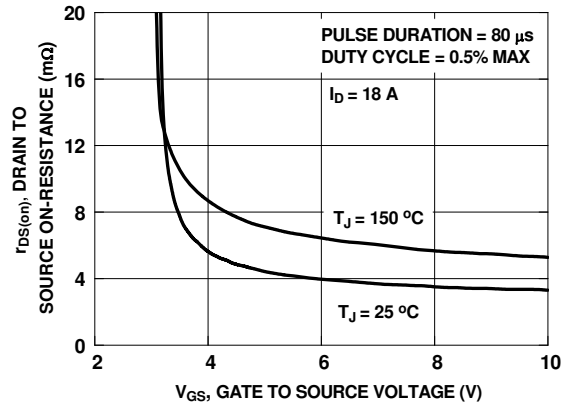
**Figure 1. On-Region Characteristics**



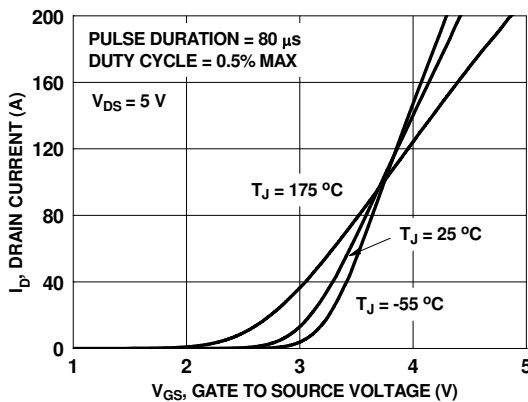
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



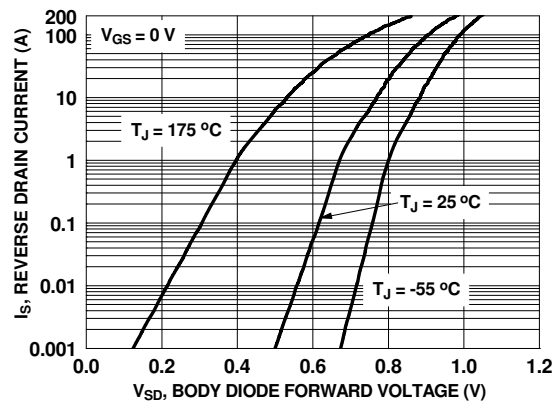
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

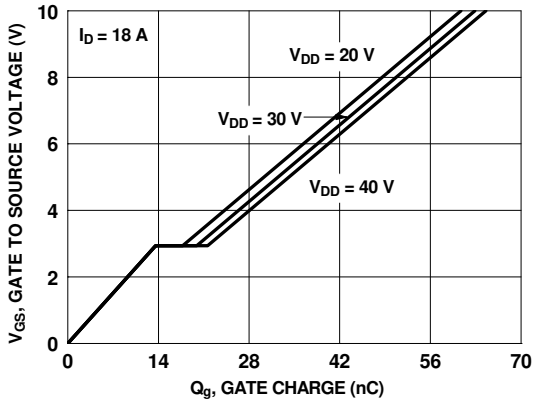


**Figure 5. Transfer Characteristics**

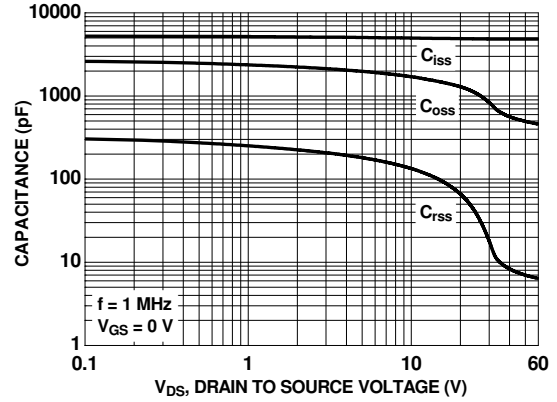


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

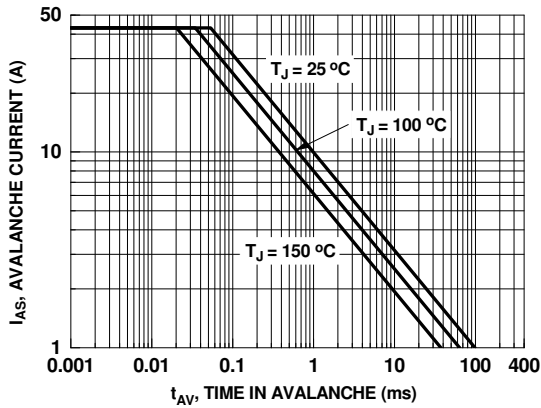
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



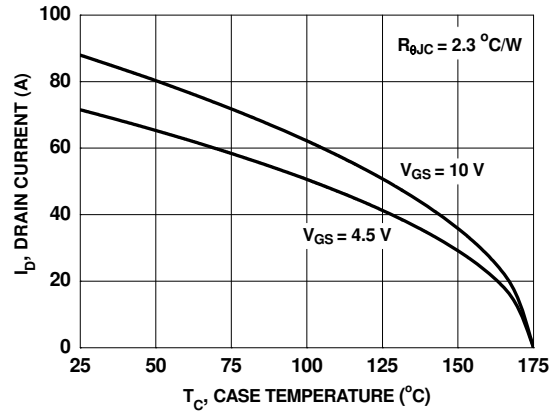
**Figure 7. Gate Charge Characteristics**



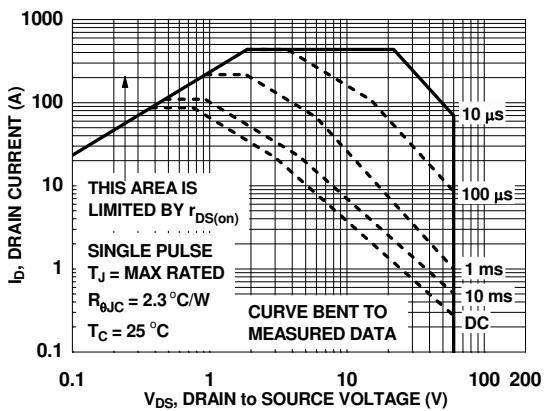
**Figure 8. Capacitance vs Drain to Source Voltage**



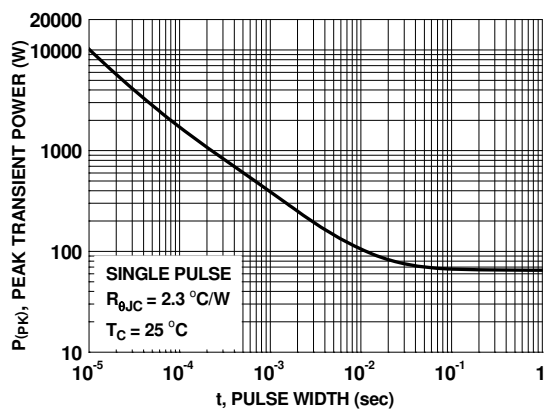
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

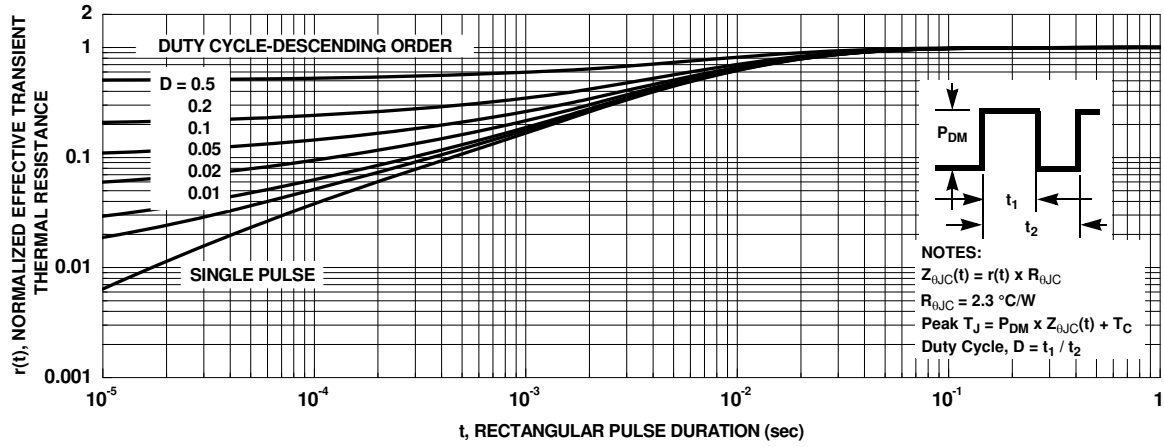


**Figure 11. Forward Bias Safe Operating Area**

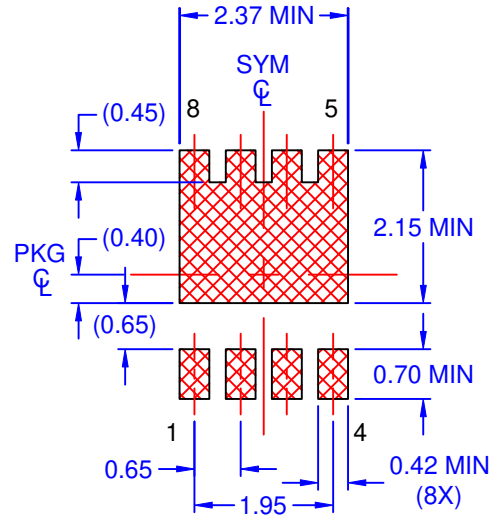
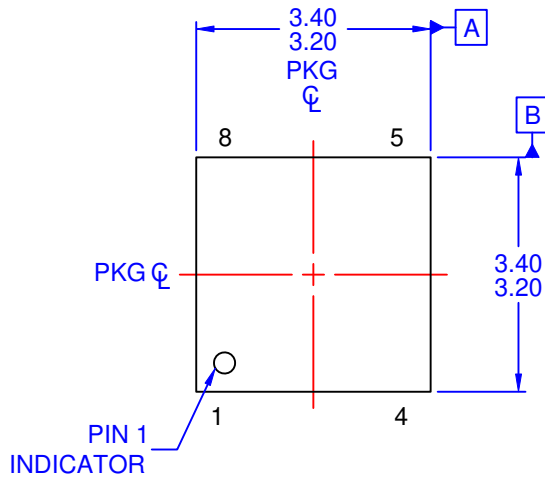


**Figure 12. Single Pulse Maximum Power Dissipation**

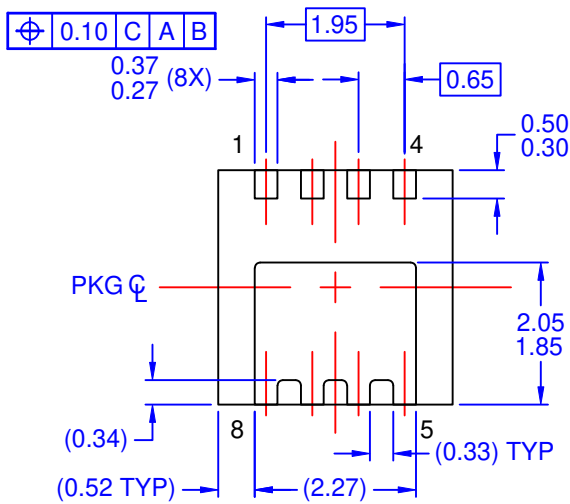
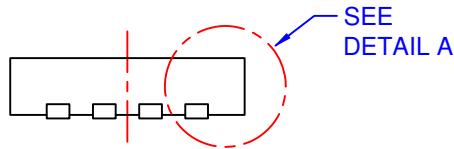
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

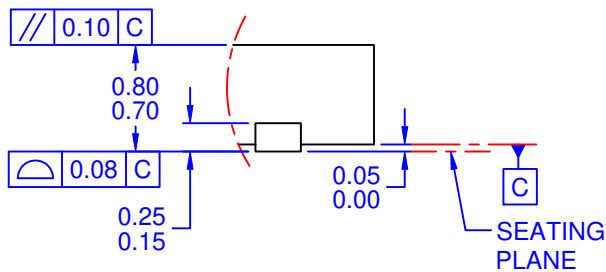


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NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08HREV1



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