

# FND361AN

## N-Channel, Logic Level, PowerTrench™

### General Description

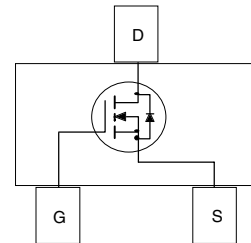
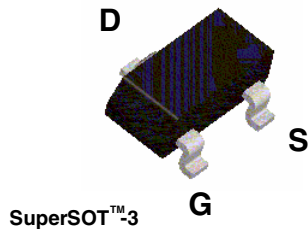
This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

### Applications

- DC/DC converter
- Load switch
- Motor drives

### Features

- 1.8 A, 30 V.  $R_{DS(on)} = 0.100 \Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(on)} = 0.150 \Omega @ V_{GS} = 4.5 \text{ V}$ .
- Low gate charge ( 2.1nC typical ).
- Fast switching speed.
- High performance trench technology for extremely low  $R_{DS(on)}$ .
- High power version of industry standard SOT-23 package. Identical pin out to SOT-23 with 30% higher power handling capability.



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	FND361AN	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage - Continuous	±20	V
I <sub>D</sub>	Drain Current - Continuous (Note 1a)	1.8	A
	- Pulsed	8	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a)	0.5	W
	(Note 1b)	0.46	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
361	FND361AN	7"	8mm	3000 units

**DMOS Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		24		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4.2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.8\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 1.8\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 1.4\text{ A}$		0.072 0.107 0.105	0.1 0.16 0.15	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	8			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 1.8\text{ A}$		5		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		220		pF
$C_{oss}$	Output Capacitance			50		pF
$C_{riss}$	Reverse Transfer Capacitance			20		pF

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6.0\ \Omega$		3	6	ns
$t$	Turn-On Rise Time			11	22	ns
$t_{d(off)}$	Turn-Off Delay Time			7	14	ns
$t_f$	Turn-Off Fall Time			3	6	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 1.8\text{ A},$ $V_{GS} = 5\text{ V}$		2.1	4	nC
$Q_{gs}$	Gate-Source Charge			0.8		nC
$Q_{gd}$	Gate-Drain Charge			0.7		nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			0.42	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note 2)		0.75	1.2	V

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $250^\circ\text{C/W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz. Cu.

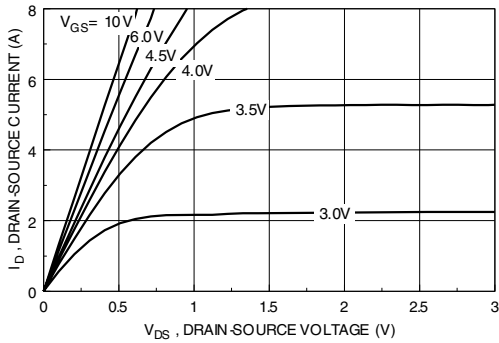


b)  $270^\circ\text{C/W}$  when mounted on a minimum pad.

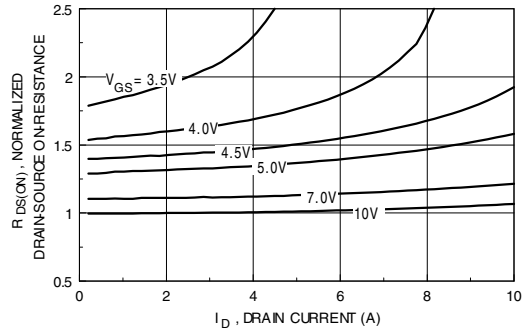
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

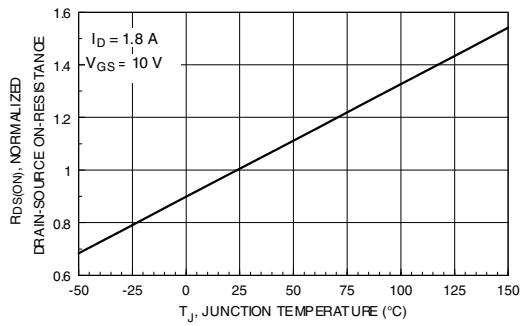
**Typical Characteristics** (continued)



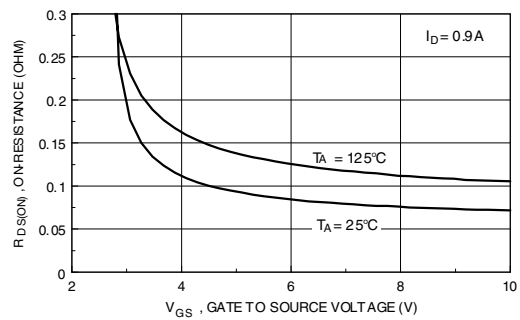
**Figure 1. On-Region Characteristics.**



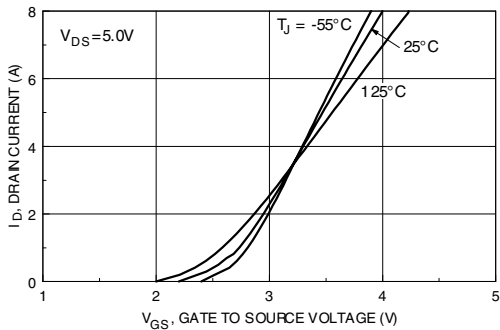
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



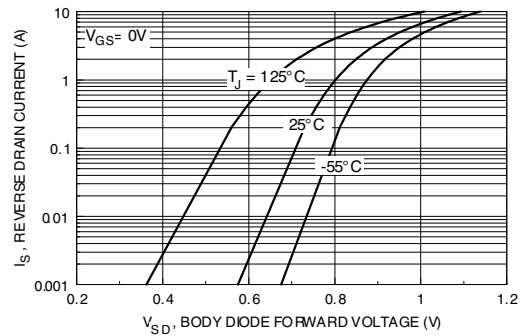
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

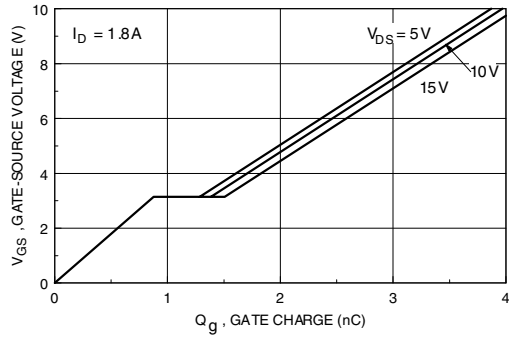


**Figure 5. Transfer Characteristics.**

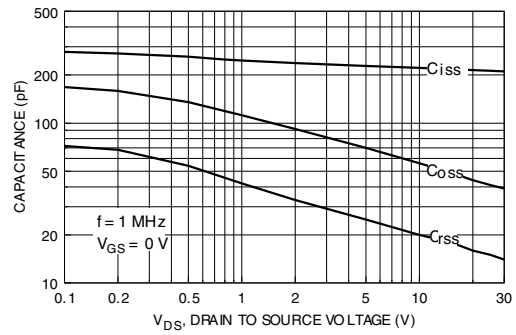


**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

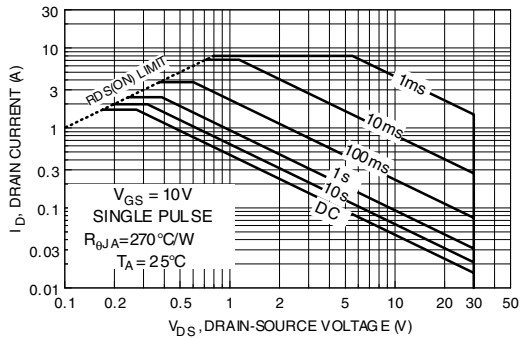
**Typical Characteristics** (continued)



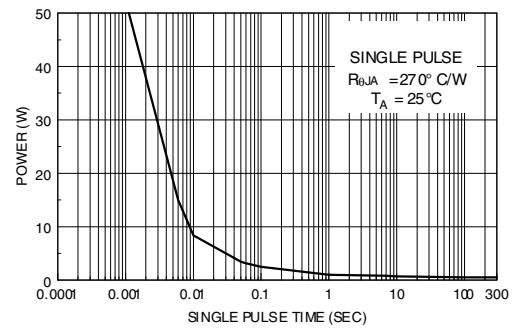
**Figure 7. Gate-Charge Characteristics.**



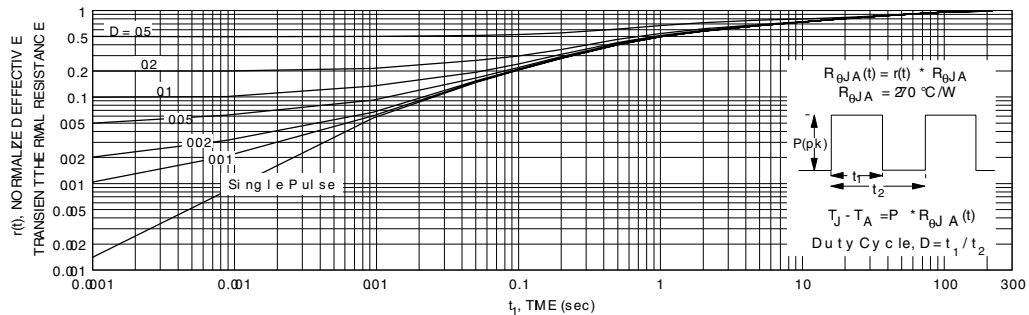
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

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FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT <sup>18</sup>	
GTO™	SuperSOT <sup>16</sup>	
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