ON Semiconductor®

FQA13N50C-F109

N-Channel QFET® MOSFET

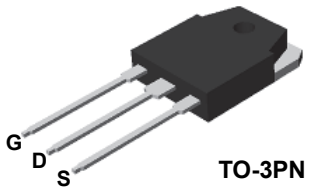
500 V, 13.5 A, 480 mΩ

Description

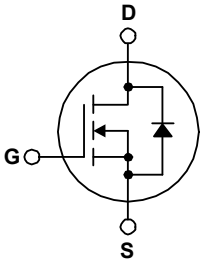
These N-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

- 13.5 A, 500 V, $R_{DS(on)}$ = 480 mΩ (Max.) @ V_{GS} = 10 V, I_D = 6.75 A
- Low Gate Charge (Typ. 43 nC)
- Low Crss (Typ. 20 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability



TO-3PN



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQA13N50C-F109	Unit
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current - Continuous (T_C = 25°C)		13.5	A
	- Continuous (T_C = 100°C)		8.5	A
I_{DM}	Drain Current - Pulsed	(Note 1)	54	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	860	mJ
I_{AR}	Avalanche Current	(Note 1)	13.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	21.8	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		218	W
	- Derate above 25°C		1.56	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.		300	°C

Thermal Characteristics

Symbol	Parameter	FQA13N50C-F109	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.58	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W

September, Rev. 3

Publication Order Number:
FQA13N50C-F109/D

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA13N50C-F109	FQA13N50C	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics

T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 6.75 A	--	0.39	0.48	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 6.75 A	--	15	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1580	2055	pF
C_{oss}	Output Capacitance		--	180	235	pF
C_{rss}	Reverse Transfer Capacitance		--	20	25	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 13.5 A, R_G = 25 Ω (Note 4)	--	25	60	ns
t_r	Turn-On Rise Time		--	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		--	130	270	ns
t_f	Turn-Off Fall Time		--	100	210	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 13.5 A, V_{GS} = 10 V (Note 4)	--	43	56	nC
Q_{gs}	Gate-Source Charge		--	7.5	--	nC
Q_{gd}	Gate-Drain Charge		--	18.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	13	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	52	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 13.5 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 13.5 A, dI_F / dt = 100 A/μs	--	410	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.5	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 5.6 mH, I_{AS} = 13.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 13.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature

Typical Characteristics

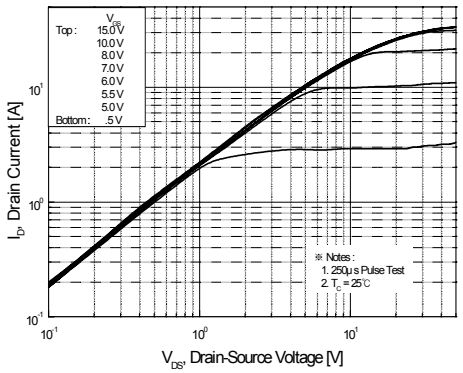


Figure 1. On-Region Characteristics

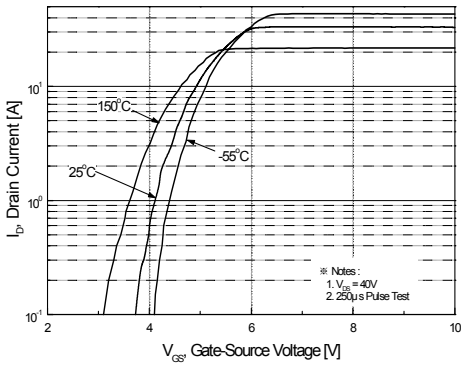


Figure 2. Transfer Characteristics

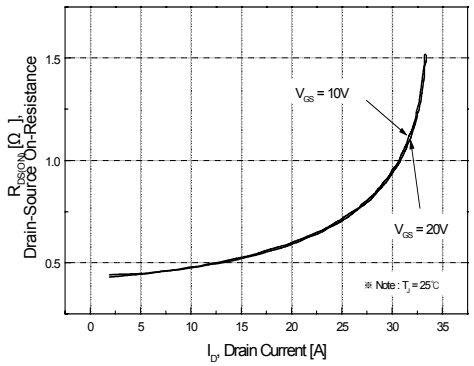


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

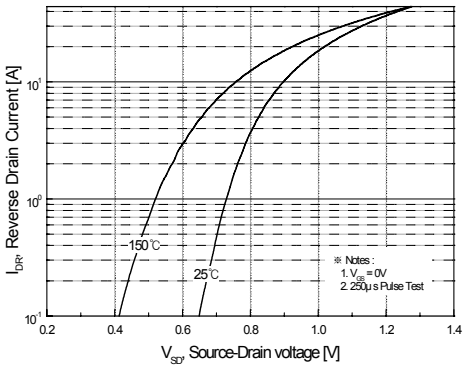


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

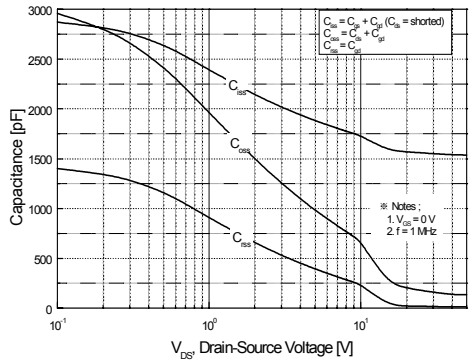


Figure 5. Capacitance Characteristics

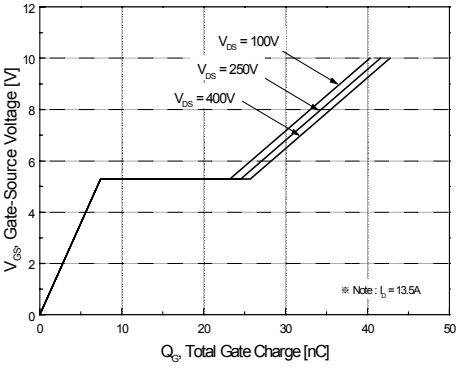


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

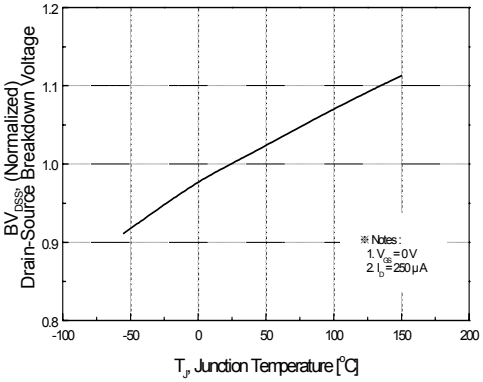


Figure 7. Breakdown Voltage Variation vs Temperature

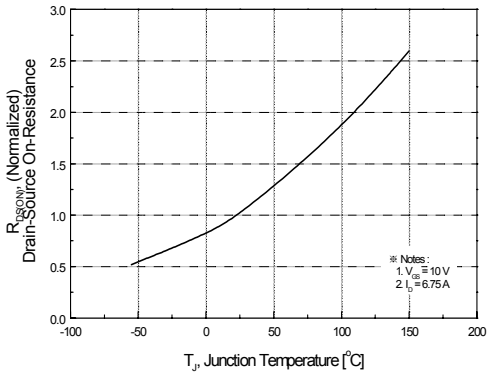


Figure 8. On-Resistance Variation vs Temperature

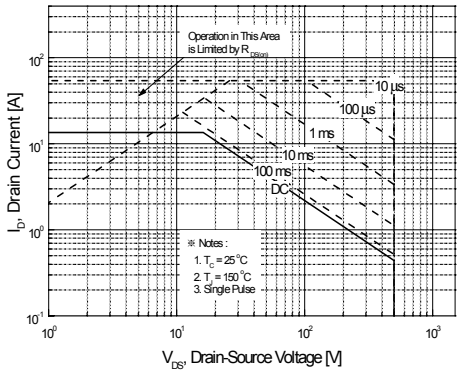


Figure 9. Maximum Safe Operating Area

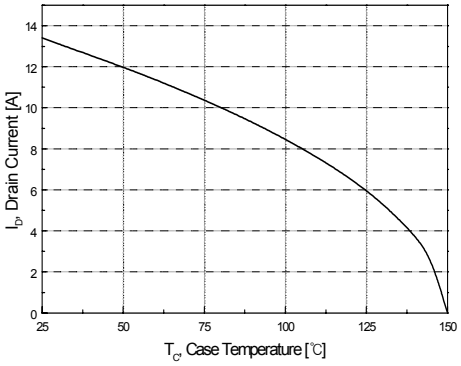


Figure 10. Maximum Drain Current vs Case Temperature

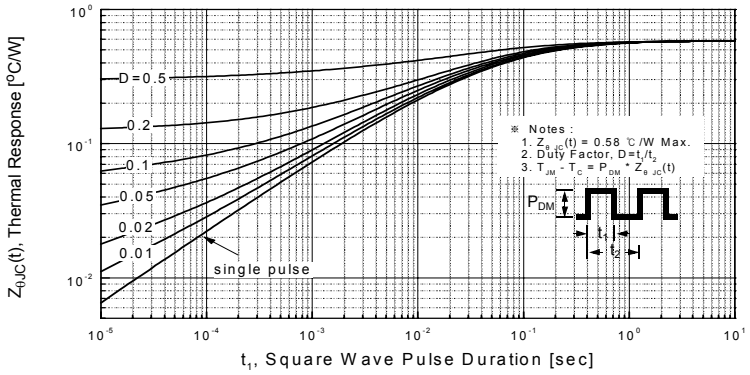


Figure 11. Transient Thermal Response Curve for FQA13N50C

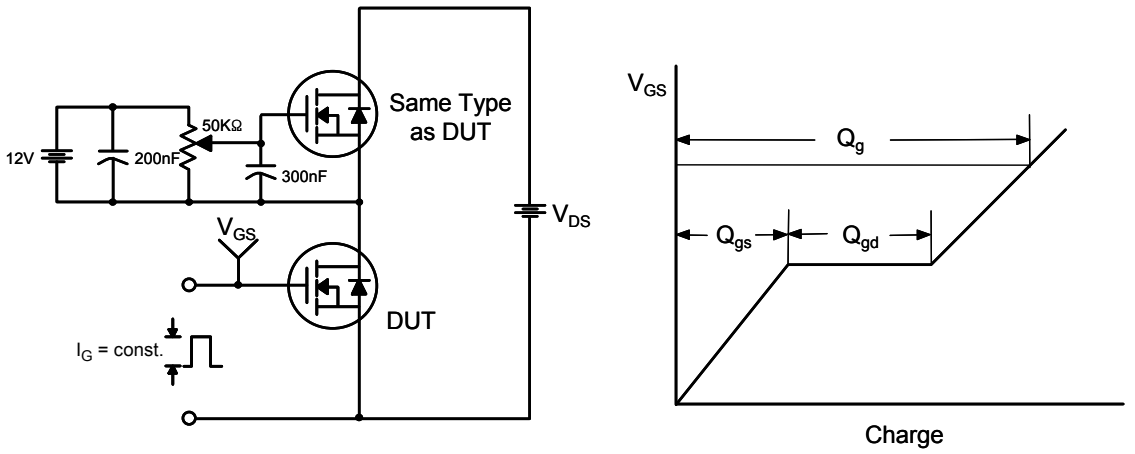


Figure 12. Gate Charge Test Circuit & Waveform

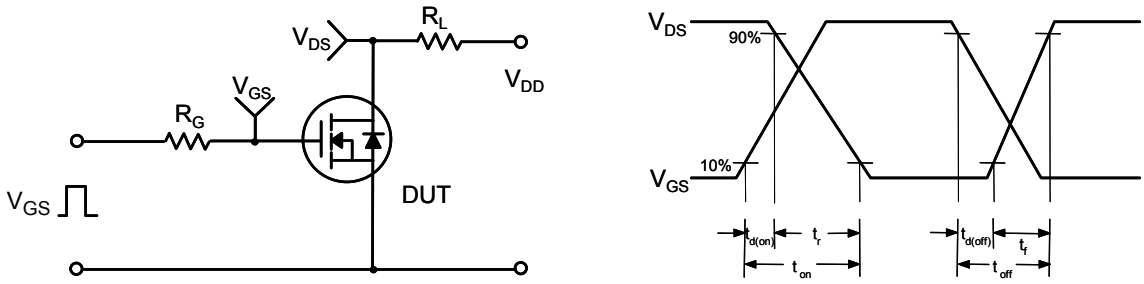


Figure 13. Resistive Switching Test Circuit & Waveforms

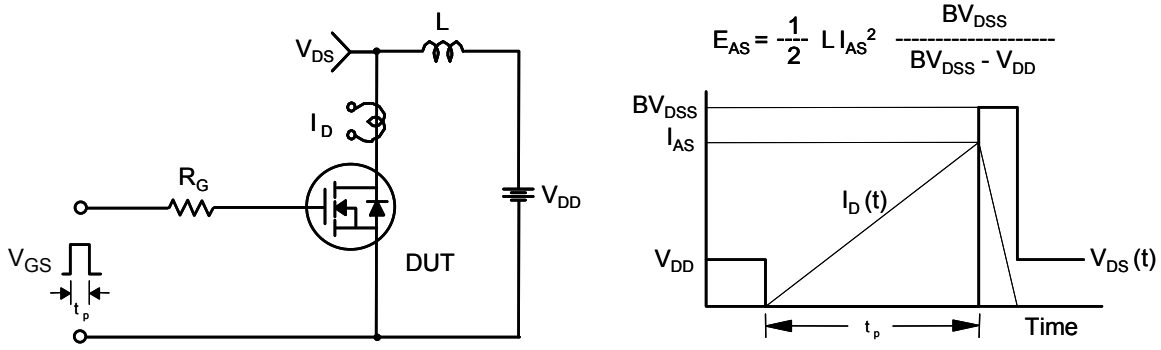


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

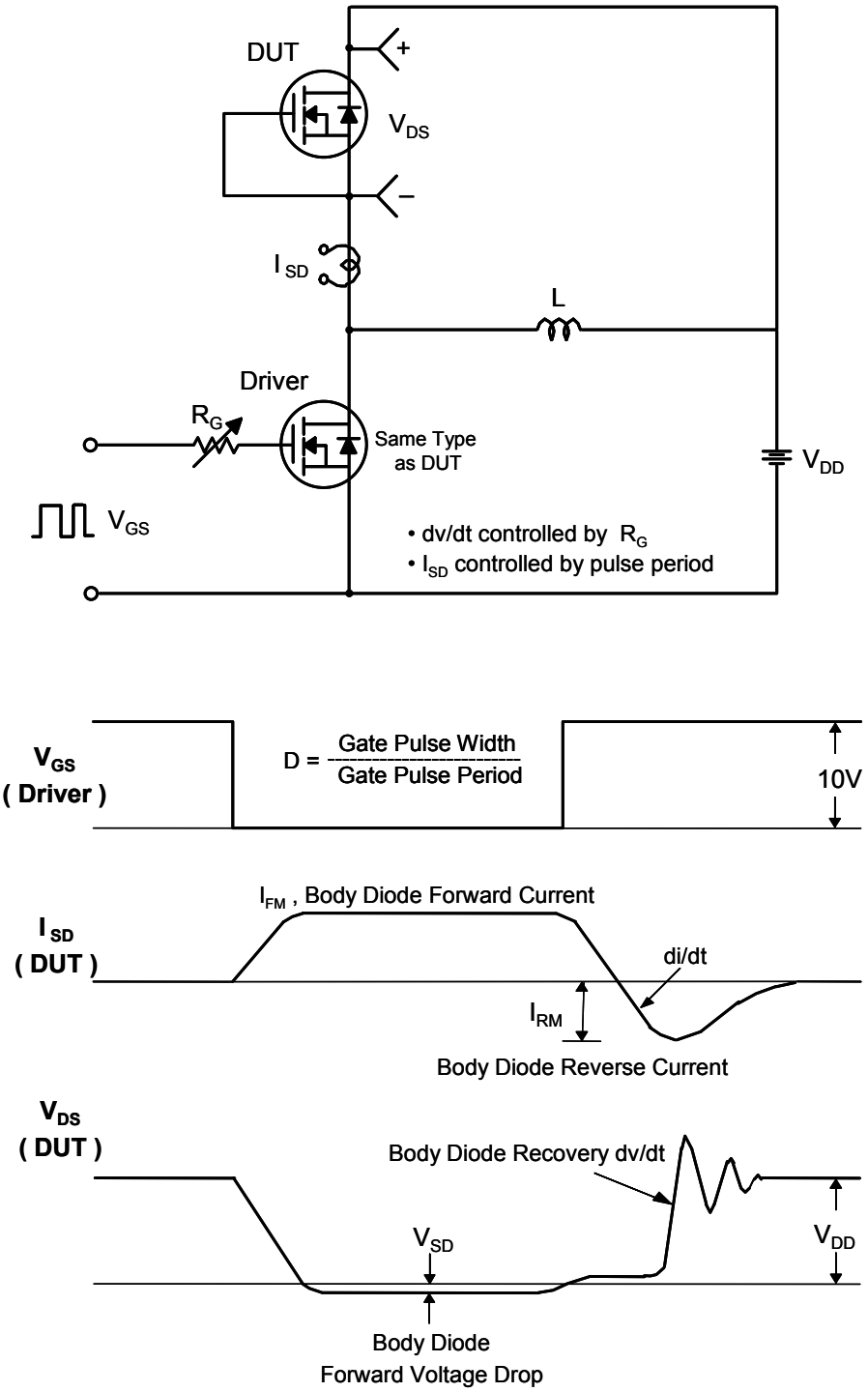
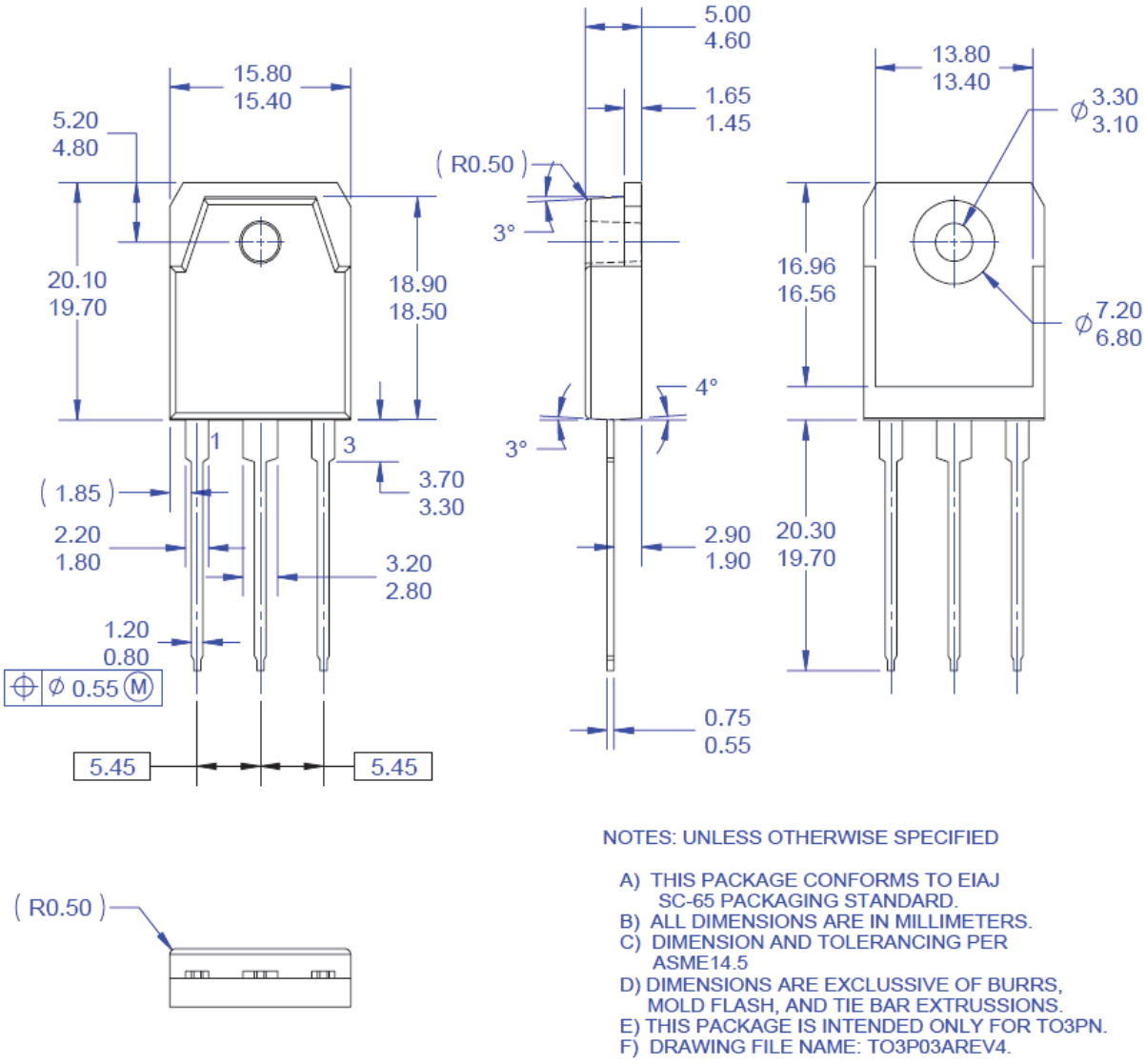


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSION AND TOLERANCING PER ASME14.5
D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.
E) THIS PACKAGE IS INTENDED ONLY FOR TO3PN.
F) DRAWING FILE NAME: TO3P03AREV4.

Figure 16. TO3, 3-Lead, Plastic, EIAJ SC-65

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