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December 2013

# FQU3N50C

# N-Channel QFET® MOSFET

500 V, 2.5 A, 2.5 Ω

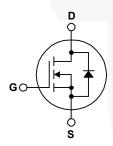
## **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### **Features**

- 2.5 A, 500 V,  $R_{DS(on)}$  = 2.5  $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 1.25 A
- Low Gate Charge (Typ. 10 nC)
- Low Crss (Typ. 8.5 pF)
- 100% Avalanche Tested





## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FQU3N50CTU	Unit	
$V_{DSS}$	Drain-Source Voltage		500	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		2.5	Α
	- Continuous (T <sub>C</sub> = 100°C)		1.5	А
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	10	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2		200	mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	2.5	А
E <sub>AR</sub>	Repetitive Avalanche Energy		3.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)		35	W
	- Derate above 25°C		0.28	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering, 1/8			

## **Thermal Characteristics**

Symbol	Parameter	FQU3N50CTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in2 Pad of 2-oz Copper), Max.	50	°C/W

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQU3N50CTU	FQU3N50C	IPAK	Tube	N/A	N/A	75 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	teristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS}$ = 0 V, $I_{D}$ = 250 $\mu$ A	500			V
ΔBV <sub>DSS</sub> / ΔΤ <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C		0.7		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V			1	μΑ
		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Charact	eristics				•	
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.25 A		2.1	2.5	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 1.25 A		1.5		S
Dynamic Cl	haracteristics			l.		Į.
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		280	365	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		50	65	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			8.5	11	pF
Switching C	Characteristics			1	1	
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 250 \text{ V}, I_D = 2.5\text{A},$		10	30	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		25	60	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			35	80	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		25	60	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 2.5A,		10	13	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V	/	1.5		nC
$Q_{gd}$	Gate-Drain Charge	(Note 4)		5.5		nC
Drain-Source	ce Diode Characteristics and Maximum Ratings			1	1/2	Į.
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				2.5	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				10	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2.5 \text{ A}$			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3 A,	4)	170	//	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dl <sub>F</sub> / dt = 100 A/μs		0.7		μС

#### NOTES:

<sup>1.</sup> Repetitive rating : pulse-width limited by maximum junction temperature.

<sup>2.</sup> L = 58 mH, I<sub>AS</sub> = 2.5 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25°C.

 $<sup>3.~</sup>I_{SD} \leq 2.5~A,~di/dt \leq \!\! 200~A/\mu s,~V_{DD} \leq BV_{DSS,}~starting~~T_J = 25^{\circ}C.$ 

<sup>4.</sup> Essentially independent of operating temperature.

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

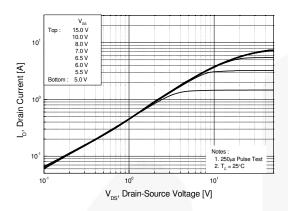
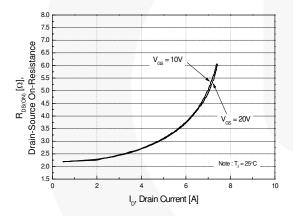


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage



**Figure 5. Capacitance Characteristics** 

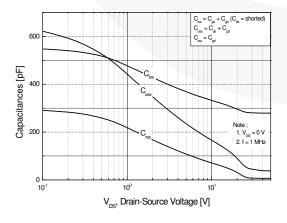


Figure 2. Transfer Characteristics

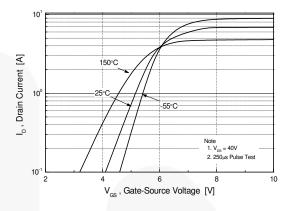
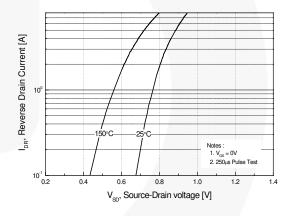
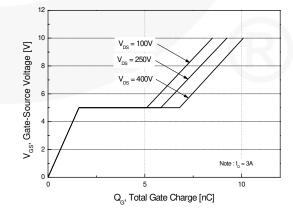


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue



**Figure 6. Gate Charge Characteristics** 



# Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

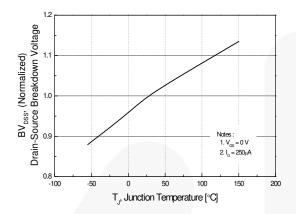


Figure 8. On-Resistance Variation vs. Temperature

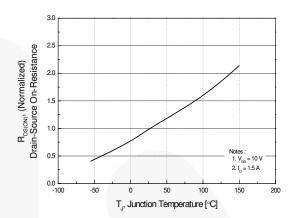


Figure 9. Maximum Safe Operating Area

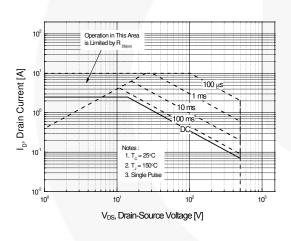


Figure 10. Maximum Drain Current vs. Case Temperature

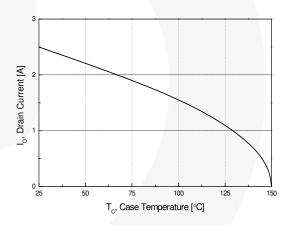
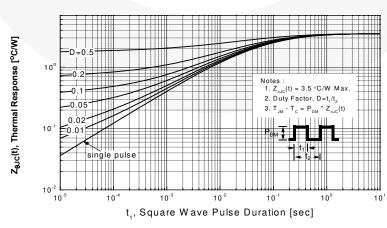


Figure 11. Transient Thermal Response Curve



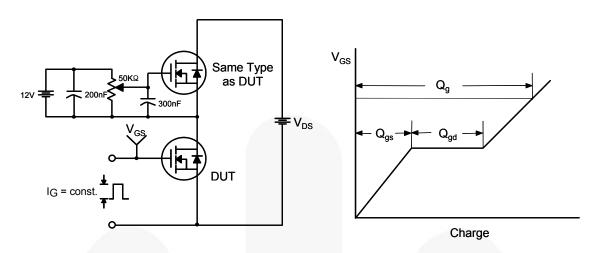


Figure 12. Gate Charge Test Circuit & Waveform

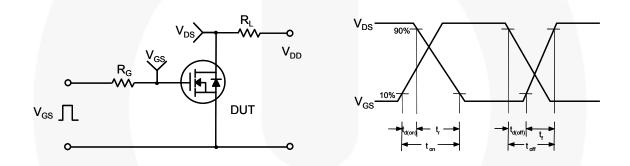


Figure 13. Resistive Switching Test Circuit & Waveforms

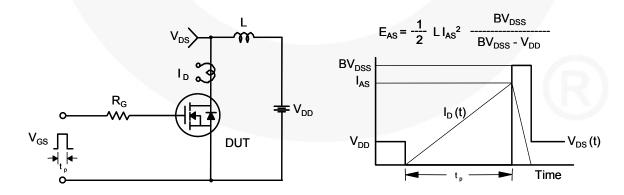


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

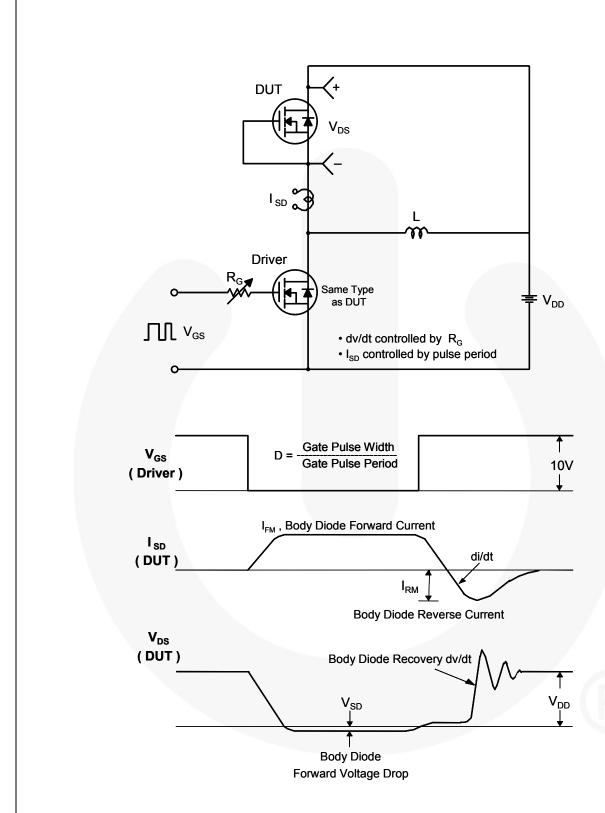


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

## **Mechanical Dimensions**

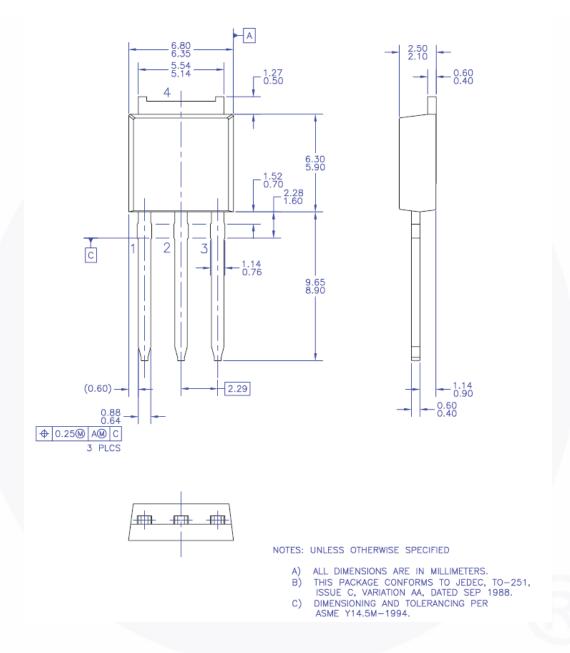


Figure 16. TO-251 (I-PAK), Molded, 3-Lead, Option AA

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