



ON Semiconductor®

# FQD9N25 / FQU9N25

## N-Channel QFET® MOSFET

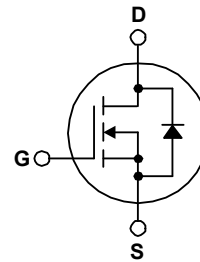
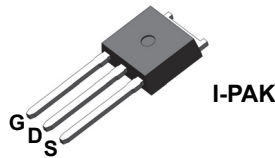
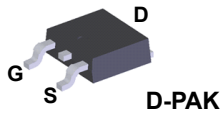
250 V, +4 A, (  $\&\$$ 'a  $\Omega$

### Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 7.4 A, 250 V,  $R_{DS(on)} = 420 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 3.7 \text{ A}$
- Low Gate Charge (Typ. 15.5 nC)
- Low  $C_{rss}$  (Typ. 15 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQD9N25TM FQD9N25TM-F080 FQU9N25TU	Unit
$V_{DSS}$	Drain-Source Voltage	250	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	7.4	A
		4.7	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	29.6	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	165	mJ
$I_{AR}$	Avalanche Current (Note 1)	7.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.5	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	55	W
		0.44	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQD9N25TM FQD9N25TM-F080 FQU9N25TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.27	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> pad of 2 oz copper), Max.	50	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD9N25TM	FQD9N25	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FQD9N25TM-F080	FQD9N25	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FQU9N25TU	FQU9N25	I-PAK	Tube	N/A	N/A	70 units

## Electrical Characteristics $T_c = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	250	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.2	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 200\text{ V}, T_c = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.7\text{ A}$	--	0.33	0.42	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 3.7\text{ A}$	--	6.8	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	540	700	pF
$C_{oss}$	Output Capacitance		--	110	145	pF
$C_{rss}$	Reverse Transfer Capacitance		--	15	20	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125\text{ V}, I_D = 9.4\text{ A},$ $R_G = 25\ \Omega$	--	13	35	ns
$t_r$	Turn-On Rise Time		--	105	220	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	60	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	45	100
$Q_g$	Total Gate Charge	$V_{DS} = 200\text{ V}, I_D = 9.4\text{ A},$ $V_{GS} = 10\text{ V}$	--	15.5	20	nC
$Q_{gs}$	Gate-Source Charge		--	3.8	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	8.5	--

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	7.4	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	29.6	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 7.4\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 9.4\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	150	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	0.8	--	$\mu\text{C}$

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 4.8\text{ mH}, I_{AS} = 7.4\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 9.4\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

## Typical Characteristics

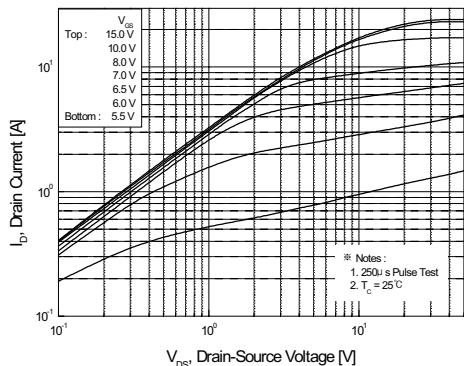


Figure 1. On-Region Characteristics

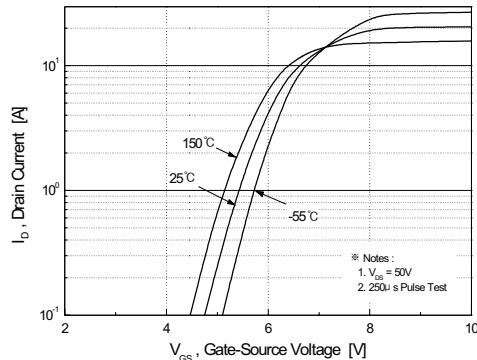


Figure 2. Transfer Characteristics

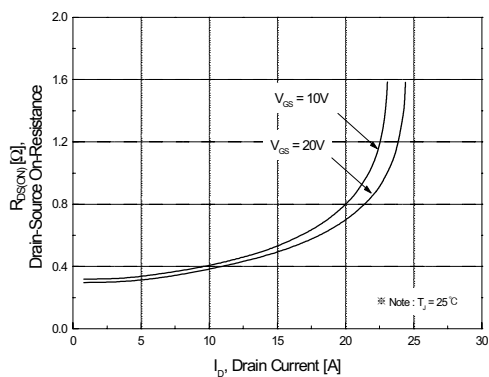


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

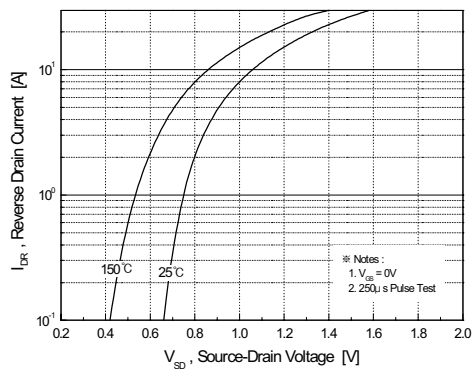


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

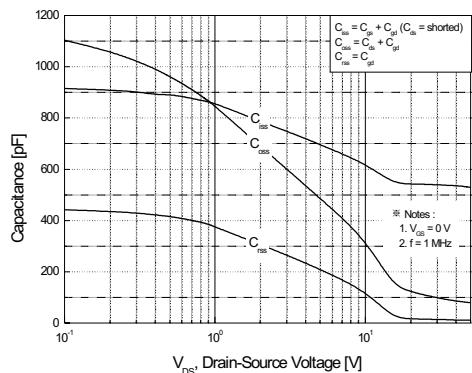


Figure 5. Capacitance Characteristics

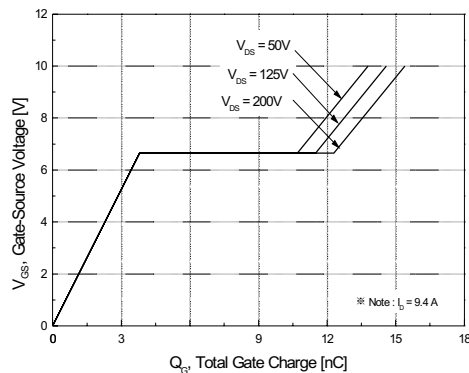
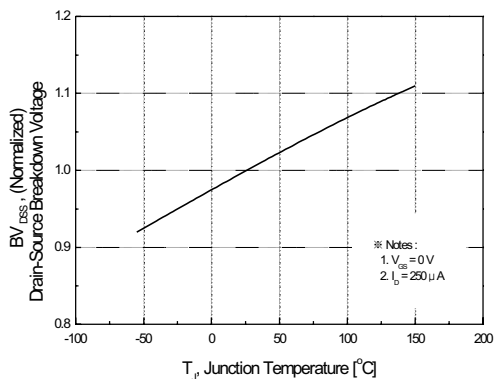
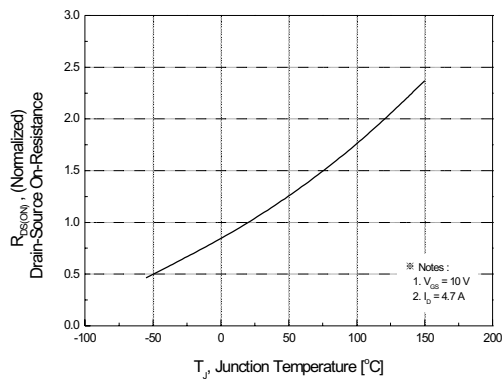


Figure 6. Gate Charge Characteristics

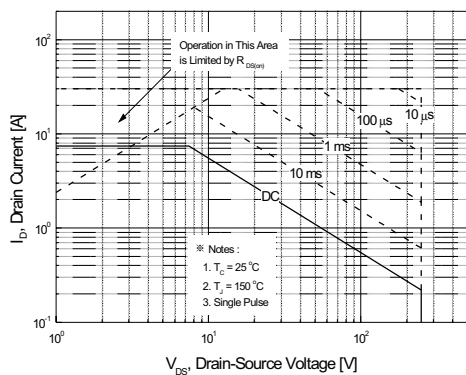
## Typical Characteristics (Continued)



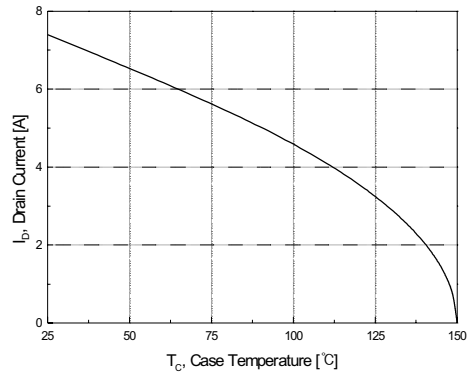
**Figure 7. Breakdown Voltage Variation vs. Temperature**



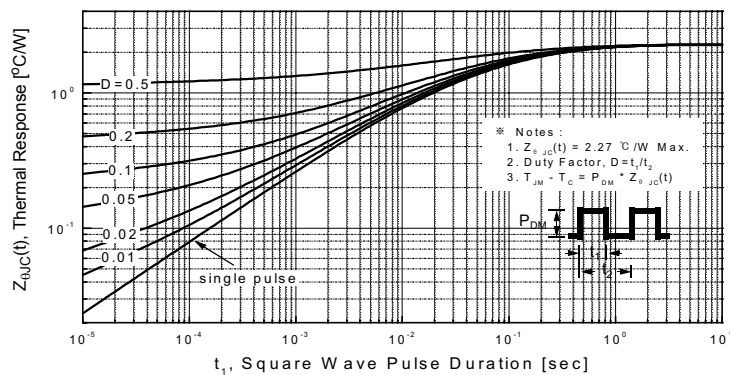
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

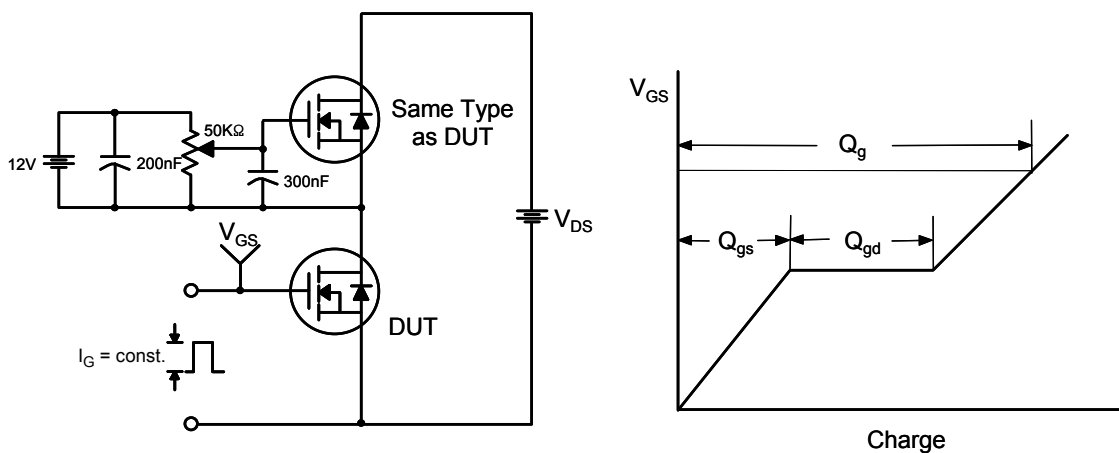


Figure 12. Gate Charge Test Circuit & Waveform

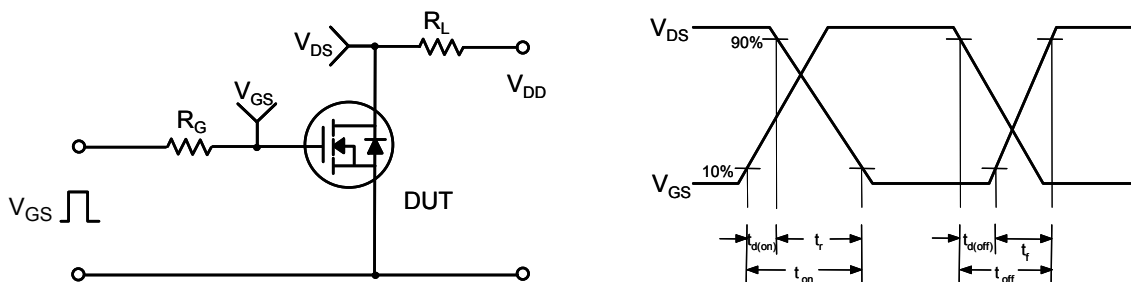


Figure 13. Resistive Switching Test Circuit & Waveforms

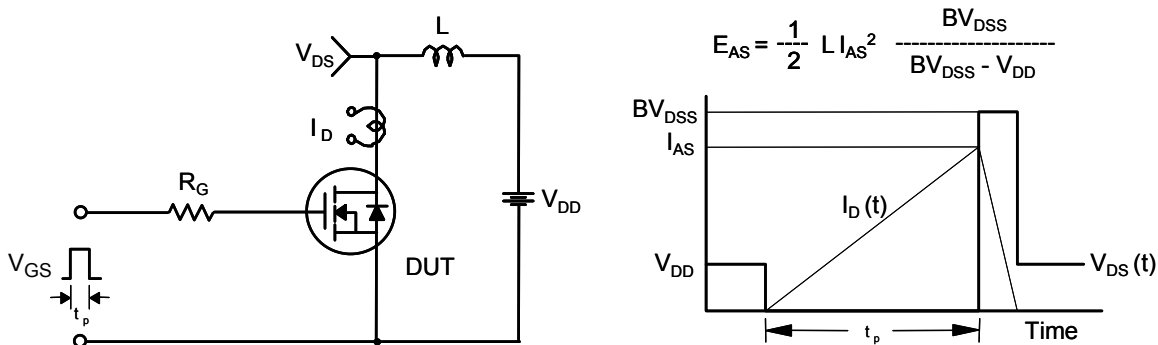


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

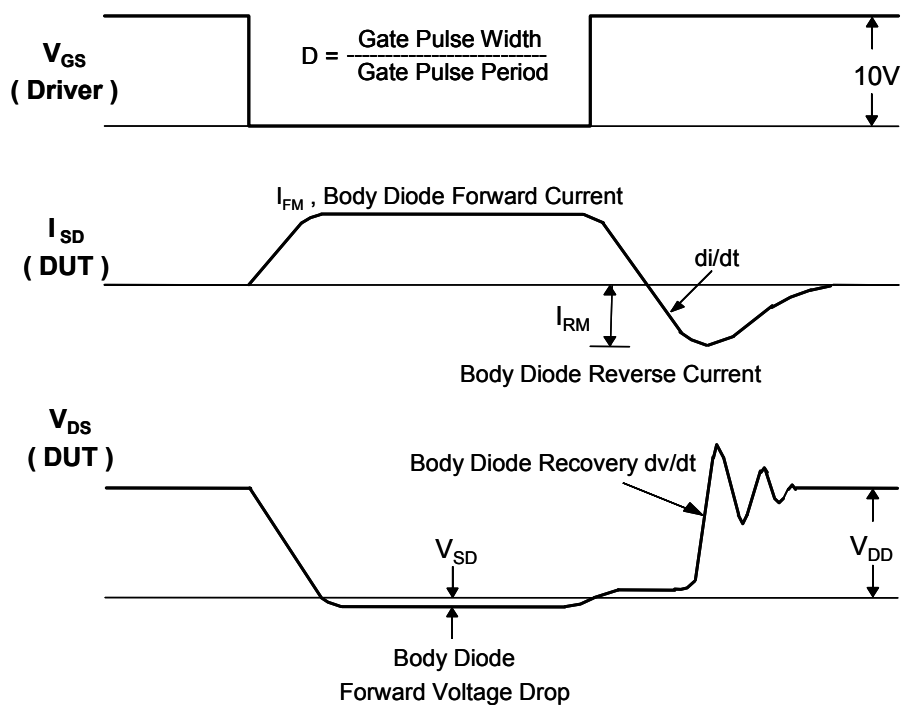
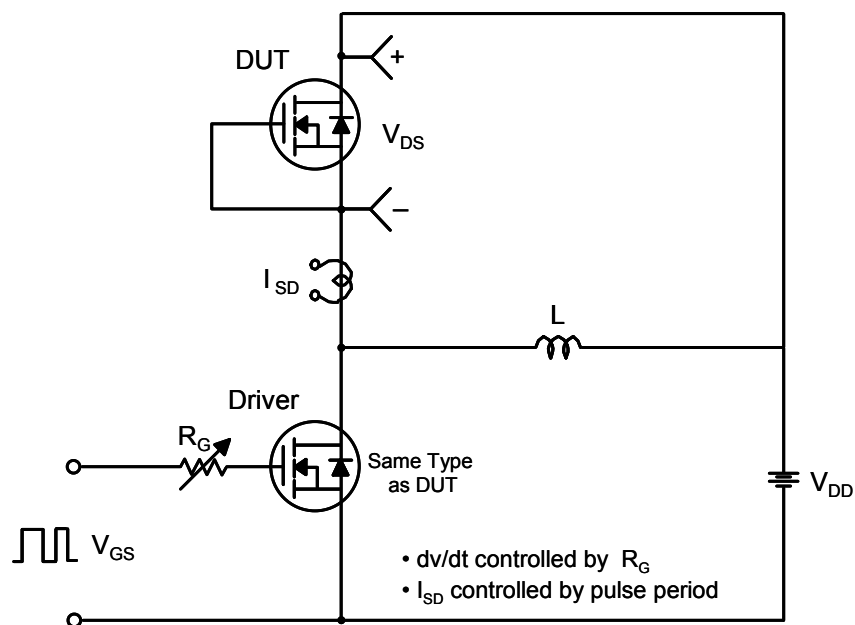
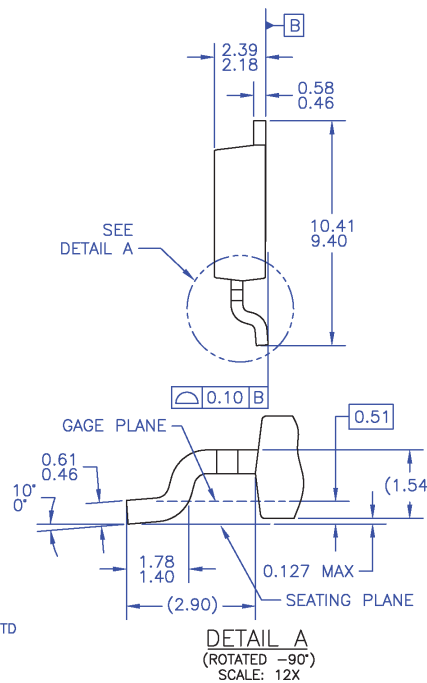
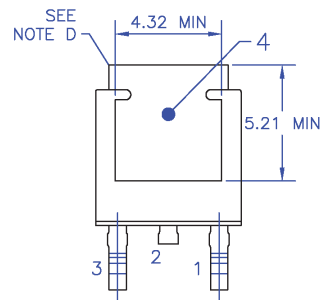
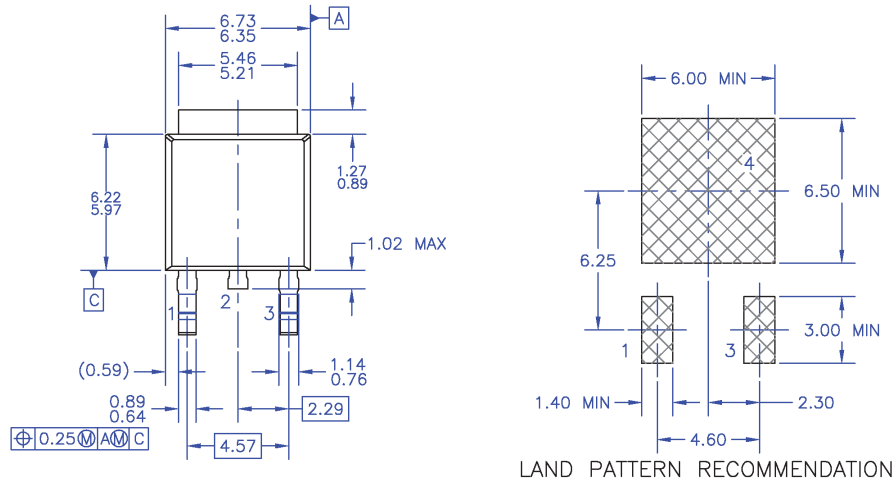


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions

### TO-252 3L (DPAK) FQD9N25TM



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

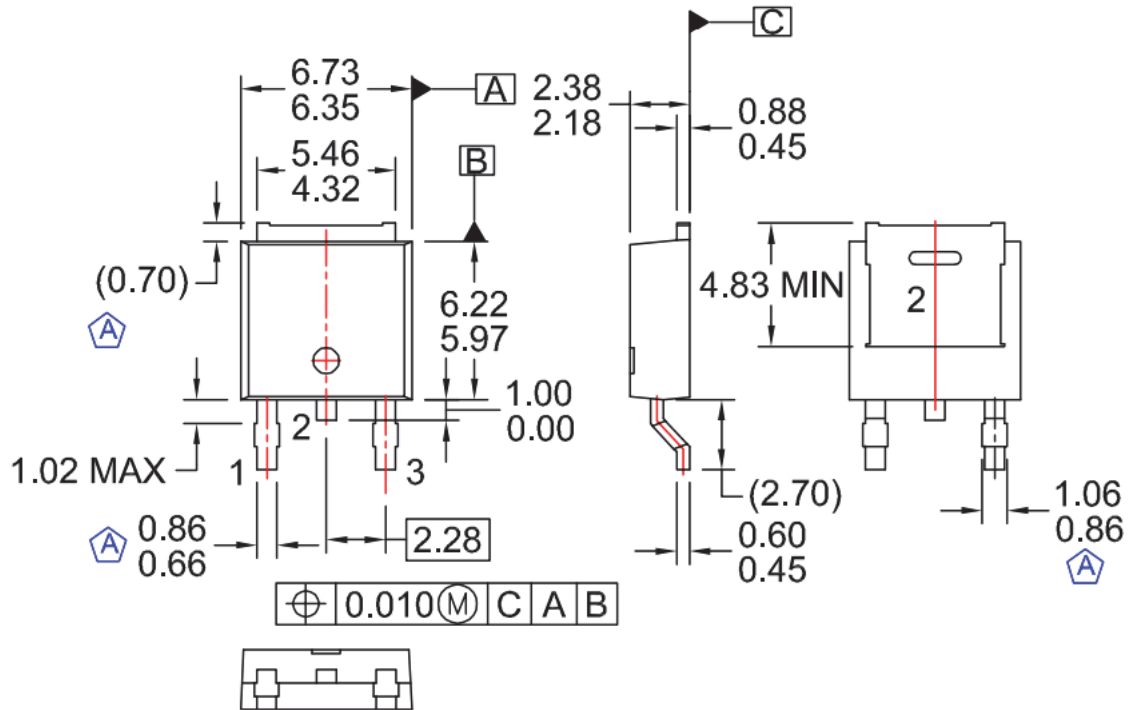
**Figure 16. TO252 (D-PAK), Molded, 3 Lead, Option AA&AB**

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Dimension in Millimeters

## Mechanical Dimensions

### TO-252 3L (DPAK) FQD9N25TM\_F080



NOTES: UNLESS OTHERWISE SPECIFIED

(A) CONFORMS TO JEDEC TO-252 VARIATION AB EXCEPT WHERE NOTED

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DRAWING CONFORMS TO ASME Y14.5M-1994

D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

E) FORMERLY NAMED BD1733

F) DRAWING FILE NAME: MKT-TO252D03REV1

**Figure 17. 3LD, TO-252, Jedec TO-252 VAR. AB, Surface Mount**

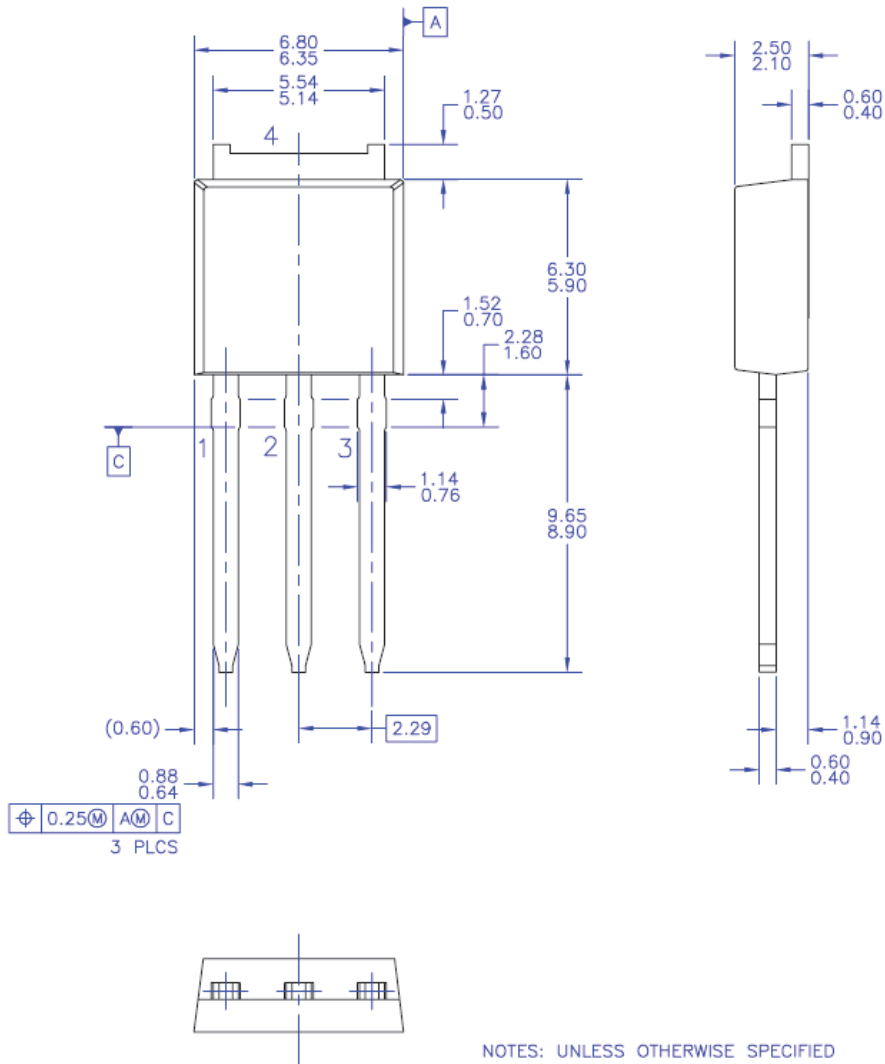
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Dimension in Millimeters



## Mechanical Dimensions

### TO-251 3L (IPAK)



**Figure 18. TO251 (IPAK) Molded 3 Lead**

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Dimension in Millimeters

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